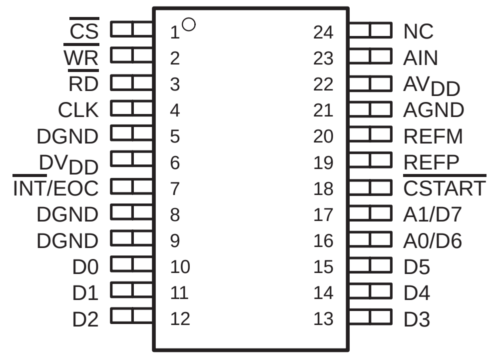
features

- **Fast Throughput Rate: 1.25 MSPS at 5 V, 625 KSPS at 3 V**
- **Wide Analog Input: 0 V to AV_{DD}**
- **Differential Nonlinearity Error: < ± 0.5 LSB**
- **Integral Nonlinearity Error: < ± 0.5 LSB**
- **Single 2.7-V to 5.5-V Supply Operation**
- **Low Power: 12 mW at 3 V and 35 mW at 5 V**
- **Auto Power Down of 1 mA Max**
- **Software Power Down: 10 µA Max**
- **Internal OSC**
- **Hardware Configurable**
- **DSP and Microcontroller Compatible Parallel Interface**
- **Binary/Twos Complement Output**
- **Hardware Controlled Extended Sampling**
- **Hardware or Software Start of Conversion**

applications

- **Mass Storage and HDD**
- **Automotive**
- **Digital Servos**
- **Process Control**
- **General-Purpose DSP**
- **Image Sensor Processing**

DW OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLV571 is an 8-bit data acquisition system that combines a high-speed 8-bit ADC and a parallel interface. The device contains two on-chip control registers allowing control of software conversion start and power down via the bidirectional parallel port. The control registers can be set to a default mode using a dummy $\overline{RD}$ while $\overline{WR}$ is tied low allowing the registers to be hardware configurable.

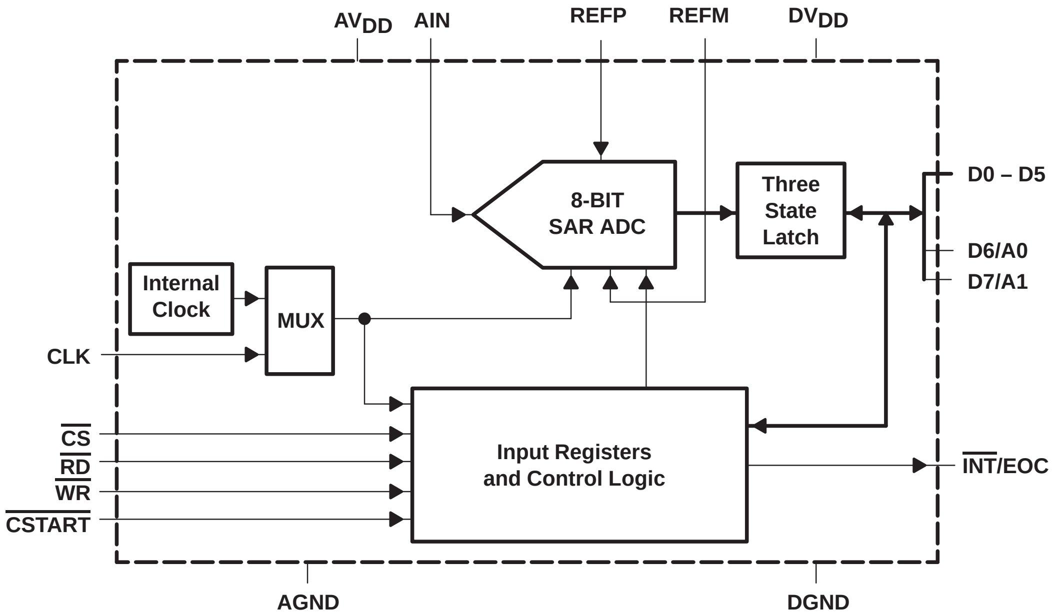
The TLV571 operates from a single 2.7-V to 5.5-V power supply. It accepts an analog input range from 0 V to AV_{DD} and digitizes the input at a maximum 1.25 MSPS throughput rate at 5 V. The power dissipations are only 12 mW with a 3-V supply or 35 mW with a 5-V supply. The device features an auto power-down mode that automatically powers down to 1 mA 50 ns after conversion is performed. In software power-down mode, the ADC is further powered down to only 10 µA.

Very high throughput rate, simple parallel interface, and low power consumption make the TLV571 an ideal choice for high-speed digital signal processing.

AVAILABLE OPTIONS

T_A	PACKAGE	
	24 TSSOP (PW)	24 SOIC (DW)
–40°C to 85°C	TLV571IPW	TLV571IDW

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	21		Analog ground
AIN	23	I	ADC analog input
AV_{DD}	22		Analog supply voltage, 2.7 V to 5.5 V
A0/D6	16	I/O	Bidirectional 3-state data bus. D6/A0 along with D7/A1 is used as address lines to access CR0 and CR1 for initialization.
A1/D7	17	I/O	Bidirectional 3-state data bus. D7/A1 along with D6/A0 is used as address lines to access CR0 and CR1 for initialization.
CLK	4	I	External clock input
$\overline{CS}$	1	I	Chip select. A logic low on $\overline{CS}$ enables the TLV571.
$\overline{CSTART}$	18	I	Hardware sample and conversion start input. The falling edge of $\overline{CSTART}$ starts sampling and the rising edge of $\overline{CSTART}$ starts conversion.
DGND	5, 8, 9		Digital ground
DV_{DD}	6		Digital supply voltage, 2.7 V to 5.5 V
D0 – D5	10–15	I/O	Bidirectional 3-state data bus
$\overline{INT}$/EOC	7	O	End-of-conversion/interrupt
NC	24		Not connected
$\overline{RD}$	3	I	Read data. A falling edge on $\overline{RD}$ enables a read operation on the data bus when $\overline{CS}$ is low.
REFM	20	I	Lower reference voltage (nominally ground). REFM must be supplied or REFM pin must be grounded.
REFP	19	I	Upper reference voltage (nominally AV_{DD}). The maximum input voltage range is determined by the difference between the voltage applied to REFP and REFM.
$\overline{WR}$	2	I	Write data. A rising edge on the $\overline{WR}$ latches in configuration data when $\overline{CS}$ is low. When using software conversion start, a rising edge on $\overline{WR}$ also initiates an internal sampling start pulse. When $\overline{WR}$ is tied to ground, the ADC in nonprogrammable (hardware configuration mode).

detailed description

analog-to-digital SAR converter

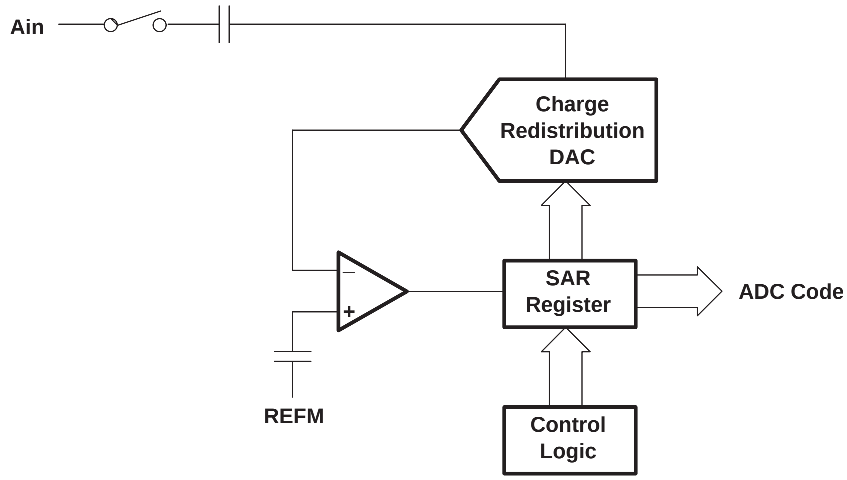


Figure 1

The TLV571 is a successive-approximation ADC utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on Ain during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

sampling frequency, f_s

The TLV571 requires 16 CLKs for each conversion, therefore the equivalent maximum sampling frequency achievable with a given CLK frequency is:

$f_{s(max)} = (1/16)\ f_{CLK}$

The TLV571 is software configurable. The first two MSB bits, D(7,6) are used to address which register to set. The remaining six bits are used as control data bits. There are two control registers, CR0 and CR1, that are user configurable. All of the register bits are written to the control register during write cycles. A description of the control registers is shown in Figure 2.

detailed description (continued)

control registers

A1	A0	D5	D4	D3	D2	D1	D0

Control Register Zero (CR0)

A(1:0)=00

D5	D4	D3	D2	D1	D0
STARTSEL	PROGEOC	CLKSEL	SWPWDN	Don’t Care	Don’t Care
0: HARDWARE START (CSTART) 1: SOFTWARE START	0: INT 1: EOC	0: Internal Clock 1: External Clock	0: NORMAL 1: Powerdown	Don’t Care	Don’t Care

Control Register One (CR1)

A(1:0)=01

D5	D4	D3	D2	D1	D0
Reserved	OSCSPD	0 Reserved	0 Reserved	OUTCODE	Reserved
0: Reserved Bit Always Write 0	0: INT. OSC. SLOW 1: INT. OSC. FAST	0: Reserved Bit Always Write 0	0: Reserved Bit, Always Write 0	0: Binary 1: 2’s Complement	0: Reserved Bit, Always Write 0

Figure 2. Input Data Format

hardware configuration option

The TLV571 can configure itself. This option is enabled when the $\overline{\text{WR}}$ pin is tied to ground and a dummy $\overline{\text{RD}}$ signal is applied. The ADC is now fully configured. Zeros or default values are applied to both control registers. The ADC is configured ideally for 3-V operation, which means the internal OSC is set at 10 MHz and hardware start of conversion using $\overline{\text{CSTART}}$.

ADC conversion modes

The TLV571 provides two start of conversion modes. Table 1 explains these modes in more detail.

detailed description (continued)

Table 1. Conversion Modes

START OF CONVERSION	OPERATION	COMMENTS – FOR INPUT
Hardware start (CSTART) CR0.D5 = 0	• Repeated conversions from AIN • $\overline{\text{CSTART}}$ falling edge to start sampling • $\overline{\text{CSTART}}$ rising edge to start conversion • If in INT mode, one $\overline{\text{INT}}$ pulse generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion, and return high at end of conversion.	$\overline{\text{CSTART}}$ rising edge must be applied a minimum of 5 ns before or after CLK rising edge.
Software start CR0.D5 = 1	• Repeated conversions from AIN • $\overline{\text{WR}}$ rising edge to start sampling initially. Thereafter, sampling occurs at the rising edge of $\overline{\text{RD}}$. • Conversion begins after 6 clocks after sampling has begun. Thereafter, if in INT mode, one $\overline{\text{INT}}$ pulse generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion and return high at end of conversion.	With external clock, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ rising edge must be a minimum 5 ns before or after CLK rising edge.

configure the device

The device can be configured by writing to control registers CR0 and CR1.

Table 2. TLV571 Programming Examples

REGISTER	INDEX		D5	D4	D3	D2	D1	D0	COMMENT
	D7	D6							
EXAMPLE1									
CR0	0	0	0	0	0	0	0	0	Normal, INT OSC
CR1	0	1	0	0	0	0	0	0	Binary
EXAMPLE2									
CR0	0	0	0	1	1	1	0	0	Power down, EXT OSC
CR1	0	1	0	0	0	0	1	0	2's complement output

power down

The TLV571 offers two power down modes, auto power down and software power down. This device will automatically proceed to auto power down mode if $\overline{\text{RD}}$ is not present one clock after conversion. Software power down is controlled directly by the user by pulling $\overline{\text{CS}}$ to DV_{DD}.

Table 3. Power Down Modes

PARAMETERS/MODES	AUTO POWER DOWN	SOFTWARE POWER DOWN ($\overline{\text{CS}}$ = DV_{DD})
Maximum power down dissipation current	1 mA	10 µA
Comparator	Power down	Power down
Clock buffer	Power down	Power down
Control registers	Saved	Saved
Minimum power down time	1 CLK	2 CLK
Minimum resume time	1 CLK	2 CLK

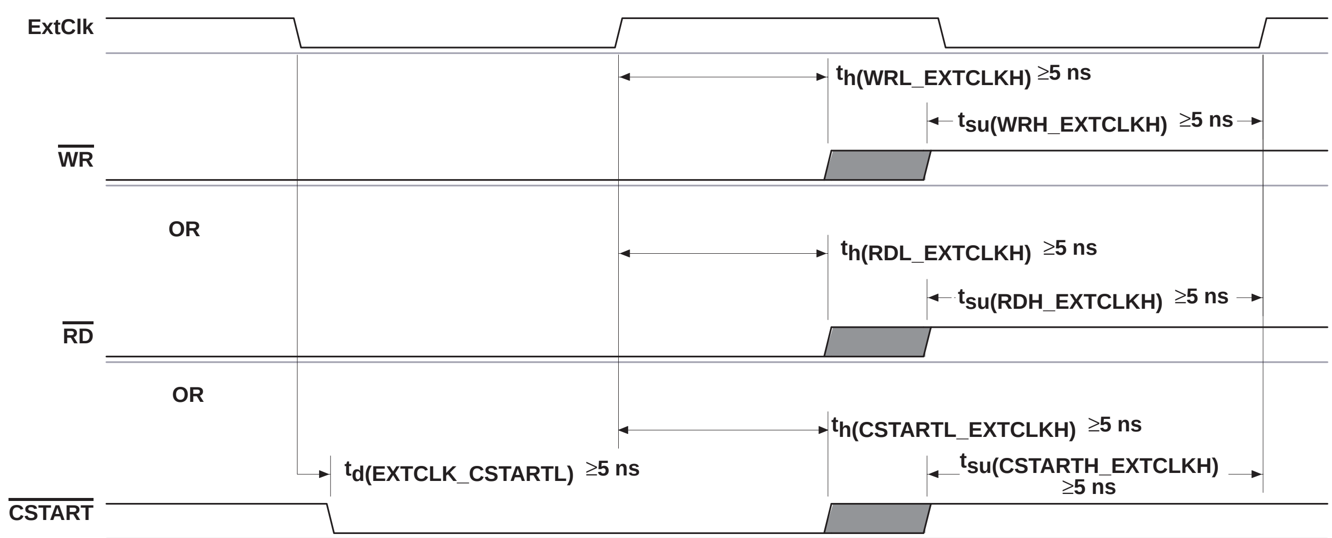
detailed description (continued)

reference voltage input

The TLV571 has two reference input pins: REFP and REFM. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REFP, REFM, and the analog input should not exceed the positive supply or be less than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REFP and is at zero when the input signal is equal to or lower than REFM.

sampling/conversion

All sampling, conversion, and data output in the device are started by a trigger. This could be the $\overline{\text{RD}}$, $\overline{\text{WR}}$, or $\overline{\text{CSTART}}$ signal depending on the mode of conversion and configuration. The rising edge of $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{CSTART}}$ signal are extremely important, since they are used to start the conversion. These edges need to stay close to the rising edge of the external clock (if it is used as CLK). The minimum setup and hold time with respect to the rising edge of the external clock should be 5 ns minimum. When the internal clock is used, this is not an issue since these two edges will start the internal clock automatically. Therefore, the setup time is always met. Software controlled sampling lasts 6 clock cycles. This is done via the CLK input or the internal oscillator if enabled. The input clock frequency can be 1 MHz to 20 MHz, translating into a sampling time from 0.6 µs to 0.3 µs. The internal oscillator frequency is 9 MHz minimum (ocillator frequency is between 9 MHz to 22 MHz), translating into a sampling time from 0.6 µs to 0.3 µs. Conversion begins immediately after sampling and lasts 10 clock cycles. This is again done using the external clock input (1 MHz–20 MHz) or the internal oscillator (9 MHz minimum) if enabled. Hardware controlled sampling, via $\overline{\text{CSTART}}$, begins on falling $\overline{\text{CSTART}}$ lasts the length of the active $\overline{\text{CSTART}}$ signal. This allows more control over the sampling time, which is useful when sampling sources with large output impedances. On rising $\overline{\text{CSTART}}$, conversion begins. Conversion in hardware controlled mode also lasts 10 clock cycles. This is done using the external clock input (1 MHz–20 MHz) or the internal oscillator (9 MHz minimum) as is the case in software controlled mode.



NOTE: t_{su} = setup time, t_h = hold time

Figure 3. Trigger Timing – Software Start Mode Using External Clock

start of conversion mechanism

There are two ways to convert data: hardware and software. In the hardware conversion mode the ADC begins sampling at the falling edge of $\overline{\text{CSTART}}$ and begins conversion at the rising edge of $\overline{\text{CSTART}}$. Software start mode ADC samples for 6 clocks, then conversion occurs for ten clocks. The total sampling and conversion process lasts only 16 clocks in this case. If $\overline{\text{RD}}$ is not detected during the next clock cycle, the ADC automatically proceeds to a power-down state. Data is valid on the rising edge of $\overline{\text{INT}}$ in both conversion modes.

hardware CSTART conversion

external clock

With $\overline{\text{CS}}$ low and $\overline{\text{WR}}$ low, data is written into the ADC. The sampling begins at the falling edge of $\overline{\text{CSTART}}$ and conversion begins at the rising edge of $\overline{\text{CSTART}}$. At the end of conversion, EOC goes from low to high, telling the host that conversion is ready to be read out. The external clock is active and is used as the reference at all times. With this mode, it is required that $\overline{\text{CSTART}}$ is not applied at the rising edge of the clock (see Figure 4).

start of conversion mechanism (continued)

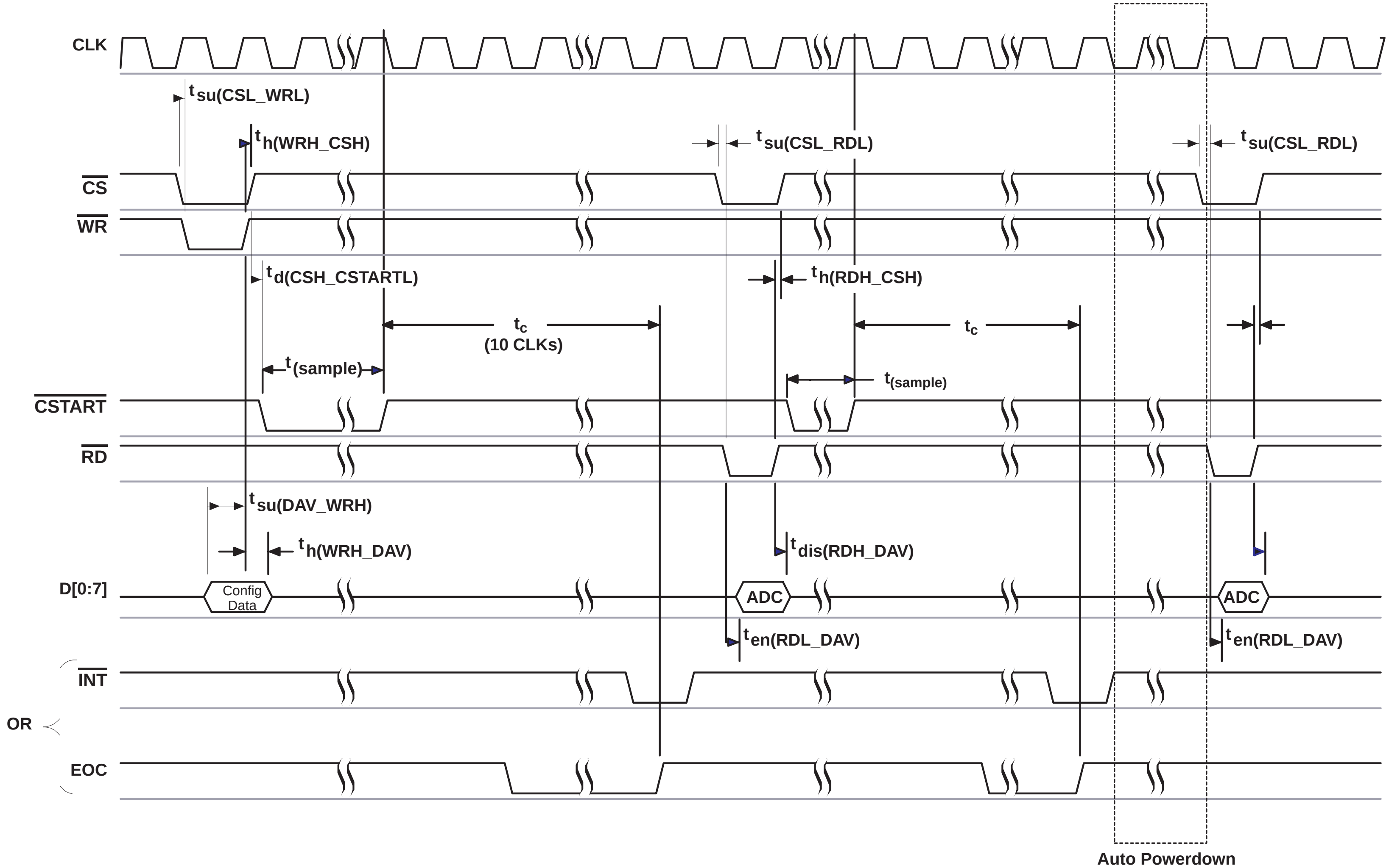


Figure 4. Input Conversion – Hardware $\overline{\text{CSTART}}$, External Clock

internal clock

With $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. The sampling begins at the falling edge of $\overline{CSTART}$, and conversion begins at the rising edge of $\overline{CSTART}$. The internal clock turns on at the rising edge of $\overline{CSTART}$. The internal clock is disabled after each conversion.

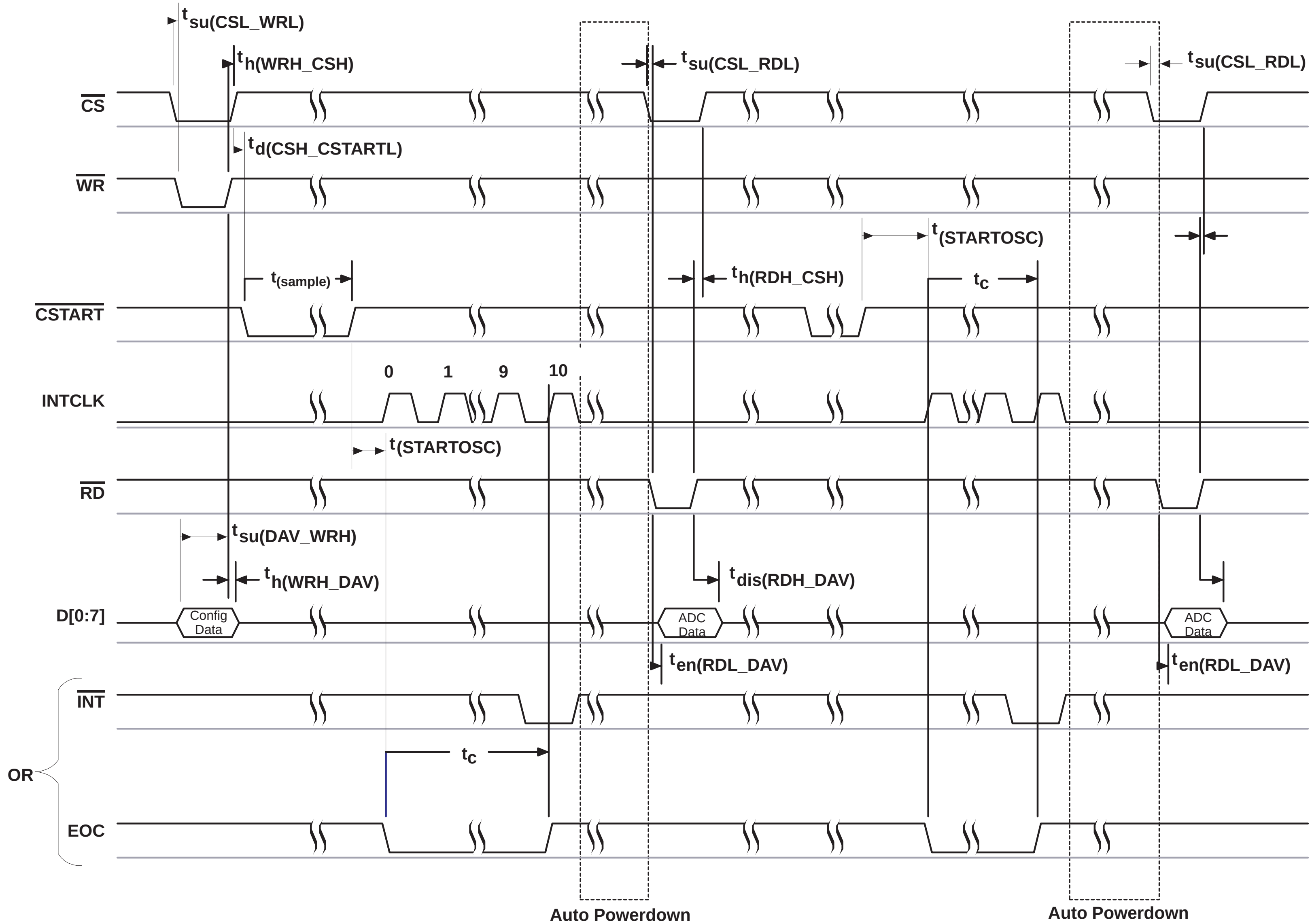


Figure 5. Input Conversion – Hardware $\overline{CSTART}$, Internal Clock

software START conversion

external clock

With $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. Sampling begins at the rising edge of $\overline{WR}$. The conversion process begins 6 clocks after sampling begins. At the end of conversion, the $\overline{INT}$ goes low telling the host that conversion is ready to be read out. EOC B low during the conversion. The external clock is active and used as the reference at all times. With this mode, $\overline{WR}$ and $\overline{RD}$ should not be applied at the rising edge of the clock (see Figure 3).

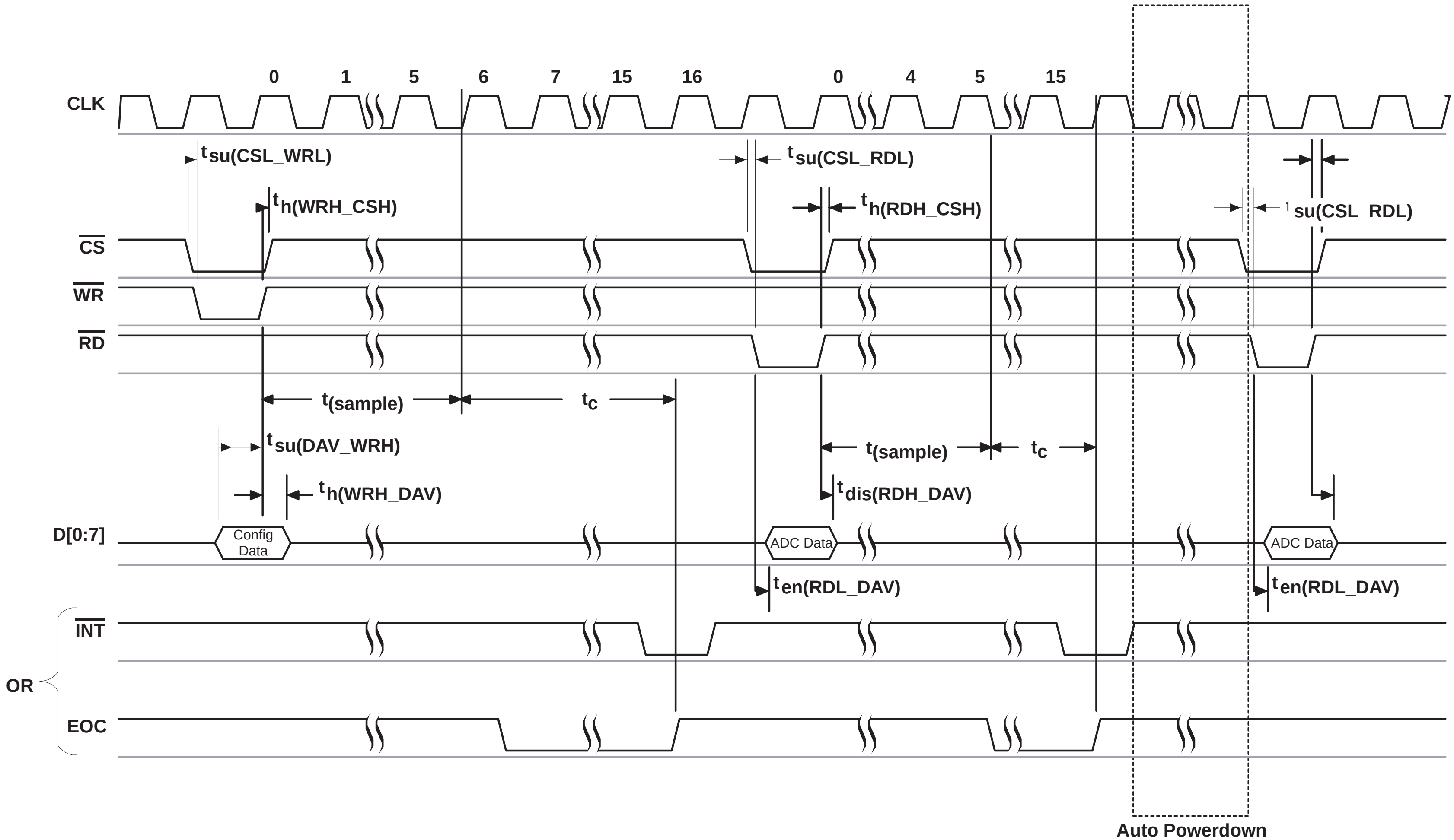


Figure 6. Input Conversion – Software Start, External Clock

software START conversion (continued)

internal clock

With $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. Sampling begins at the rising edge of $\overline{WR}$. Conversion begins 6 clocks after sampling begins. The internal clock begins at the rising edge of $\overline{WR}$. The internal clock is disabled after each conversion. Subsequent sampling begins at the rising edge of $\overline{RD}$.

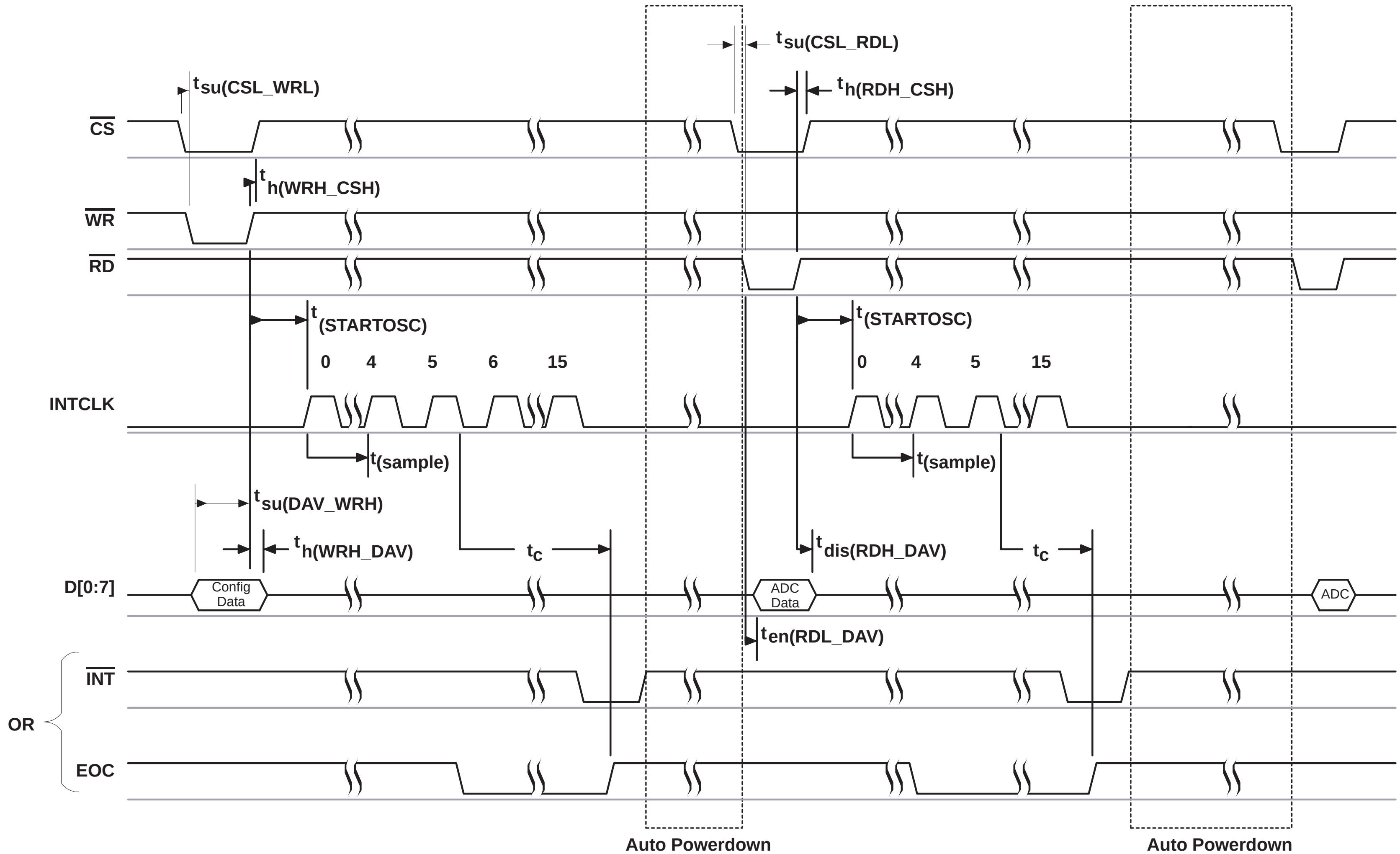


Figure 7. Input Conversion – Software Start, Internal Clock

software START conversion (continued)

system clock source

The TLV571 internally derives multiple clocks from the SYSCLK for different tasks. SYSCLK is used for most conversion subtasks. The source of SYSCLK is programmable via control register zero, bit 3. The source of SYSCLK is changed at the rising edge of $\overline{\text{WR}}$ of the cycle when CR0.D3 is programmed.

internal clock (CR0.D3 = 0, SYSCLK = internal OSC)

The TLV571 has a built-in 10 MHz OSC. When the internal OSC is selected as the source of SYSCLK, the internal clock starts with a delay (one half of the OSC period max) after the falling edge of the conversion trigger (either $\overline{\text{WR}}$, $\overline{\text{RD}}$, or $\overline{\text{CSTART}}$). The OSC speed can be set to 10 ± 1 MHz or 20 ± 2 MHz by setting register bit CR1.D4.

external clock (CR0.D3 = 1, SYSCLK = external clock)

The TLV571 is designed to accept an external clock input (CMOS/TTL logic) with frequencies from 1 MHz to 20 MHz.

host processor interface

The TLV571 provides a generic high-speed parallel interface that is compatible with high-performance DSPs and general-purpose microprocessors. The interface includes D(0–7), $\overline{\text{INT}}$/EOC, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.

output format

The data output format is unipolar (code 0 to 255). The output code format can be either binary or twos complement by setting register bit CR1.D1.

power up and initialization

After power up, $\overline{\text{CS}}$ must be low to begin an I/O cycle. $\overline{\text{INT}}$/EOC is initially high. The TLV571 requires two write cycles to configure the two control registers. The first conversion after the device has returned from the power down state may be invalid and should be disregarded.

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

software START conversion (continued)

signal-to-noise ratio + distortion (SINAD)

Signal-to-noise ratio + disortion is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$N = (SINAD - 1.76)/6.02$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, the effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

DSP interface

The TLV571 is a 8-bit single input channel analog-to-digital converter with throughput up to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V. To achieve 1.25 MSPS throughput, the ADC must be clocked at 20 MHz. Likewise to achieve 625 KSPS throughout, the ADC must be clocked at 10 MHz. The TLV571 can be easily interfaced to microcontrollers, ASICs, and DSPs. Figure 8 shows the pin connections to interface the TLV571 to the TMS320C6x DSP.

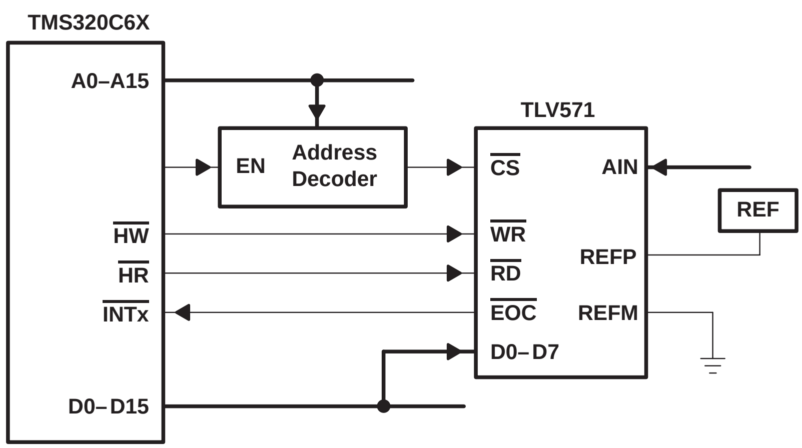


Figure 8. TMS320C6x DSP Interface

grounding and decoupling considerations

General practices should apply to the PCB design to limit high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. In most cases 0.1-μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Since their effectiveness depends largely on the proximity to the individual supply pin, they should be placed as close to the supply pins as possible.

To reduce high frequency and noise coupling, it is highly recommended that digital and analog grounds be shorted immediately outside the package. This can be accomplished by running a low impedance line between DGND and AGND under the package.

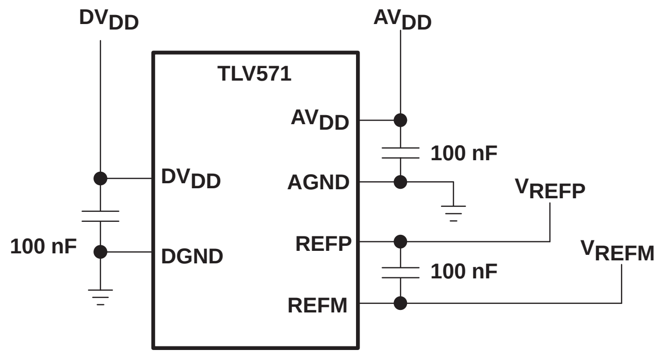
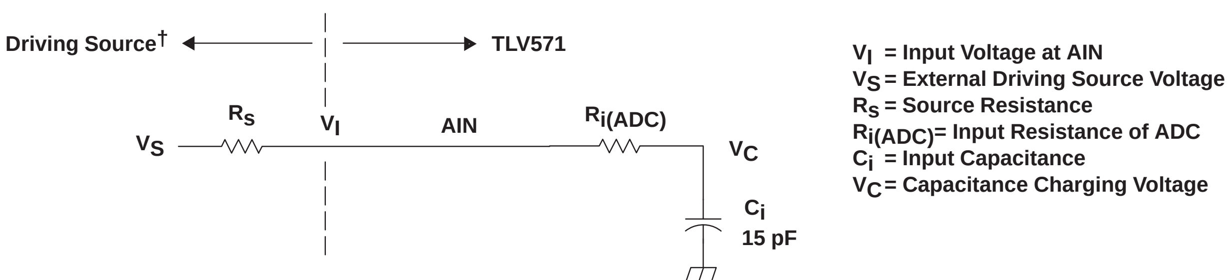


Figure 9. Placement for Decoupling Capacitors

power supply ground layout

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the ADC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.



† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 10. Equivalent Input Circuit Including the Driving Source

simplified analog input analysis

Using the equivalent circuit in Figure 10, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB, t_{ch}(1/2 LSB), can be derived as follows.

The capacitance charging voltage is given by:

$$V_{C(t)} = V_S\left(1 - e^{-t_{ch}/R_tC_i}\right) \tag{1}$$

Where

$R_t = R_s + R_i$

$R_i = R_{i(ADC)}$

t_{ch} = Charge time

The input impedance R_i is 718 Ω at 5 V, and is higher (~ 1.25 kΩ) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$V_C\ (1/2\ LSB) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for cycle time t_c gives:

$$V_S - \left(V_S/512\right) = V_S\left(1 - e^{-t_{ch}/R_tC_i}\right) \tag{3}$$

and time to change to 1/2 LSB (minimum sampling time) is:

$$t_{ch}\ (1/2\ LSB) = R_t \times C_i \times \ln(512)$$

Where

$\ln(512) = 6.238$

Therefore, with the values given, the time for the analog input signal to settle is:

$$t_{ch}\ (1/2\ LSB) = (R_S + 718\ \Omega) \times 15\ pF \times \ln(512) \tag{4}$$

This time must be less than the converter sample time shown in the timing diagrams. Which is 6x SCLK.

$$t_{ch}\ (1/2\ LSB) \le 6x\ 1/f_{(SCLK)} \tag{5}$$

Therefore the maximum SCLK frequency is:

$$Max(f_{(SCLK)}) = 6/t_{ch}\ (1/2\ LSB) = 6/(\ln(512) \times R_t \times C_i) \tag{6}$$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, GND to V_{CC} . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . –0.3 V to AV_{DD} + 0.3 V
Reference input voltage range . . . . AV_{DD} + 0.3 V
Digital input voltage range . . . . –0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . –40°C to 150°C
Operating free-air temperature range, T_A, ... –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	MAX	UNIT
Analog supply voltage, AV_{DD}	2.7	5.5	V
Digital supply voltage, DV_{DD}	2.7	5.5	V

NOTE 1: Abs (AV_{DD} – DV_{DD}) < 0.5 V

analog inputs

	MIN	MAX	UNIT
Analog input voltage, AIN	AGND	VREFP	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2.1	2.4		V
Low level input voltage, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Input CLK frequency	DV_{DD} = 4.5 V to 5.5 V			20	MHz
	DV_{DD} = 2.7 V to 3.3 V			10	MHz
Pulse duration, CLK high, $t_{w(CLKH)}$	DV_{DD} = 4.5 V to 5.5 V, f_{CLK} = 20 MHz	23			ns
	DV_{DD} = 2.7 V to 3.3 V, f_{CLK} = 10 MHz	46			ns
Pulse duration, CLK low, $t_{w(CLKL)}$	DV_{DD} = 4.5 V to 5.5 V, f_{CLK} = 20 MHz	23			ns
	DV_{DD} = 2.7 V to 3.3 V, f_{CLK} = 10 MHz	46			ns
Rise time, I/O and control, CLK, $\overline{CS}$	50 pF output load	4			ns
Fall time, I/O and control, CLK, $\overline{CS}$	50 pF output load	4			

reference specifications

			MIN	NOM	MAX	UNIT
External reference voltage	VREFP	AV_{DD} = 3 V	2		AV_{DD}	V
		AV_{DD} = 5 V	2.5		AV_{DD}	V
	VREFM	AV_{DD} = 3 V	AGND		1	V
		AV_{DD} = 5 V	AGND		2	V
	VREFP – VREFM		2		AV_{DD}–AGND	V

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = DV_{DD}	–1		1	µA
I_{IL}	Low-level input current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = 0 V	–1		1	µA
C_i	Input capacitance			10	15	pF
Logic outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 µA to 0.5 mA	DV_{DD}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA to 0.5 mA			0.4	V
I_{OZ}	High-impedance-state output current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = DV_{DD}			1	µA
I_{OL}	Low-impedance-state output current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = 0 V			–1	µA
C_o	Output capacitance			5		pF
	Internal clock	3 V, AV_{DD} = DV_{DD}	9	10	11	MHz
		5 V, AV_{DD} = DV_{DD}	18	20	22	

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			8		Bits
Accuracy						
	Integral nonlinearity, INL	Best fit		±0.3	±0.5	LSB
	Differential nonlinearity, DNL			±0.3	±0.5	LSB
	Missing codes				0	
E_O	Offset error			±0.15%	±0.3%	FSR
E_G	Gain error			±0.2%	±0.4%	FSR
Analog input						
C_i	Input capacitance	AIN, AV_{DD} = 3 V, AV_{DD} = 5 V		15		pF
		MUX input, AV_{DD} = 3 V, AV_{DD} = 5 V		25		pF
I_{lkg}	Input leakage current	V_{AIN} = 0 to AV_{DD}			±1	µA
Voltage reference input						
r_i	Input resistance		2			kΩ
C_i	Input capacitance			300		pF
Power supply						
	Operating supply current, $I_{DD} + I_{REF}$	AV_{DD} = DV_{DD} = 3 V, f_{CLK} = 10 MHz		4	5.5	mA
		AV_{DD} = DV_{DD} = 5 V, f_{CLK} = 20 MHz		7	8.5	mA
PD	Power dissipation	AV_{DD}+DV_{DD} = 3 V		12	17	mW
		AV_{DD}+DV_{DD} = 5 V		35	43	mW
I_{PD}	Supply current in power-down mode	Software, $I_{DD} + I_{REF}$, AV_{DD} = 3 V		1	8	µA
		Software, $I_{DD} + I_{REF}$, AV_{DD} = 5 V		2	10	µA
		Auto, $I_{DD} + I_{REF}$, AV_{DD} = 3 V		0.5	1	mA
		Auto, $I_{DD} + I_{REF}$, AV_{DD} = 5 V		0.5	1	mA

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted) (continued)

ac specifications, AV_{DD} = DV_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Signal-to-noise ratio, SNR		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	47	49		dB
			f_S = 625 KSPS, AV_{DD} = 3 V	47	49		dB
Signal-to-noise ratio + distortion, SINAD		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	47	49		dB
			f_S = 625 KSPS, AV_{DD} = 3 V	47	49		dB
Total harmonic distortion, THD		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V		–64	–52	dB
			f_S = 625 KSPS, AV_{DD} = 3 V		–62	–52	dB
Effective number of bits, ENOB		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	7.5	7.9		Bits
			f_S = 625 KSPS, AV_{DD} = 3 V	7.5	7.9		Bits
Spurious free dynamic range, SFDR		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V		–65	–51	dB
			f_S = 625 KSPS, AV_{DD} = 3 V		–64	–51	dB
Analog input							
Full-power bandwidth	–1 dB	Full-scale 0 dB input sine wave		12	18		MHz
	–3 dB	Full-scale 0 dB input sine wave			30		MHz
Small-signal bandwidth	–1 dB	–20 dB input sine wave		15	20		MHz
	–3 dB	–20 dB input sine wave			35		MHz
Sampling rate, f_S		AV_{DD} = 4.5 V to 5.5 V		0.0625		1.25	MSPS
		AV_{DD} = 2.7 V to 3.3 V		0.0625		0.625	MSPS

timing requirements, $AV_{DD} = DV_{DD}$ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CLK)}$	Input clock Cycle time	DV_{DD} = 4.5 V to 5.5 V	50			ns
		DV_{DD} = 2.7 V to 3.3 V	100			ns
$t_{(sample)}$	Reset and sampling time			6		SYSCLK Cycles
t_c	Total conversion time			10		SYSCLK Cycles
$t_{wL(EOC)}$	Pulse width, end of conversion, EOC			10		SYSCLK Cycles
$t_{wL(INT)}$	Pulse width, interrupt			1		SYSCLK Cycles
$t_{(STARTOSC)}$	Start-up time, internal oscillator		100			ns
$t_{d(CSH\_CSTARTL)}$	Delay time, $\overline{CS}$ high to $\overline{CSTART}$ low			10		ns
$t_{en(RDL\_DAV)}$	Enable time, data out	DV_{DD} = 5 V at 50 pF		20		ns
		DV_{DD} = 3 V at 50 pF		40		ns
$t_{dis(RDH\_DAV)}$	Disable time, data out	DV_{DD} = 5 V at 50 pF		5		ns
		DV_{DD} = 3 V at 50 pF		10		ns
$t_{su(CSL\_WRL)}$	Setup time, $\overline{CS}$ to $\overline{WR}$		5			ns
$t_{h(WRH\_CSH)}$	Hold time, $\overline{CS}$ to $\overline{WR}$		5			ns
$t_{w(WR)}$	Pulse width, write		1			Clock Period
$t_{w(RD)}$	Pulse width, read		1			Clock Period
$t_{su(DAV\_WRH)}$	Setup time, data valid to $\overline{WR}$		10			ns
$t_{h(WRH\_DAV)}$	Hold time, data valid to $\overline{WR}$		5			ns
$t_{su(CSL\_RDL)}$	Setup time, $\overline{CS}$ to $\overline{RD}$			5		ns
$t_{h(RDH\_CSH)}$	Hold time, $\overline{CS}$ to $\overline{RD}$			5		ns
$t_{h(WRL\_EXTXLKH)}$	Hold time $\overline{WR}$ to clock high		5			ns
$t_{h(RDL\_EXTCLKH)}$	Hold time $\overline{RD}$ to clock high		5			ns
$t_{h(CSTARTL\_EXTCLKH)}$	Hold time $\overline{CSTART}$ to clock high		5			ns
$t_{su(WRH\_EXTCLKH)}$	Setup time $\overline{WR}$ high to clock high		5			ns
$t_{su(RDH\_EXTCLKH)}$	Setup time $\overline{RD}$ high to clock high		5			ns
$t_{su(CSTARTH\_EXTCLKH)}$	Setup time $\overline{CSTART}$ high to clock high		5			ns
$t_{d(EXTCLK\_CSTARTL)}$	Delay time clock low to $\overline{CSTART}$ low		5			ns

NOTE: Specifications subject to change without notice.
Data valid is denoted as DAV.

TYPICAL CHARACTERISTICS

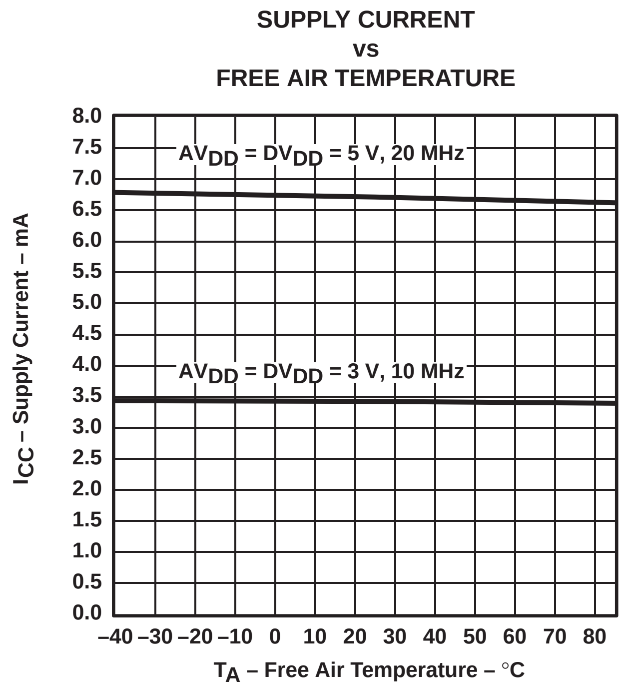


Figure 11

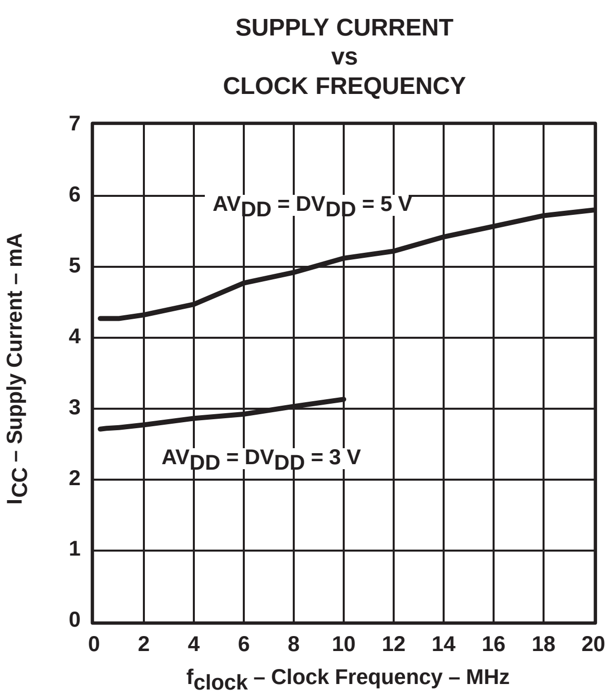


Figure 12

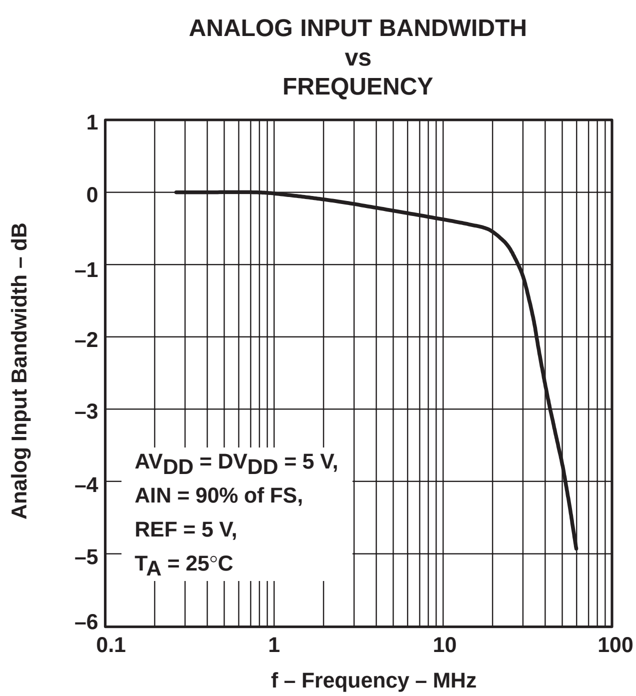


Figure 13

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY
vs
DIGITAL OUTPUT CODE

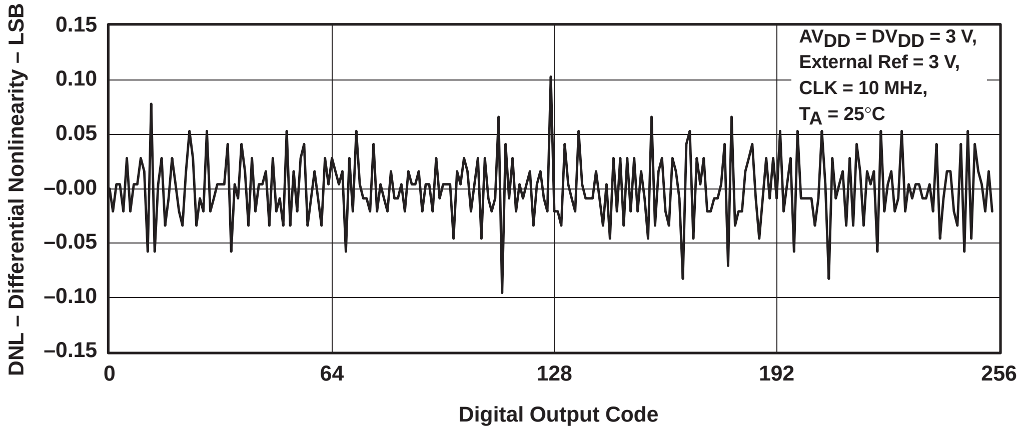


Figure 14

INTEGRAL NONLINEARITY
vs
DIGITAL OUTPUT CODE

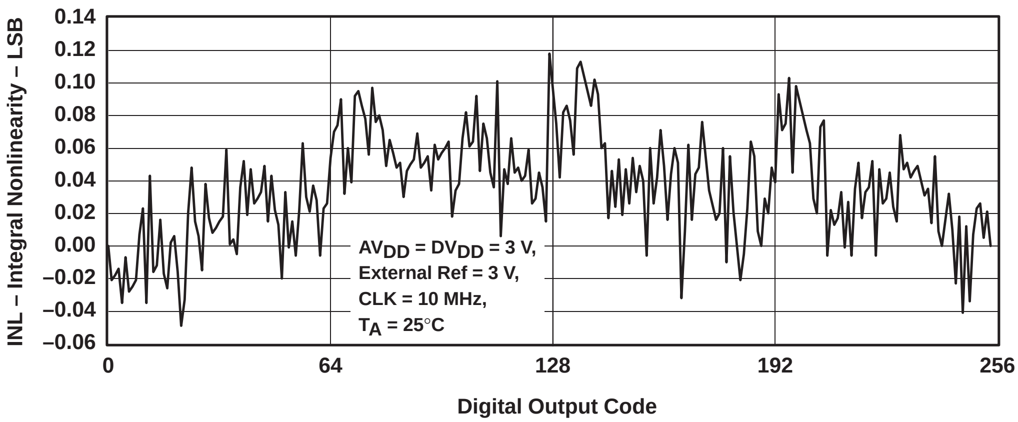


Figure 15

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY vs DIGITAL OUTPUT CODE

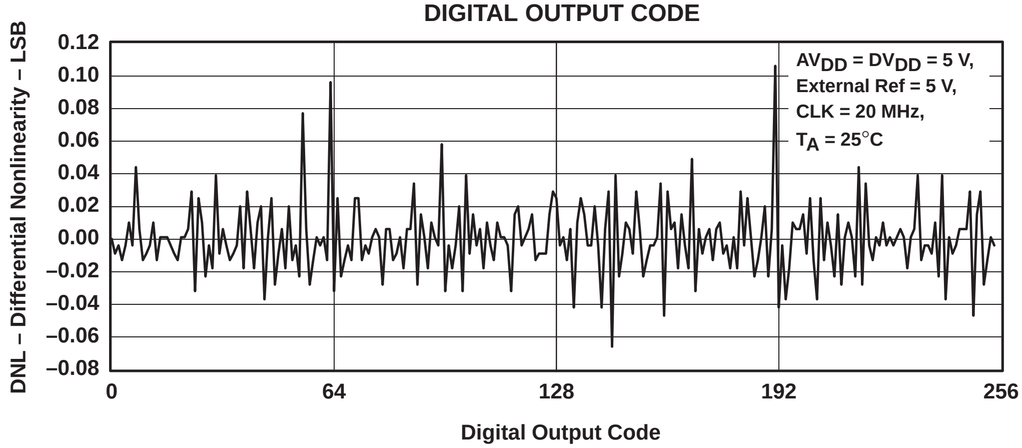


Figure 16

INTEGRAL NONLINEARITY vs DIGITAL OUTPUT CODE

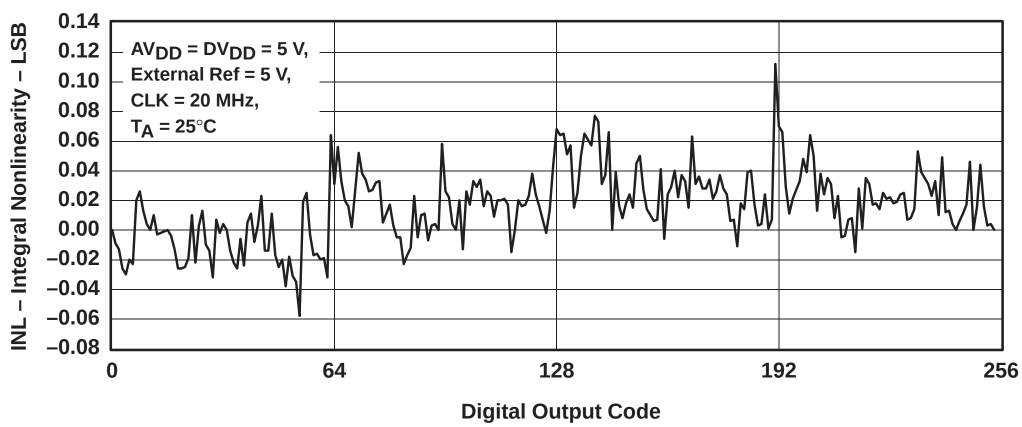


Figure 17

TYPICAL CHARACTERISTICS

**EFFECTIVE NUMBER OF BITS
vs
FREQUENCY**

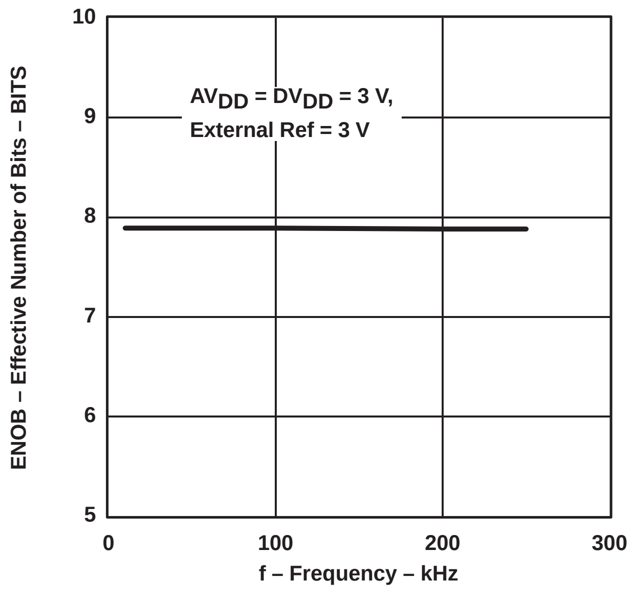


Figure 18

**EFFECTIVE NUMBER OF BITS
vs
FREQUENCY**

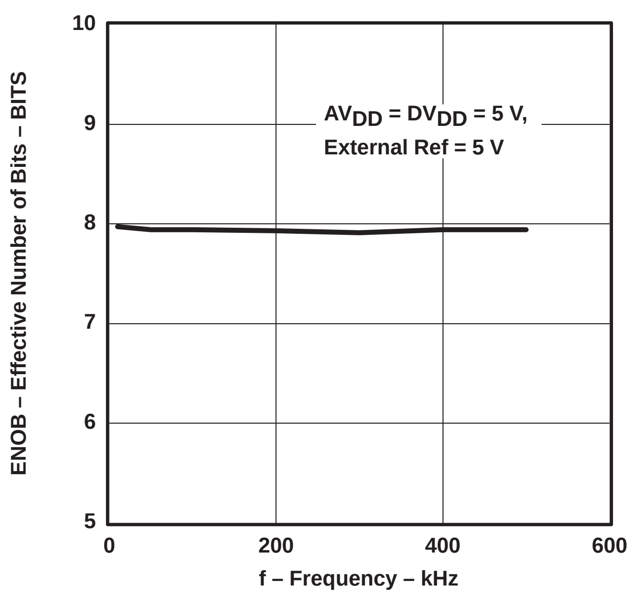


Figure 19

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM
vs
FREQUENCY

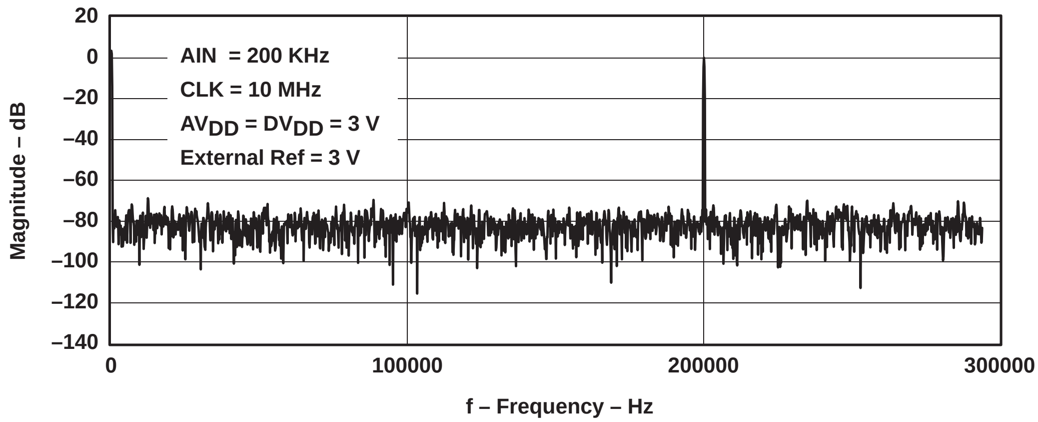


Figure 20

FAST FOURIER TRANSFORM
vs
FREQUENCY

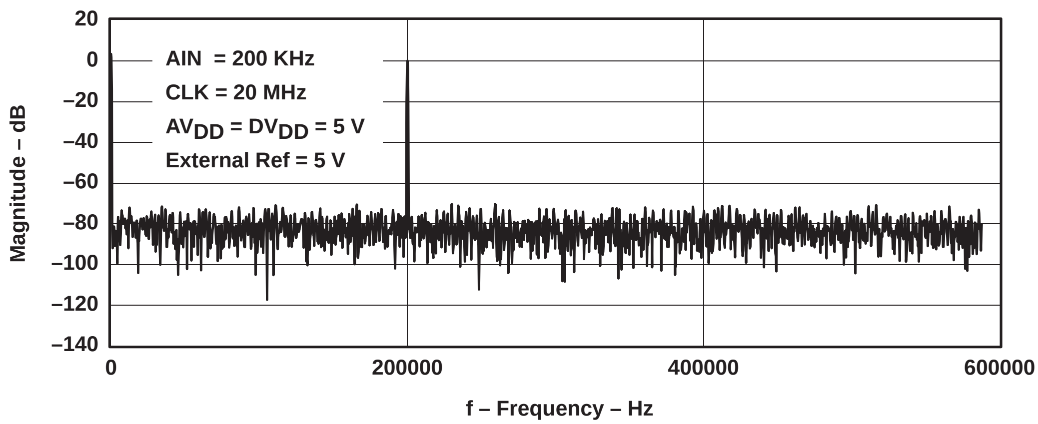


Figure 21

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV571IDW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV571I
TLV571IDW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV571I
TLV571IPW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TY571
TLV571IPW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TY571

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

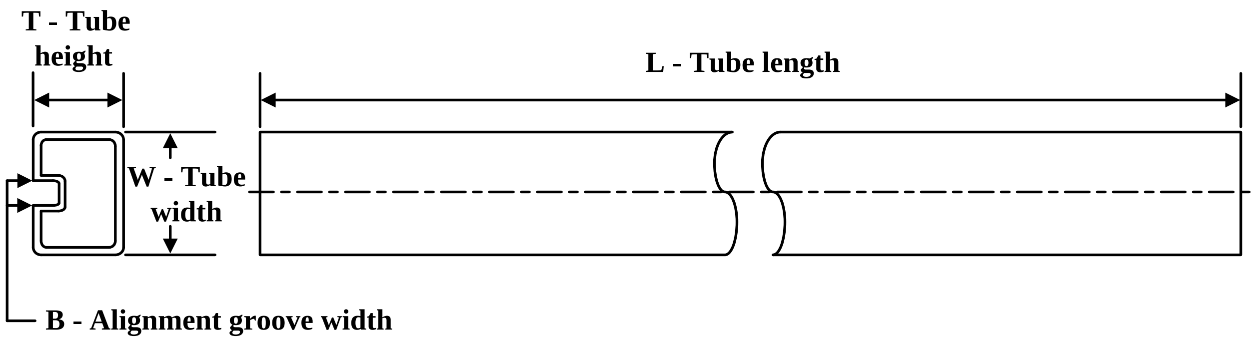
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

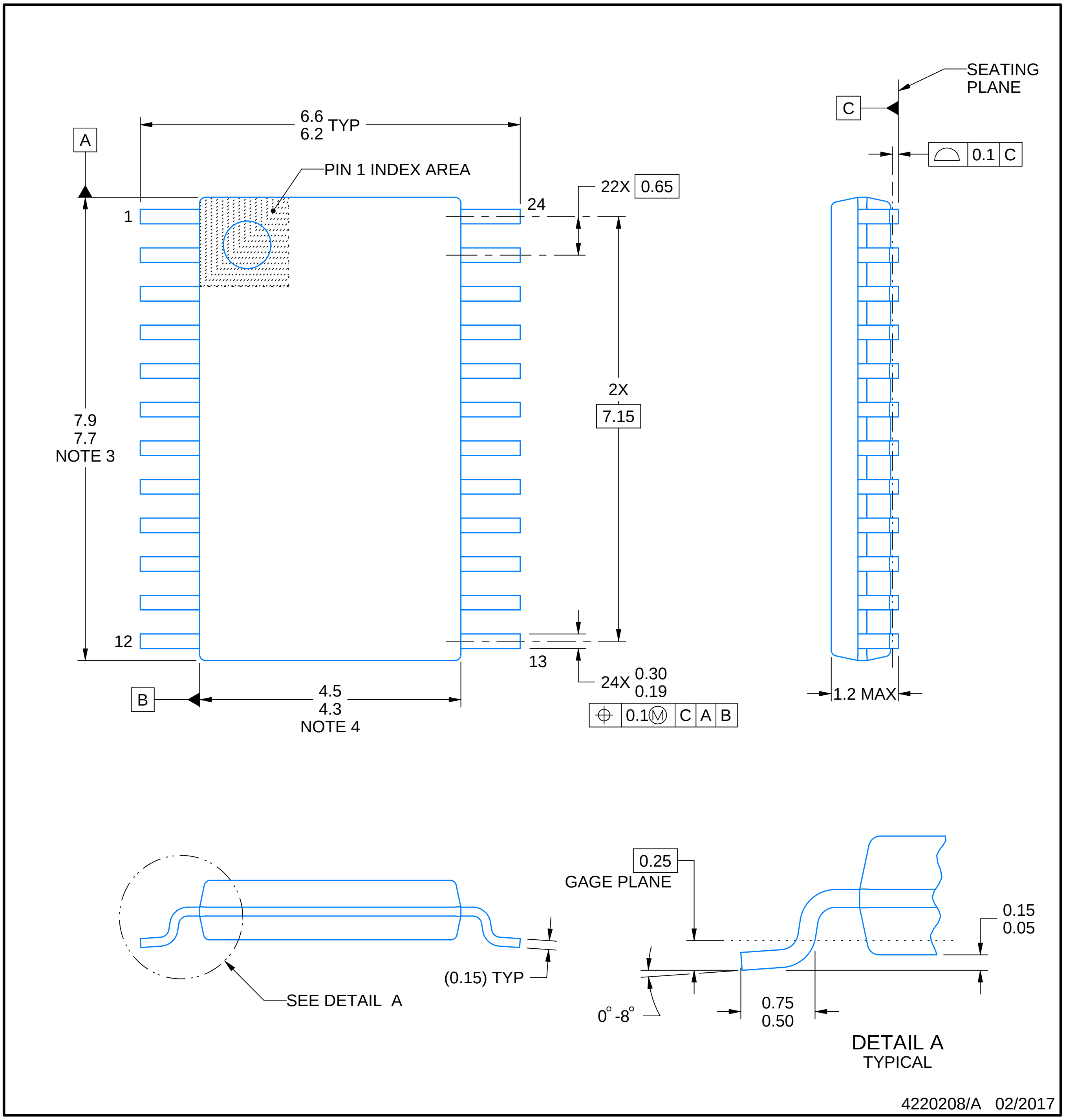
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



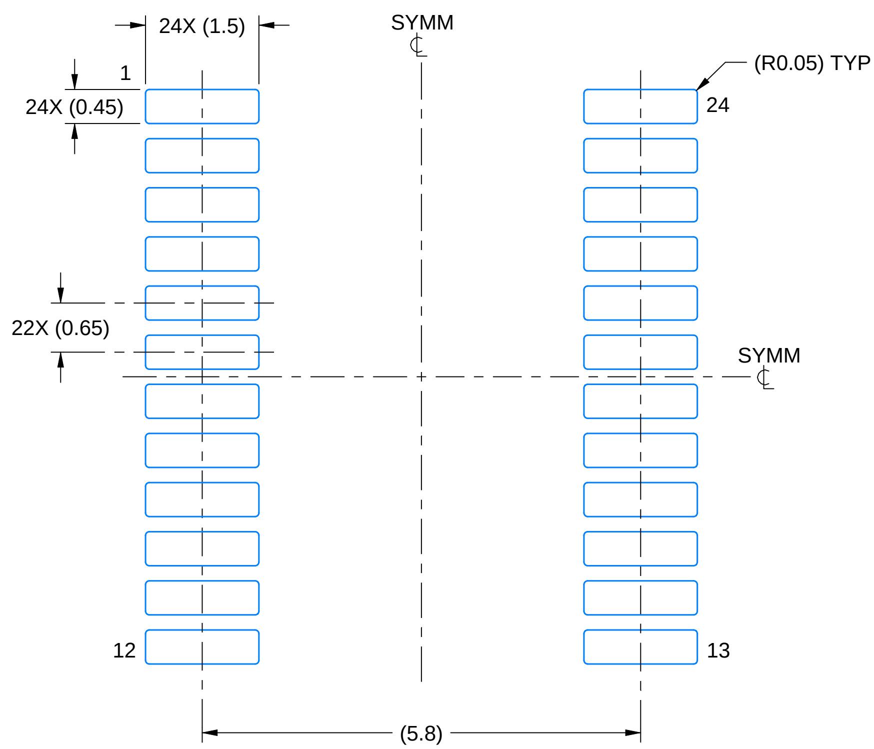
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV571IDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
TLV571IDW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
TLV571IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLV571IPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

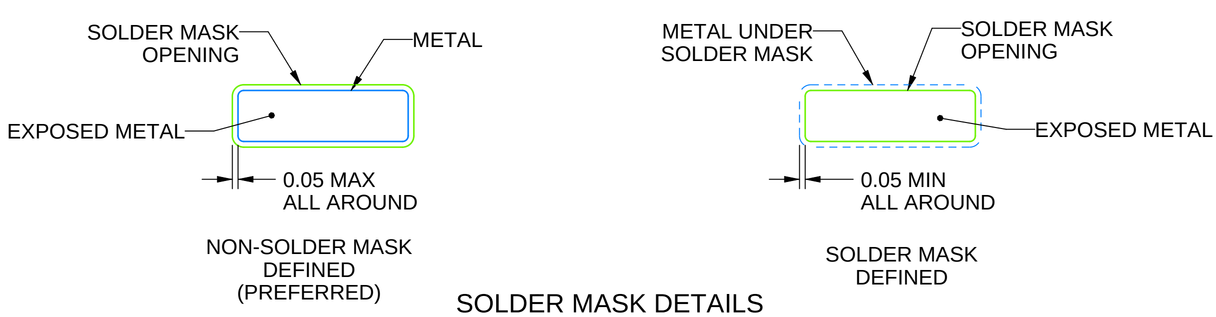


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

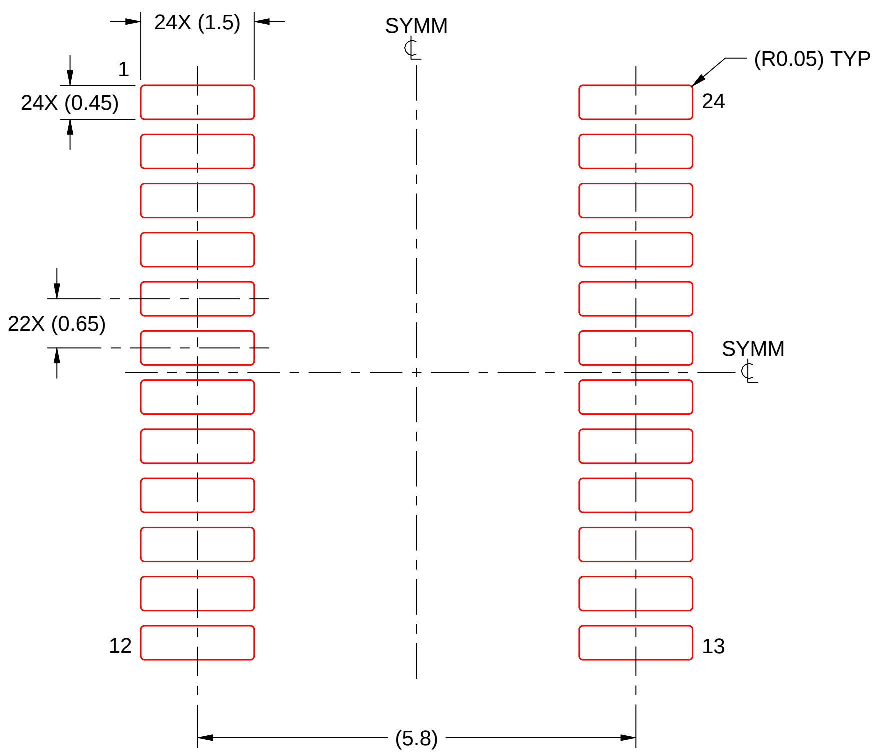


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



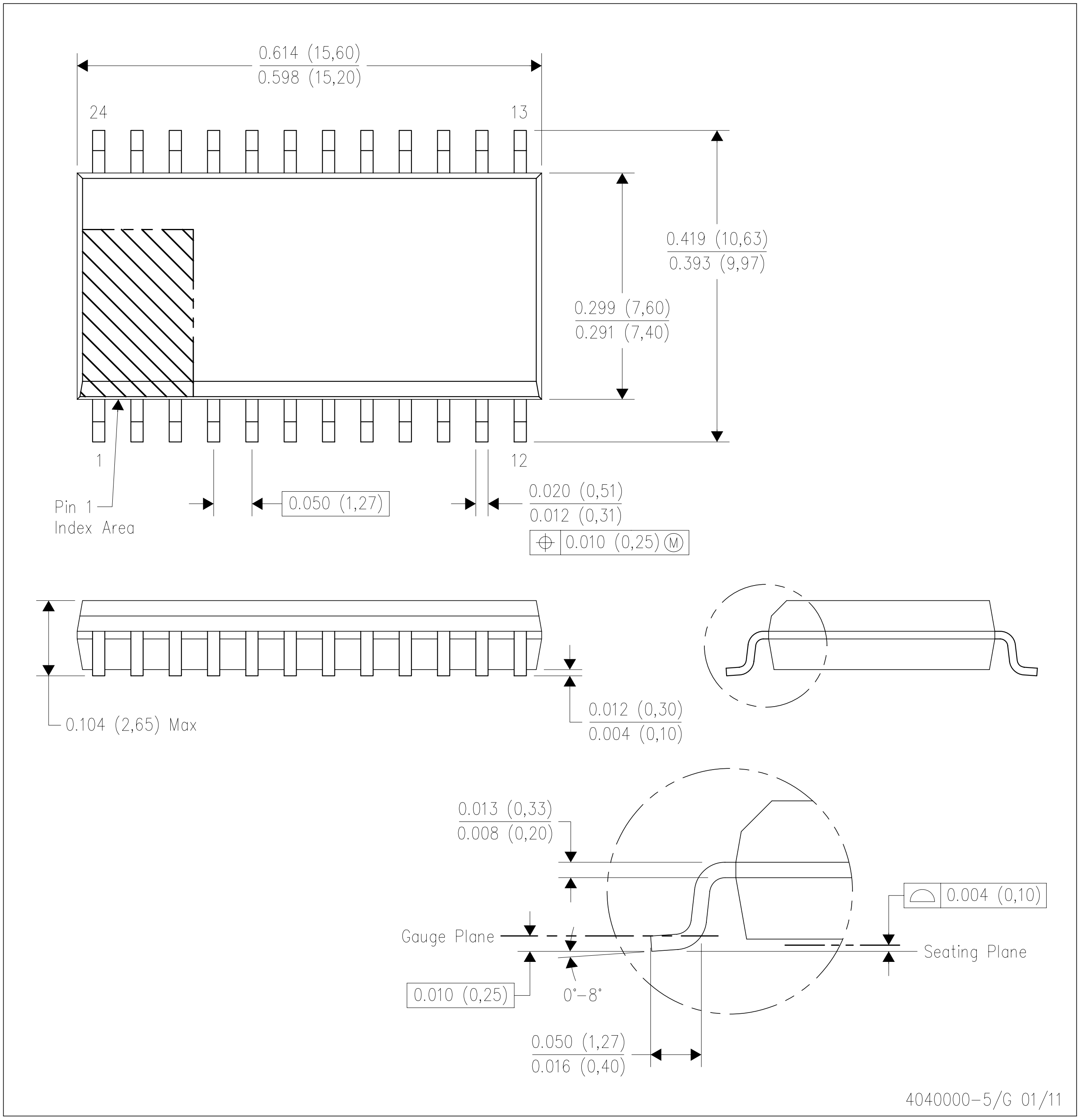
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER