

## 2.7-V TO 5.5-V, LOW POWER, 12-BIT, DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

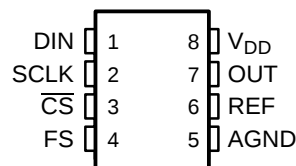
### FEATURES

- 12-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
  - 1  $\mu$ s in Fast Mode
  - 3.5  $\mu$ s in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity . . . <0.5 LSB Typ
- Monotonic Over Temperature

### APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

D OR DGK PACKAGE  
(TOP VIEW)



### DESCRIPTION

The TLV5636 is a 12-bit voltage output DAC with a flexible 4-wire serial interface. The serial interface allows glueless interface to TMS320 and SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The programmable settling time of the DAC allows the designer to optimize speed vs power dissipation. With its on-chip programmable precision voltage reference, the TLV5636 simplifies overall system design.

Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC and 8-pin MSOP package to reduce board space in standard commercial and industrial temperature ranges

### AVAILABLE OPTIONS

| T <sub>A</sub> | PACKAGE   |             |
|----------------|-----------|-------------|
|                | SOIC (D)  | MSOP (DGK)  |
| 0°C to 70°C    | TLV5636CD | TLV5636CDGK |
| -40°C to 85°C  | TLV5636ID | TLV5636IDGK |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

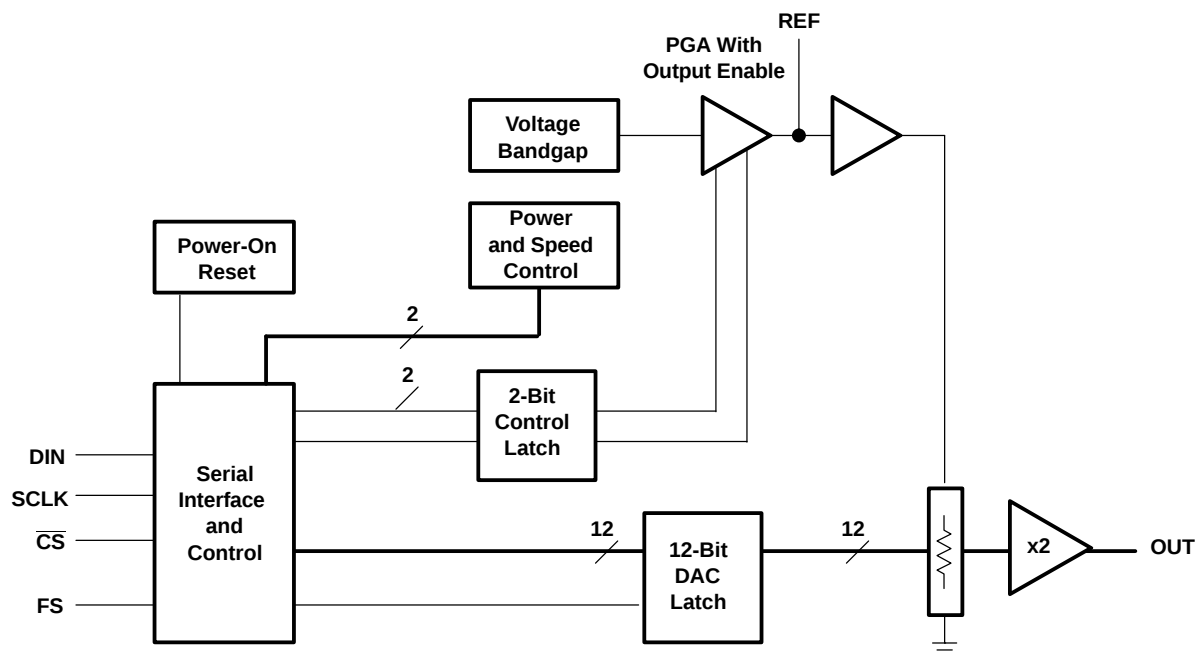
SPI, QSPI are trademarks of Motorola, Inc..

Microwire is a trademark of National Semiconductor Corporation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### FUNCTIONAL BLOCK DIAGRAM



### Terminal Functions

| TERMINAL        |     | I/O/P | DESCRIPTION                                                          |
|-----------------|-----|-------|----------------------------------------------------------------------|
| NAME            | NO. |       |                                                                      |
| AGND            | 5   | P     | Ground                                                               |
| $\overline{CS}$ | 3   | I     | Chip select. Digital input active low, used to enable/disable inputs |
| DIN             | 1   | I     | Digital serial data input                                            |
| FS              | 4   | I     | Frame sync input                                                     |
| OUT             | 7   | O     | DAC A analog voltage output                                          |
| REF             | 6   | I/O   | Analog reference voltage input/output                                |
| SCLK            | 2   | I     | Digital serial clock input                                           |
| $V_{DD}$        | 8   | P     | Positive power supply                                                |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                              |          | UNIT                        |
|--------------------------------------------------------------|----------|-----------------------------|
| Supply voltage ( $V_{DD}$ to AGND)                           |          | 7 V                         |
| Reference input voltage                                      |          | - 0.3 V to $V_{DD} + 0.3$ V |
| Digital input voltage range                                  |          | - 0.3 V to $V_{DD} + 0.3$ V |
| Operating free-air temperature range, $T_A$                  | TLV5636C | 0°C to 70°C                 |
|                                                              | TLV5636I | -40°C to 85°C               |
| Storage temperature range, $T_{stg}$                         |          | -65°C to 150°C              |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |          | 260°C                       |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

|                                              |                               | MIN  | NOM   | MAX            | UNIT       |
|----------------------------------------------|-------------------------------|------|-------|----------------|------------|
| Supply voltage, $V_{DD}$                     | $V_{DD} = 5$ V                | 4.5  | 5     | 5.5            | V          |
|                                              | $V_{DD} = 3$ V                | 2.7  | 3     | 3.3            | V          |
| Power on Reset, POR                          |                               | 0.55 |       | 2              | V          |
| High-level digital input voltage, $V_{IH}$   | $DV_{DD} = 2.7$ V             | 2    |       |                | V          |
|                                              | $DV_{DD} = 5.5$ V             | 2.4  |       |                |            |
| Low-level digital input voltage, $V_{IL}$    | $DV_{DD} = 2.7$ V             |      |       | 0.6            | V          |
|                                              | $DV_{DD} = 5.5$ V             |      |       | 1              |            |
| Reference voltage, $V_{ref}$ to REF terminal | $V_{DD} = 5$ V <sup>(1)</sup> | AGND | 2.048 | $V_{DD} - 1.5$ | V          |
|                                              | $V_{DD} = 3$ V <sup>(1)</sup> | AGND | 1.024 | $V_{DD} - 1.5$ | V          |
| Load resistance, $R_L$                       |                               | 2    |       |                | k $\Omega$ |
| Load capacitance, $C_L$                      |                               |      |       | 100            | pF         |
| Clock frequency, $f_{CLK}$                   |                               |      |       | 20             | MHz        |
| Operating free-air temperature, $T_A$        | TLV5636C                      | 0    |       | 70             | °C         |
|                                              | TLV5636I                      | -40  |       | 85             |            |

- (1) Due to the x2 output buffer, a reference input voltage . ( $V_{DD} - 0.4$  V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

| POWER SUPPLY    |                              |                                                                         |      |     |      |     |      |
|-----------------|------------------------------|-------------------------------------------------------------------------|------|-----|------|-----|------|
| PARAMETER       |                              | TEST CONDITIONS                                                         |      | MIN | TYP  | MAX | UNIT |
| I <sub>DD</sub> | Power supply current         | No load,<br>All inputs = AGND or V <sub>DD</sub> ,<br>DAC latch = 0x800 | Fast |     | 2.3  | 3.3 | mA   |
|                 |                              |                                                                         | Slow |     | 1.5  | 1.9 |      |
|                 | Power-down supply current    | See <a href="#">Figure 8</a>                                            |      |     | 0.01 | 10  | μA   |
| PSRR            | Power supply rejection ratio | Zero scale <sup>(1)</sup>                                               |      |     | -65  |     | dB   |
|                 |                              | Full Scale <sup>(2)</sup>                                               |      |     | -65  |     |      |

- (1) Power supply rejection ratio at zero scale is measured by varying  $V_{DD}$  and is given by:  
 $PSRR = 20 \log [(E_{ZS}(V_{DDmax}) - E_{ZS}(V_{DDmin}))/V_{DDmax}]$   
(2) Power supply rejection ratio at full scale is measured by varying  $V_{DD}$  and is given by:  
 $PSRR = 20 \log [(E_G(V_{DDmax}) - E_G(V_{DDmin}))/V_{DDmax}]$

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

| STATIC DAC SPECIFICATIONS |                                               |                         |  |      |     |      |                 |
|---------------------------|-----------------------------------------------|-------------------------|--|------|-----|------|-----------------|
| PARAMETER                 |                                               | TEST CONDITIONS         |  | MIN  | TYP | MAX  | UNIT            |
| Resolution                |                                               |                         |  | 12   |     |      | Bits            |
| INL                       | Integral nonlinearity                         | See note <sup>(1)</sup> |  | ±2   |     | ±4   | LSB             |
| DNL                       | Differential nonlinearity                     | See note <sup>(2)</sup> |  | ±0.5 |     | ±1   | LSB             |
| E <sub>ZS</sub>           | Zero-scale error (offset error at zero scale) | See note <sup>(3)</sup> |  |      |     | ±20  | mV              |
| E <sub>ZS</sub> TC        | Zero-scale-error temperature coefficient      | See note <sup>(4)</sup> |  | 10   |     |      | μV/°C           |
| E <sub>G</sub>            | Gain error                                    | See note <sup>(5)</sup> |  |      |     | ±0.6 | % of FS voltage |
| E <sub>G</sub> TC         | Gain error temperature coefficient            | See note <sup>(6)</sup> |  | 10   |     |      | ppm/°C          |

- (1) The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 4095.
- (2) The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 4095.
- (3) Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
- (4) Zero-scale-error temperature coefficient is given by:  $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$ .
- (5) Gain error is the deviation from the ideal output ( $2V_{ref} - 1$  LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
- (6) Gain error temperature coefficient is given by:  $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$ .

| OUTPUT SPECIFICATIONS |                                 |                                                          |  |     |     |                       |                 |
|-----------------------|---------------------------------|----------------------------------------------------------|--|-----|-----|-----------------------|-----------------|
| PARAMETER             |                                 | TEST CONDITIONS                                          |  | MIN | TYP | MAX                   | UNIT            |
| V <sub>O</sub>        | Voltage output range            | R <sub>L</sub> = 10 kΩ                                   |  | 0   |     | V <sub>DD</sub> - 0.4 | V               |
|                       | Output load regulation accuracy | V <sub>O</sub> = 4.096 V, 2.048 V, R <sub>L</sub> = 2 kΩ |  |     |     | ±0.25                 | % of FS voltage |

### REFERENCE PIN CONFIGURED AS OUTPUT (REF)

| PARAMETER                |                              | TEST CONDITIONS          |  | MIN   | TYP   | MAX   | UNIT |
|--------------------------|------------------------------|--------------------------|--|-------|-------|-------|------|
| V <sub>ref(OUTL)</sub>   | Low reference voltage        |                          |  | 1.003 | 1.024 | 1.045 | V    |
| V <sub>ref(OUTH)</sub>   | High reference voltage       | V <sub>DD</sub> > 4.75 V |  | 2.027 | 2.048 | 2.068 | V    |
| I <sub>ref(source)</sub> | Output source current        |                          |  |       |       | 1     | mA   |
| I <sub>ref(sink)</sub>   | Output sink current          |                          |  | -1    |       |       | mA   |
| Load capacitance         |                              |                          |  |       |       | 100   | pF   |
| PSRR                     | Power supply rejection ratio |                          |  | -65   |       |       | dB   |

### REFERENCE INPUT CONFIGURED AS INPUT (REF)

| PARAMETER                 |                   | TEST CONDITIONS                                              |      | MIN | TYP | MAX                   | UNIT |
|---------------------------|-------------------|--------------------------------------------------------------|------|-----|-----|-----------------------|------|
| V <sub>I</sub>            | Input voltage     |                                                              |      | 0   |     | V <sub>DD</sub> - 1.5 | V    |
| R <sub>i</sub>            | Input resistance  |                                                              |      | 10  |     |                       | kΩ   |
| C <sub>i</sub>            | Input capacitance |                                                              |      | 5   |     |                       | pF   |
| Reference input bandwidth |                   | REF = 0.2 V <sub>pp</sub> + 1.024 V dc                       | Fast | 1.3 |     |                       | MHz  |
|                           |                   |                                                              | Slow | 525 |     |                       |      |
| Reference feed through    |                   | REF = 1 V <sub>pp</sub> at 1 kHz + 1.024 V dc <sup>(1)</sup> |      | -80 |     |                       | dB   |

- (1) Reference feedthrough is measured at the DAC output with an input code = 0x000.

| DIGITAL INPUT   |                                  |                                  |     |     |     |      |
|-----------------|----------------------------------|----------------------------------|-----|-----|-----|------|
| PARAMETER       |                                  | TEST CONDITIONS                  | MIN | TYP | MAX | UNIT |
| I <sub>IH</sub> | High-level digital input current | V <sub>I</sub> = V <sub>DD</sub> |     |     | 1   | μA   |
| I <sub>IL</sub> | Low-level digital input current  | V <sub>I</sub> = 0 V             | -1  |     |     | μA   |
| C <sub>i</sub>  | Input capacitance                |                                  |     | 8   |     | pF   |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

| ANALOG OUTPUT DYNAMIC PERFORMANCE |                                    |                                                                                                               |                           |      |     |     |      |      |
|-----------------------------------|------------------------------------|---------------------------------------------------------------------------------------------------------------|---------------------------|------|-----|-----|------|------|
| PARAMETER                         |                                    | TEST CONDITIONS                                                                                               |                           |      | MIN | TYP | MAX  | UNIT |
| t <sub>s(FS)</sub>                | Output settling time (full scale)  | R <sub>L</sub> = 10 kΩ,<br>see note <sup>(1)</sup>                                                            | C <sub>L</sub> = 100 pF,  | Fast | 1   | 3   | μs   |      |
|                                   |                                    |                                                                                                               |                           | Slow | 3.5 | 7   |      |      |
| t <sub>s(CC)</sub>                | Output settling time, code to code | R <sub>L</sub> = 10 kΩ,<br>see note <sup>(2)</sup>                                                            | C <sub>L</sub> = 100 pF,  | Fast | 0.5 | 1.5 | μs   |      |
|                                   |                                    |                                                                                                               |                           | Slow | 1   | 2   |      |      |
| SR                                | Slew rate                          | R <sub>L</sub> = 10 kΩ,<br>see note <sup>(3)</sup>                                                            | C <sub>L</sub> = 100 pF,  | Fast | 8   |     | V/μs |      |
|                                   |                                    |                                                                                                               |                           | Slow | 1.5 |     |      |      |
| Glitch energy                     |                                    | DIN = 0 to 1,<br>CS = V <sub>DD</sub>                                                                         | f <sub>out</sub> = 1 kHz, |      | 5   |     | nV-s |      |
| SNR                               | Signal-to-noise ratio              | f <sub>s</sub> = 480 kSPS,    f <sub>out</sub> = 1 kHz,<br>R <sub>L</sub> = 10 kΩ,    C <sub>L</sub> = 100 pF |                           |      | 71  | 75  | dB   |      |
| S/(N+D)                           | Signal-to-noise + distortion       |                                                                                                               |                           |      | 59  | 66  |      |      |
| THD                               | Total harmonic distortion          |                                                                                                               |                           |      | -67 | -59 |      |      |
| Spurious free dynamic range       |                                    |                                                                                                               |                           |      | 59  | 69  |      |      |

- (1) Settling time is the time for the output signal to remain within +0.5 LSB of the final measured value for a digital input code change of 0x20 to 0xFDF and 0xFDF to 0x020 respectively. Assured by design; not tested.
- (2) Settling time is the time for the output signal to remain within +0.5 LSB of the final measured value for a digital input code change of one count. Assured by design; not tested.
- (3) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

## TIMING REQUIREMENTS

| DIGITAL INPUTS           |                                                                                                                                                                                                                                                                                       |     |     |     |      |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
|                          |                                                                                                                                                                                                                                                                                       | MIN | NOM | MAX | UNIT |
| t <sub>SU</sub> (CS-FS)  | Setup time, $\overline{\text{CS}}$ low before FS falling edge                                                                                                                                                                                                                         | 10  |     |     | ns   |
| t <sub>SU</sub> (FS-CK)  | Setup time, FS low before first negative SCLK edge                                                                                                                                                                                                                                    | 8   |     |     | ns   |
| t <sub>SU</sub> (C16-FS) | Setup time, 16 <sup>th</sup> negative edge after FS low on which bit D0 is sampled before rising edge of FS.                                                                                                                                                                          | 10  |     |     | ns   |
| t <sub>SU</sub> (C16-CS) | Setup time, 16 <sup>th</sup> positive SCLK edge (first positive after D0 is sampled) before $\overline{\text{CS}}$ rising edge. If FS is used instead of 16 <sup>th</sup> positive edge to update DAC, then setup time between FS rising edge and $\overline{\text{CS}}$ rising edge. | 10  |     |     | ns   |
| t <sub>WH</sub>          | SCLK pulse duration high                                                                                                                                                                                                                                                              | 25  |     |     | ns   |
| t <sub>WL</sub>          | SCLK pulse duration low                                                                                                                                                                                                                                                               | 25  |     |     | ns   |
| t <sub>SU</sub> (D)      | Setup time, data ready before SCLK falling edge                                                                                                                                                                                                                                       | 8   |     |     | ns   |
| t <sub>H</sub> (D)       | Hold time, data held valid after SCLK falling edge                                                                                                                                                                                                                                    | 5   |     |     | ns   |
| t <sub>WH</sub> (FS)     | FS duration high                                                                                                                                                                                                                                                                      | 25  |     |     | ns   |



## TYPICAL CHARACTERISTICS

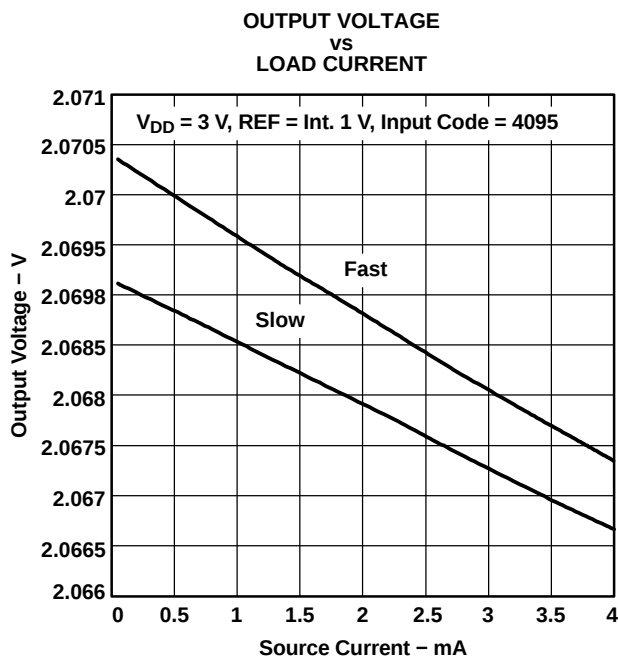


Figure 2.

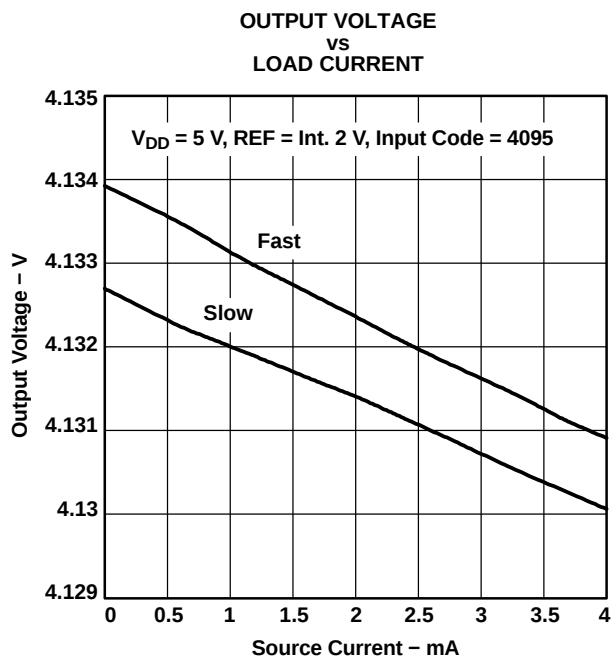


Figure 3.

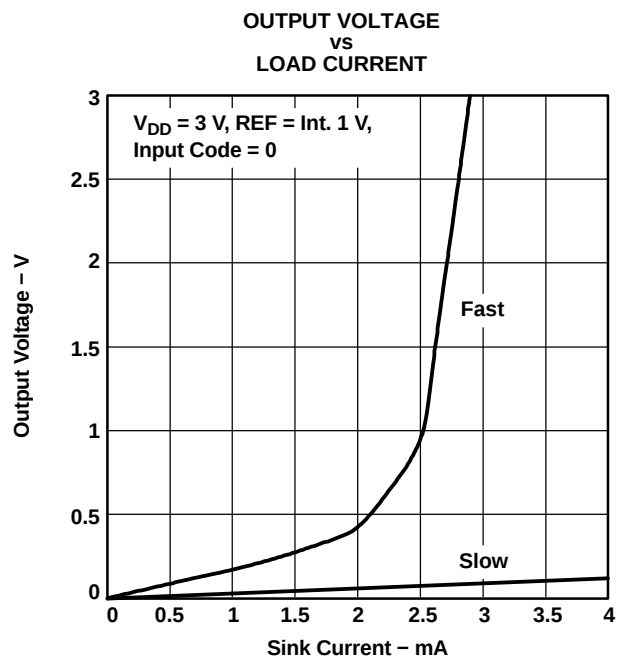


Figure 4.

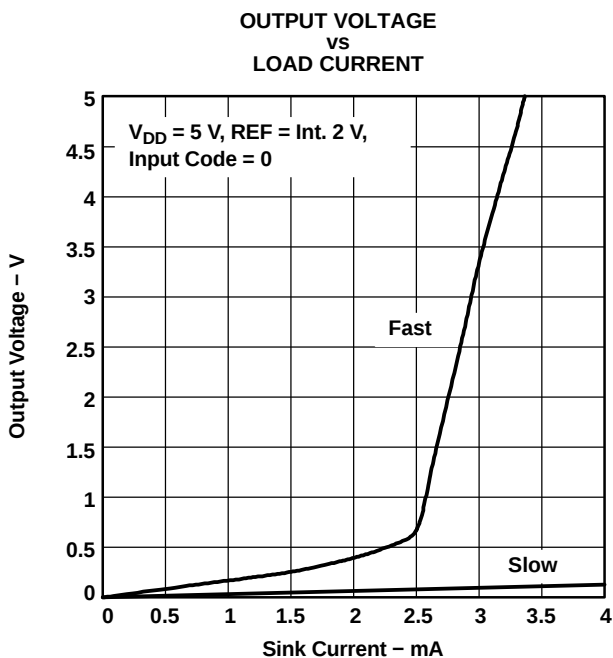


Figure 5.

## TYPICAL CHARACTERISTICS (continued)

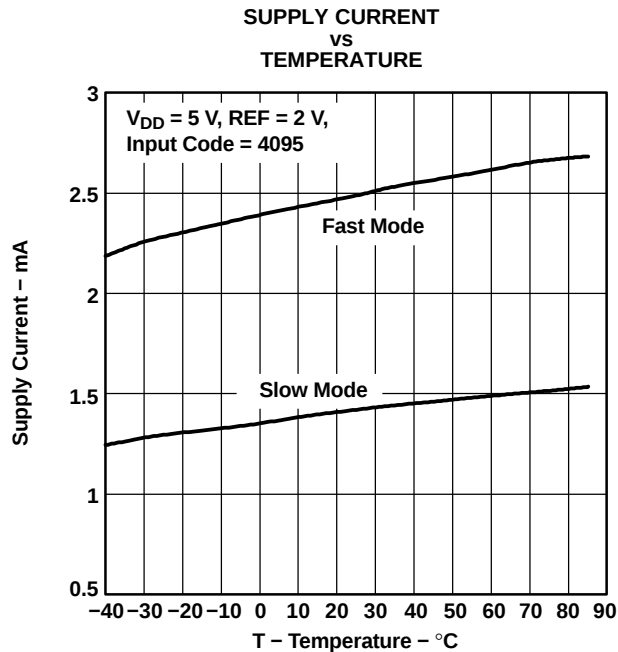


Figure 6.

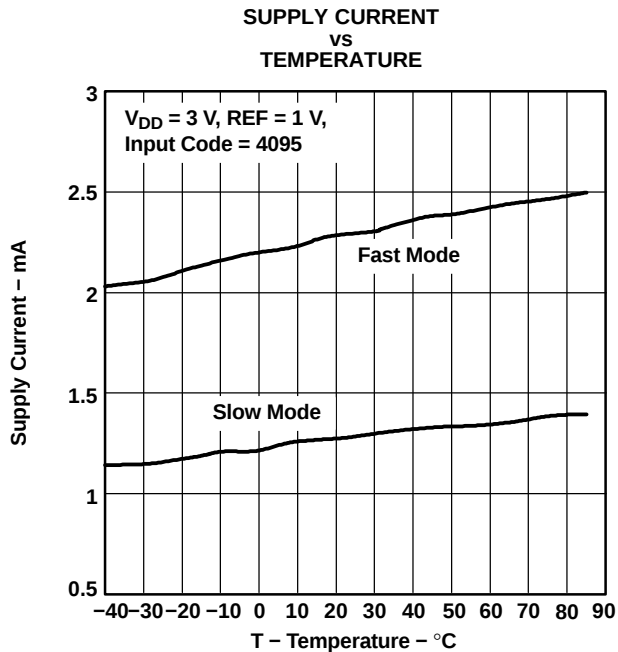


Figure 7.

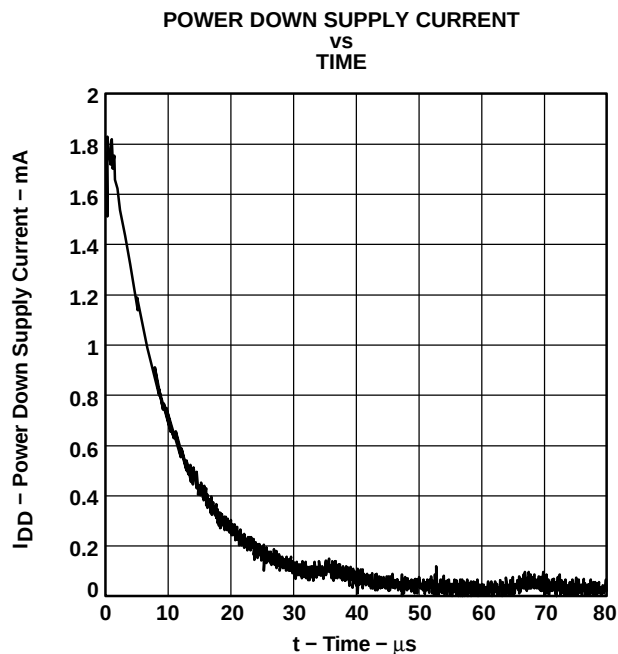


Figure 8.

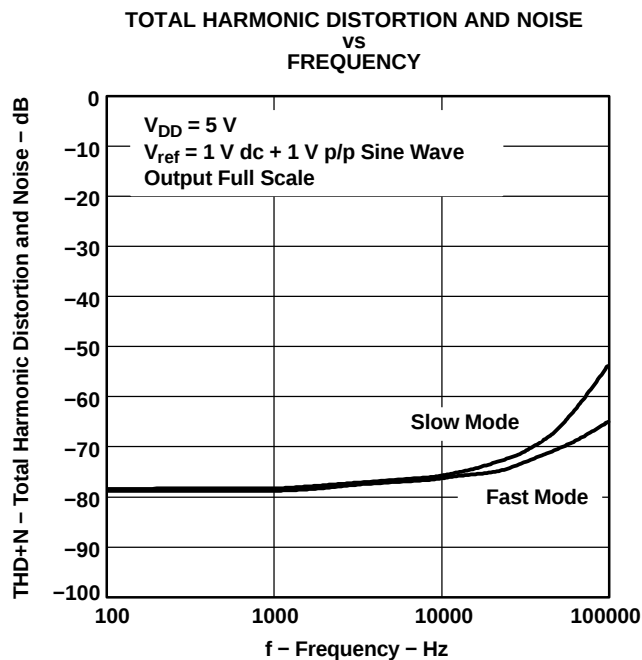


Figure 9.

## TYPICAL CHARACTERISTICS (continued)

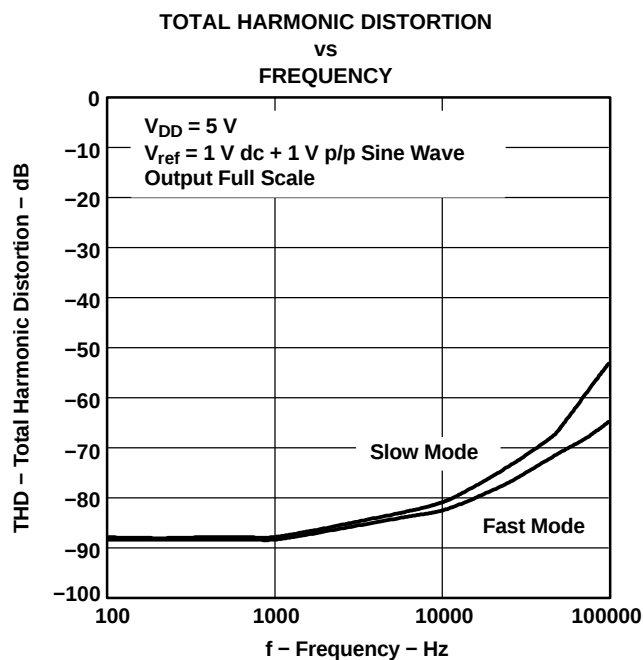


Figure 10.

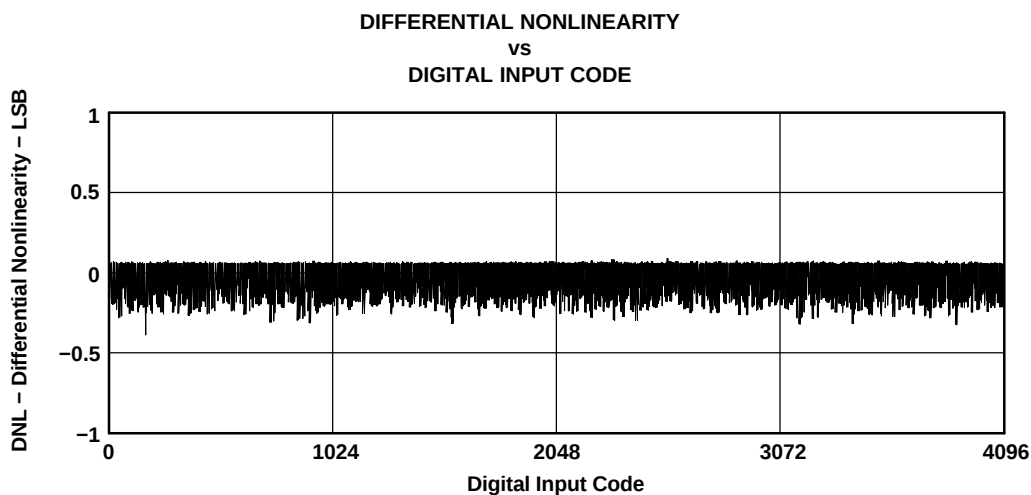
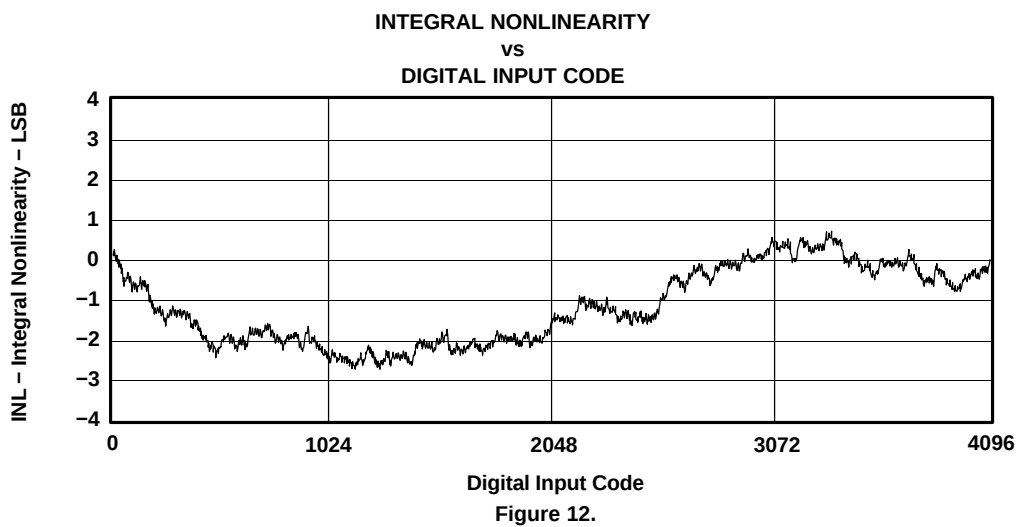


Figure 11.

## TYPICAL CHARACTERISTICS (continued)



## APPLICATION INFORMATION

### GENERAL FUNCTION

The TLV5636 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) for each channel is given by:

$$2 \text{ REF } \frac{\text{CODE}}{2^n} [\text{V}]$$

where REF is the reference voltage and CODE is the digital input value within the range of  $0_{10}$  to  $2^{n-1}$ , where  $n = 12$  (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

### SERIAL INTERFACE

The device has to be enabled with  $\overline{\text{CS}}$  set to low. A falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on high-low transitions of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5636 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four-wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). Figure 13 shows an example with two TLV5636s connected directly to a TMS320 DSP.

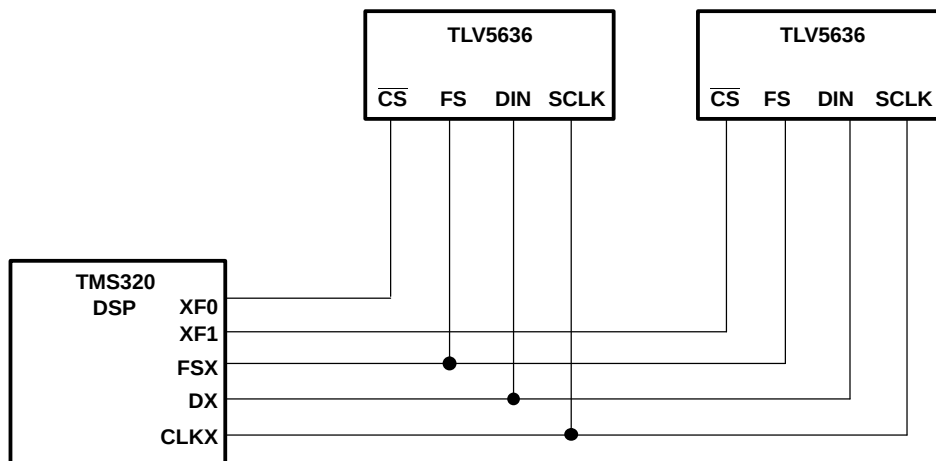


Figure 13. TMS320 Interface

If there is no need to have more than one device on the serial bus, then  $\overline{\text{CS}}$  can be tied low. Figure 14 shows an example of how to connect the TLV5636 to TMS320, SPI™ or Microwire™ using only three pins.

## APPLICATION INFORMATION (continued)

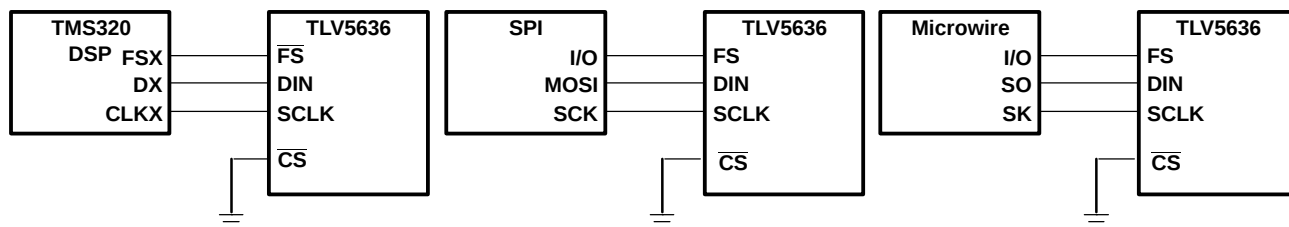


Figure 14. Three Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5636. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

### SERIAL CLOCK AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{\text{sclmax}} = \frac{1}{t_{\text{whmin}} + t_{\text{wlmin}}} = 20 \text{ MHz} \quad (1)$$

The maximum update rate is:

$$f_{\text{updatemax}} = \frac{1}{16(t_{\text{whmin}} + t_{\text{wlmin}})} = 1.25 \text{ MHz} \quad (2)$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5636 has to be considered, too.

### DATA FORMAT

The 16-bit data word for the TLV5636 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

| D15 | D14 | D13 | D12 | D11          | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|--------------|-----|----|----|----|----|----|----|----|----|----|----|
| R1  | SPD | PWR | R0  | 12 Data bits |     |    |    |    |    |    |    |    |    |    |    |

SPD : Speed control bit                      1 = fast mode                      0 = slow mode  
PWR : Power control bit                      1 = power down                      0 = normal operation

The following table lists the possible combination of the register select bits:

#### Register Select Bits

| R1 | R0 | REGISTER                       |
|----|----|--------------------------------|
| 0  | 0  | Write data to DAC              |
| 0  | 1  | Reserved                       |
| 1  | 0  | Reserved                       |
| 1  | 1  | Write data to control register |

The meaning of the 12 data bits depends on the selected register. For the DAC register, the 12 data bits determine the new DAC output value:

**Data Bits: DAC**

| D11           | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|-----|----|----|----|----|----|----|----|----|----|----|
| New DAC value |     |    |    |    |    |    |    |    |    |    |    |

If the control register is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

**Data Bits: CONTROL**

| D11              | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1   | D0   |
|------------------|-----|----|----|----|----|----|----|----|----|------|------|
| X <sup>(1)</sup> | X   | X  | X  | X  | X  | X  | X  | X  | X  | REF1 | REF0 |

(1) X = don't care

REF1 and REF0 determine the reference source. If internal reference is selected, REF1 and REF0 determine the reference voltage.

**Reference Bits**

| REF1 | REF0 | REFERENCE |
|------|------|-----------|
| 0    | 0    | External  |
| 0    | 1    | 1.024 V   |
| 1    | 0    | 2.048 V   |
| 1    | 1    | External  |

**CAUTION:**

**If external reference voltage is applied to the REF pin, external reference MUST be selected.**

**EXAMPLE:**

- Set DAC output, select fast mode, select internal reference at 2.048 V:

**Set reference voltage to 2.048 V (CONTROL register):**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1   | 1   | 0   | 1   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  |

**Write new DAC value and update DAC output:**

| D15 | D14 | D13 | D12 | D11                  | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|----------------------|-----|----|----|----|----|----|----|----|----|----|----|
| 0   | 1   | 0   | 0   | New DAC output value |     |    |    |    |    |    |    |    |    |    |    |

The DAC output is updated on the rising clock edge after D0 is sampled.

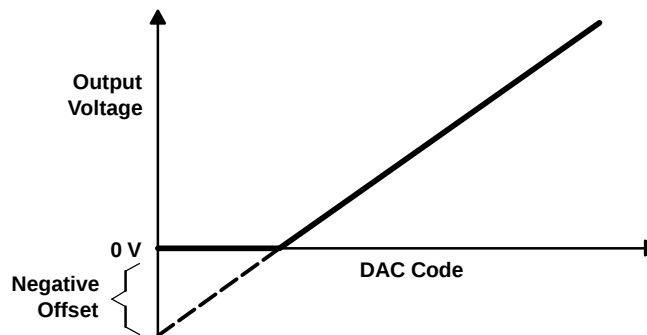
To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

## LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE END SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in [Figure 15](#).



**Figure 15. Effect of Negative Offset (Single Supply)**

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

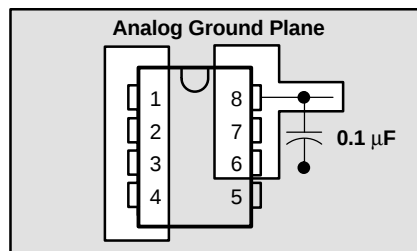
For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

## POWER-SUPPLY BYPASSING AND GROUND MANAGEMENT

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- $\mu$ F ceramic-capacitor bypass should be connected between  $V_{DD}$  and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

[Figure 16](#) shows the ground plane layout and bypassing technique.



**Figure 16. Power-Supply Bypassing**

## **DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY**

### **Integral Nonlinearity (INL)**

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

### **Differential Nonlinearity (DNL)**

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

### **Zero-Scale Error ( $E_{zs}$ )**

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

### **Gain Error ( $E_G$ )**

Gain error is the error in slope of the DAC transfer function.

### **Total Harmonic Distortion (THD)**

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

### **Signal-To-Noise Ratio + Distortion (S/N+D)**

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

### **Spurious Free Dynamic Range (SFDR)**

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TLV5636CD</a>    | Active        | Production           | SOIC (D)   8    | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 5636C               |
| TLV5636CD.A                  | Active        | Production           | SOIC (D)   8    | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 5636C               |
| <a href="#">TLV5636CDGK</a>  | Active        | Production           | VSSOP (DGK)   8 | 80   TUBE             | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | 0 to 70      | AJF                 |
| TLV5636CDGK.A                | Active        | Production           | VSSOP (DGK)   8 | 80   TUBE             | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJF                 |
| <a href="#">TLV5636CDGKR</a> | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | 0 to 70      | AJF                 |
| TLV5636CDGKR.A               | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJF                 |
| <a href="#">TLV5636ID</a>    | Active        | Production           | SOIC (D)   8    | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 5636I               |
| TLV5636ID.A                  | Active        | Production           | SOIC (D)   8    | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 5636I               |
| <a href="#">TLV5636IDGK</a>  | Active        | Production           | VSSOP (DGK)   8 | 80   TUBE             | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJG                 |
| TLV5636IDGK.A                | Active        | Production           | VSSOP (DGK)   8 | 80   TUBE             | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJG                 |
| <a href="#">TLV5636IDGKR</a> | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJG                 |
| TLV5636IDGKR.A               | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 85    | AJG                 |
| <a href="#">TLV5636IDR</a>   | Active        | Production           | SOIC (D)   8    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 5636I               |
| TLV5636IDR.A                 | Active        | Production           | SOIC (D)   8    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 5636I               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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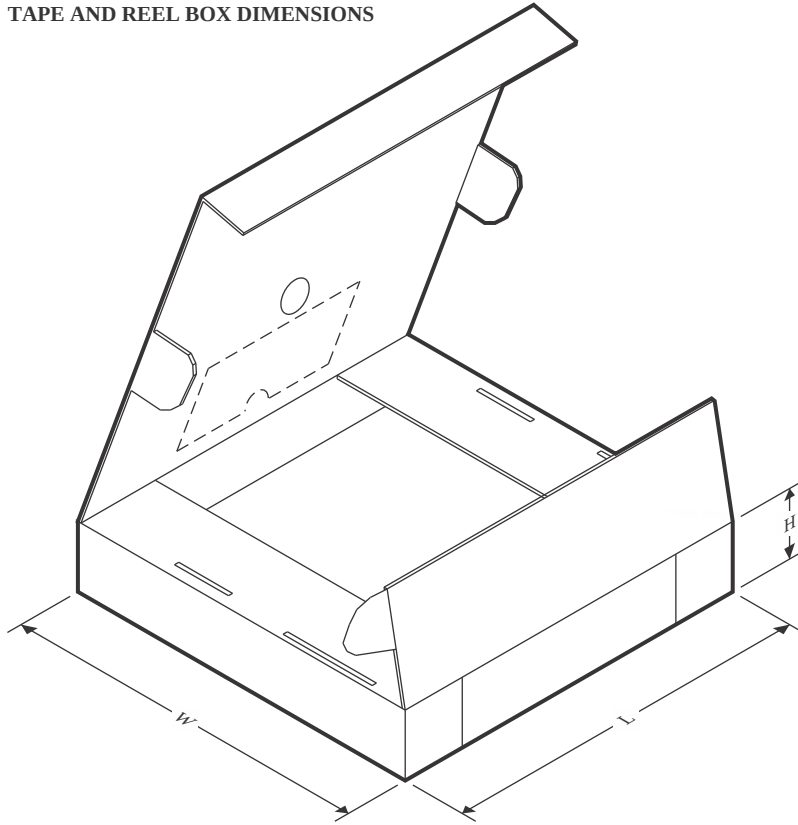
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV5636CDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV5636IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV5636IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV5636CDGKR | VSSOP        | DGK             | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TLV5636IDGKR | VSSOP        | DGK             | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TLV5636IDR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TLV5636CD     | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TLV5636CD.A   | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TLV5636CDGK   | DGK          | VSSOP        | 8    | 80  | 331.47 | 6.55   | 3000   | 2.88   |
| TLV5636CDGK.A | DGK          | VSSOP        | 8    | 80  | 331.47 | 6.55   | 3000   | 2.88   |
| TLV5636ID     | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TLV5636ID.A   | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TLV5636IDGK   | DGK          | VSSOP        | 8    | 80  | 331.47 | 6.55   | 3000   | 2.88   |
| TLV5636IDGK.A | DGK          | VSSOP        | 8    | 80  | 331.47 | 6.55   | 3000   | 2.88   |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



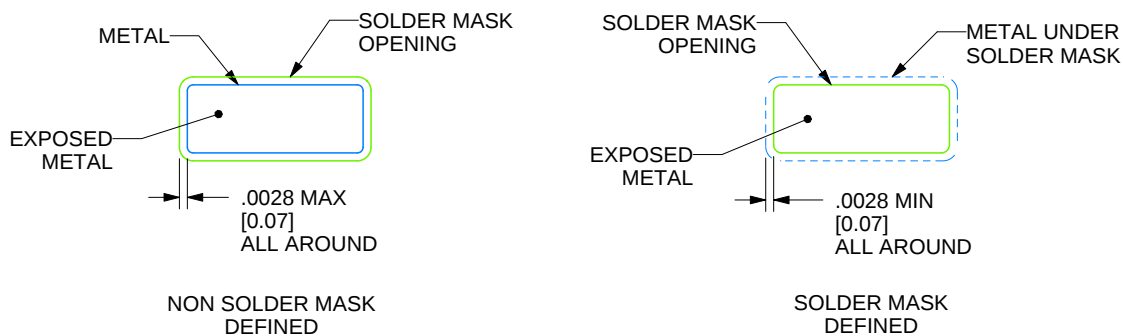
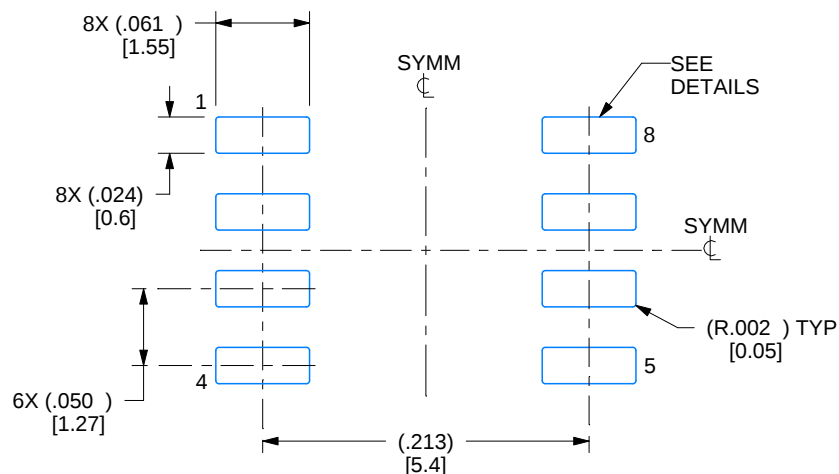
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

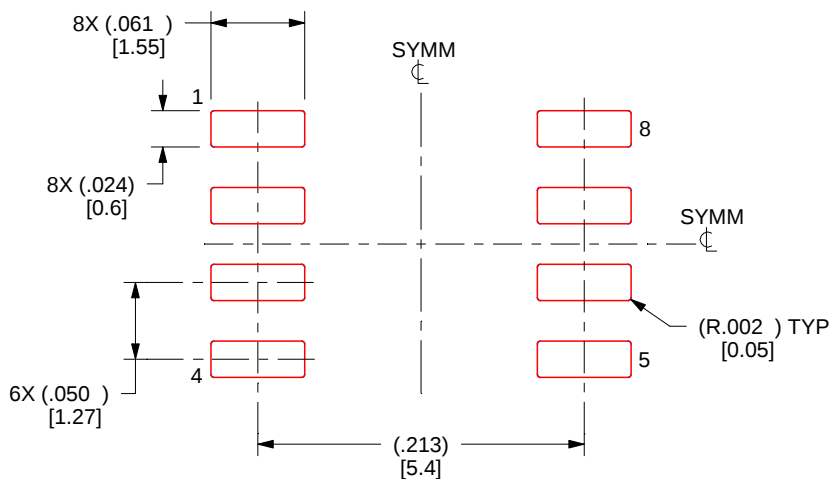
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



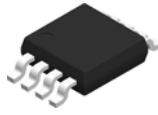
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

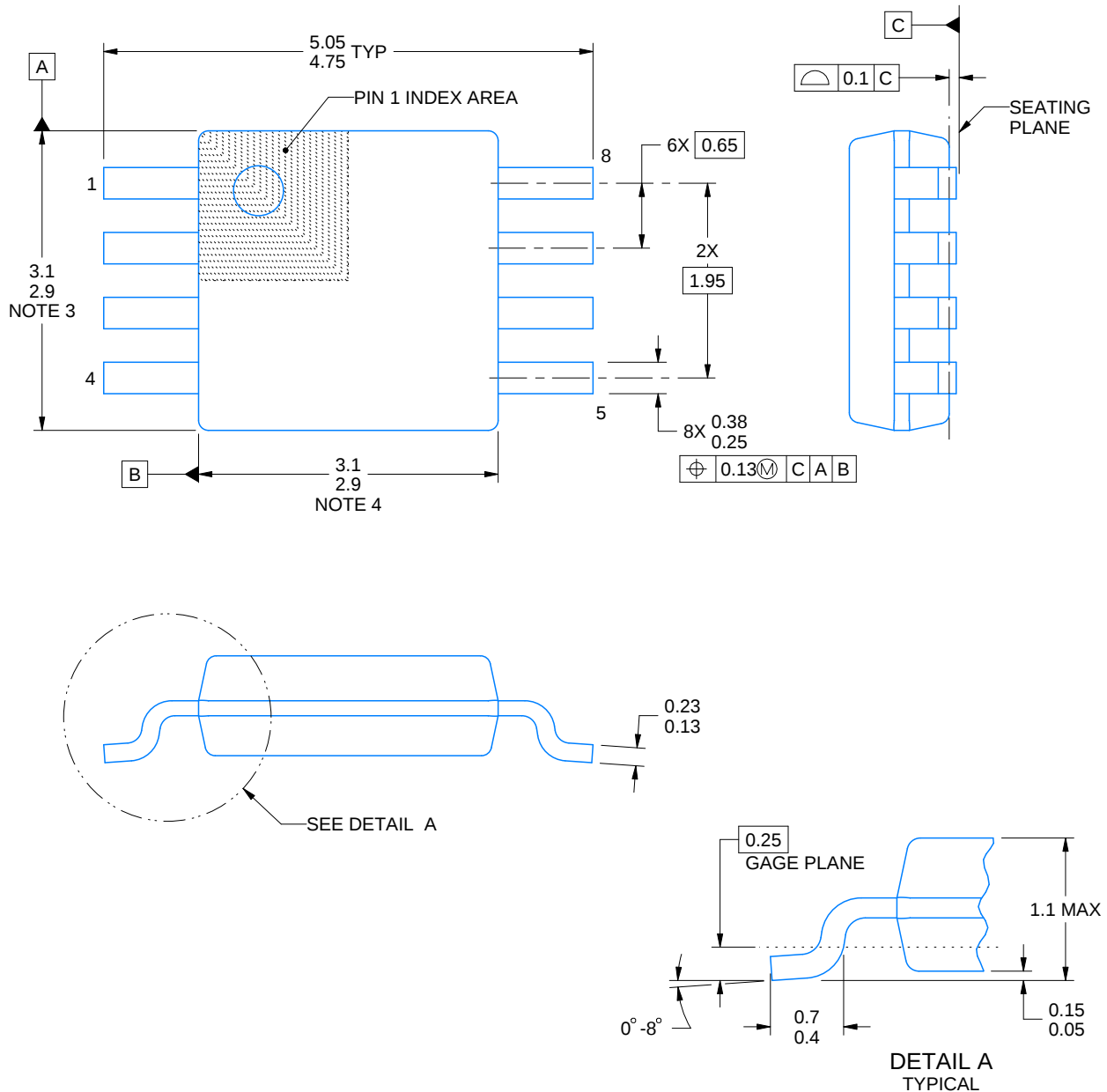
DGK0008A



## PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

### NOTES:

PowerPAD is a trademark of Texas Instruments.

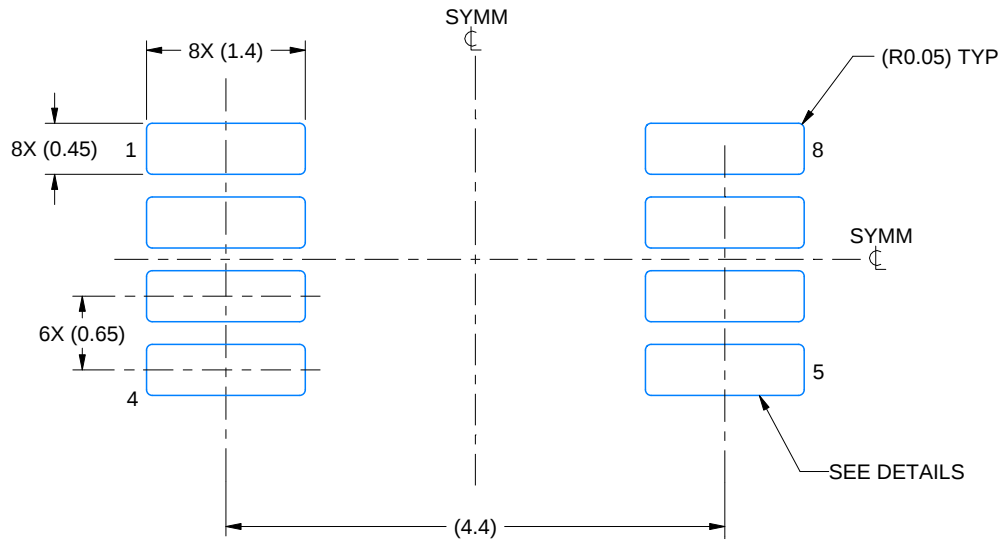
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

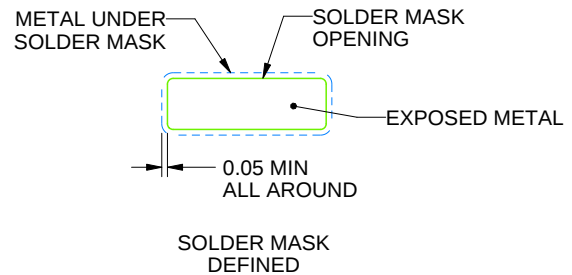
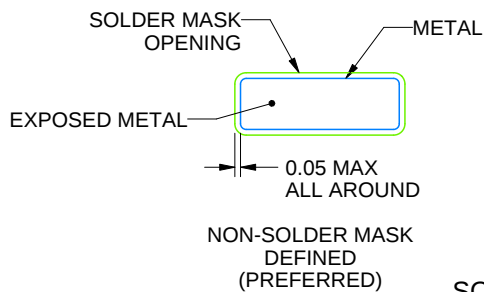
DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

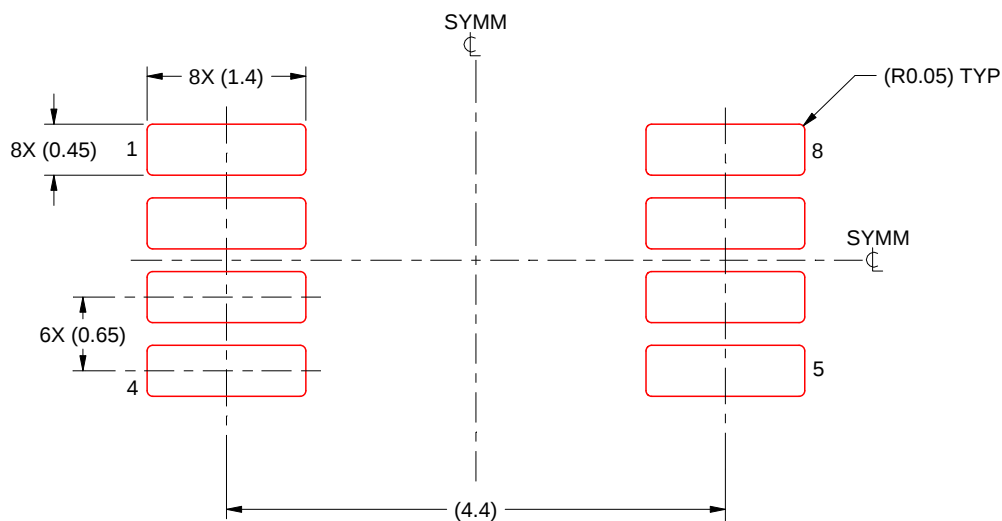
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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