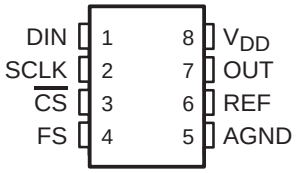
features

- 8-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
  - 1 μs in Fast Mode,
  - 3.5 μs in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity . . . <0.2 LSB
- Monotonic Over Temperature

D OR DGK PACKAGE
(TOP VIEW)



applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

description

The TLV5624 is a 8-bit voltage output DAC with a flexible 4-wire serial interface. The serial interface allows glueless interface to TMS320 and SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 8 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The programmable settling time of the DAC allows the designer to optimize speed vs power dissipation. With its on-chip programmable precision voltage reference, the TLV5624 simplifies overall system design.

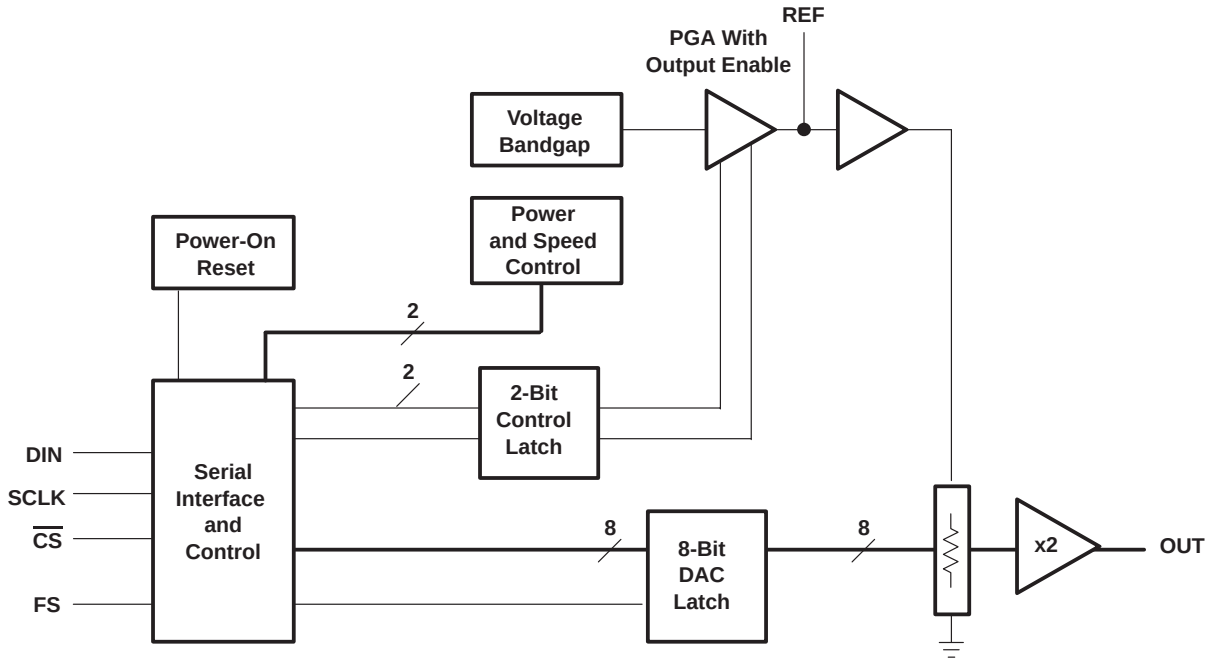
Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC and 8-pin MSOP package to reduce board space in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SOIC (D)	MSOP (DGK)
0°C to 70°C	TLV5624CD	TLV5624CDGK
−40°C to 85°C	TLV5624ID	TLV5624IDGK

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{CS}$	3	I	Chip select. Digital input active low, used to enable/disable inputs
DIN	1	I	Digital serial data input
FS	4	I	Frame sync input
OUT	7	O	DAC A analog voltage output
REF	6	I/O	Analog reference voltage input/output
SCLK	2	I	Digital serial clock input
V_{DD}	8	P	Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . . 7 V
Reference input voltage range . . . . . − 0.3 V to V_{DD} + 0.3 V
Digital input voltage range . . . . . − 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5624C . . . . . 0°C to 70°C
TLV5624I . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	
Power on reset, POR		0.55		2	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (see Note 1)	AGND	2.048	V_{DD} −1.5	V
Reference voltage, V_{ref} to REF terminal	V_{DD} = 3 V (see Note 1)	AGND	1.024	V_{DD} −1.5	V
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				20	MHz
Operating free-air temperature, T_A	TLV5624C	0		70	°C
	TLV5624I	−40		85	

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ (V_{DD}−0.4 V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		2.3	3.3	mA
			Slow		1.5	1.9	
	Power down supply current	See Figure 8			0.01	10	µA
PSRR	Power supply rejection ratio	Zero scale, See Note 2			−65		dB
		Full scale, See Note 3			−65		

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [(E_{ZS}(V_{DD}max) - E_{ZS}(V_{DD}min))/V_{DD}max]$
3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [(E_G(V_{DD}max) - E_G(V_{DD}min))/V_{DD}max]$

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8			bits
INL	Integral nonlinearity, end point adjusted	See Note 4		±0.3	±0.5	LSB
DNL	Differential nonlinearity	See Note 5		±0.07	±0.2	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See Note 6			±20	mV
E_{ZS} TC	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
E_G	Gain error	See Note 8			±0.6	% full scale V
E_G T_C	Gain error temperature coefficient	See Note 9		10		ppm/°C

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 255.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 255.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
8. Gain error is the deviation from the ideal output ($2V_{ref}$ − 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	R_L = 10 kΩ	0		V_{DD}−0.4	V
	Output load regulation accuracy	V_O = 4.096 V, 2.048 V R_L = 2 kΩ		±0.10	±0.25	% full scale V

reference pin configured as output (REF)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(OUTL)}$	Low reference voltage		1.003	1.024	1.045	V
$V_{ref(OUTH)}$	High reference voltage	V_{DD} > 4.75 V	2.027	2.048	2.069	V
$I_{ref(source)}$	Output source current				1	mA
$I_{ref(sink)}$	Output sink current		−1			mA
	Load capacitance		1	10		ωF
PSRR	Power supply rejection ratio			−65		dB

electrical characteristics over recommended operating conditions (unless otherwise noted) (Continued)

reference pin configured as input (REF)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage			0		$V_{DD}-1.5$	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc	Fast		1.3		MHz
			Slow		525		kHz
	Reference feedthrough	REF = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 10)			−80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V	−1			µA
C_i	Input capacitance			8		pF

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, See Note 11	Fast		1	3	µs
			Slow		3.5	7	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, See Note 12	Fast		0.5	1.5	µs
			Slow		1	2	
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See Note 13	Fast		8		V/µs
			Slow		1.5		
	Glitch energy	$\overline{DIN}$ = 0 to 1, $\overline{CS}$ = V_{DD}, f_{CLK} = 100 kHz,			5		nV−S
SNR	Signal-to-noise ratio	f_s = 480 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF		53	57		dB
S/(N+D)	Signal-to-noise + distortion			48	47		
THD	Total harmonic distortion				−50	−48	
	Spurious free dynamic range			50	62		

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDFand 0xFDF to 0x020 respectively. Not tested, assured by design.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su(CS-FS)}$	Setup time, $\overline{CS}$ low before FS falling edge	10			ns
$t_{su(FS-CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, 16th negative SCLK edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
$t_{su(C16-CS)}$	Setup time, 16th positive SCLK edge (first positive after D0 is sampled) before $\overline{CS}$ rising edge. If FS is used instead of 16th positive edge to update DAC, then setup time between FS rising edge and $\overline{CS}$ rising edge.	10			ns
t_{wH}	SCLK pulse duration high	25			ns
t_{wL}	SCLK pulse duration low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{H(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	FS pulse duration high	25			ns

PARAMETER MEASUREMENT INFORMATION

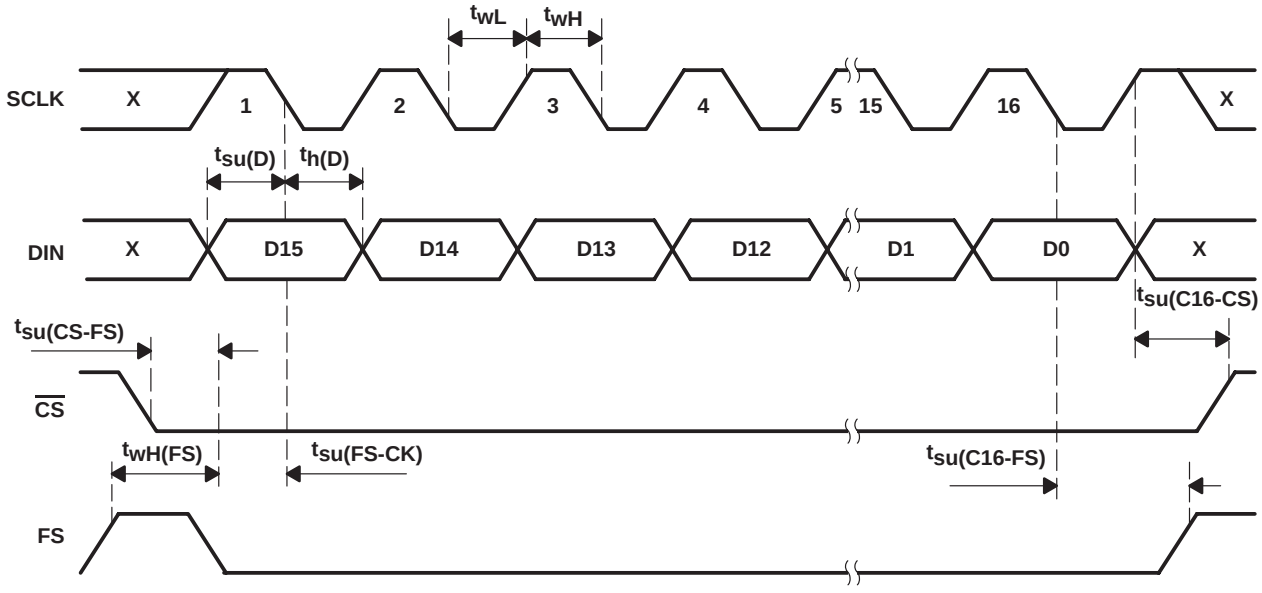


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LOAD CURRENT

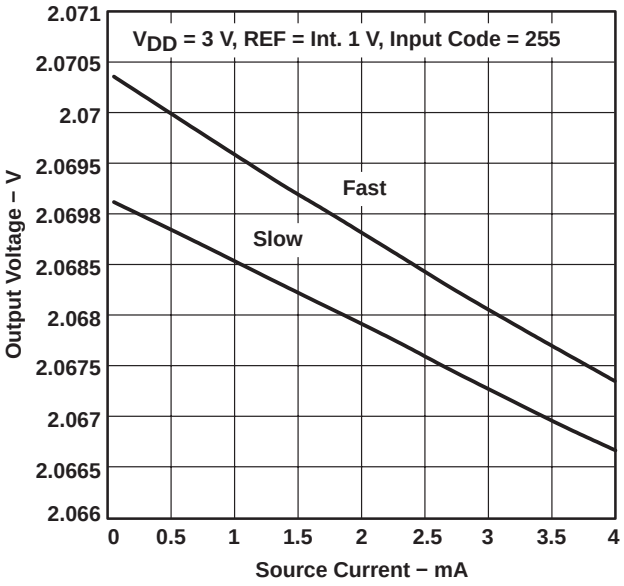


Figure 2

OUTPUT VOLTAGE
vs
LOAD CURRENT

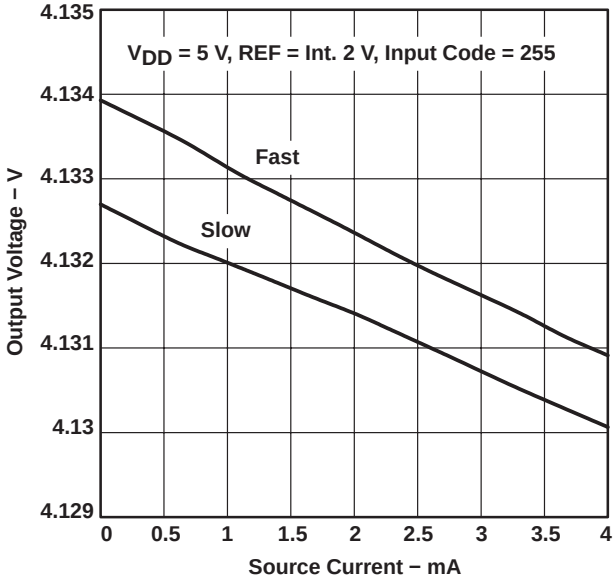


Figure 3

OUTPUT VOLTAGE
vs
LOAD CURRENT

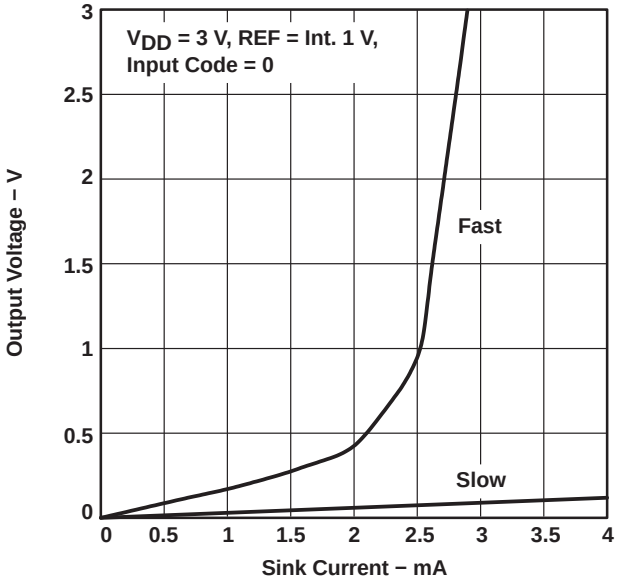


Figure 4

OUTPUT VOLTAGE
vs
LOAD CURRENT

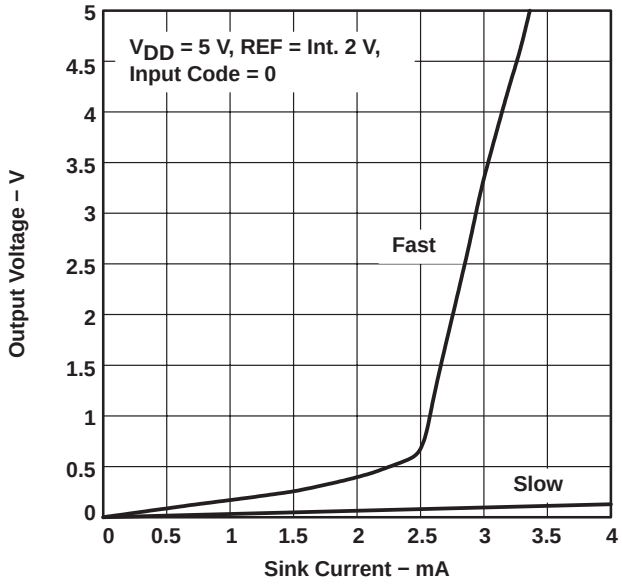


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
TEMPERATURE

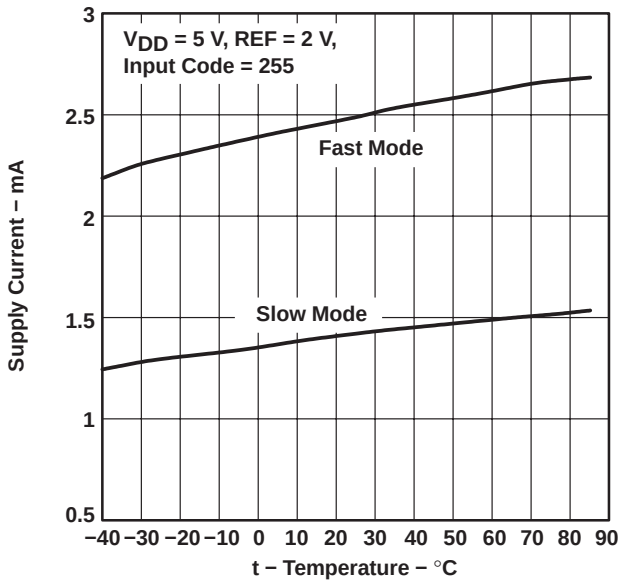


Figure 6

SUPPLY CURRENT
vs
TEMPERATURE

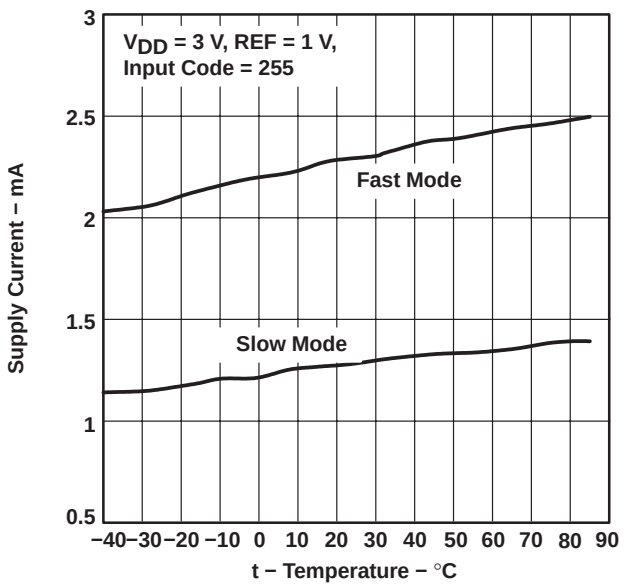


Figure 7

POWER DOWN SUPPLY CURRENT
vs
TIME

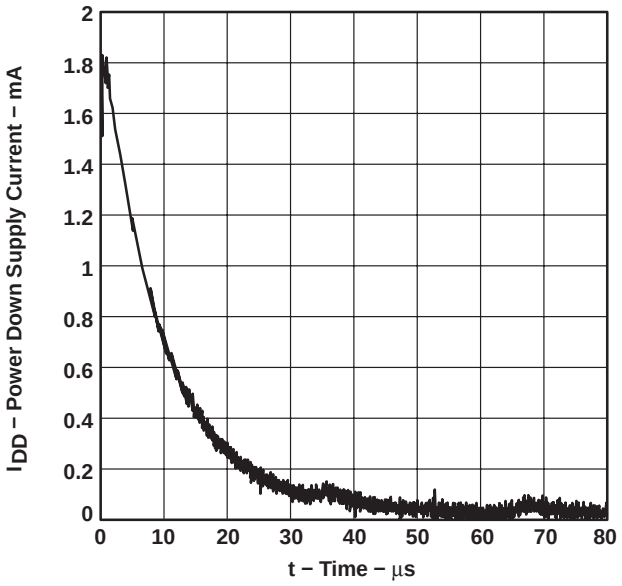


Figure 8

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

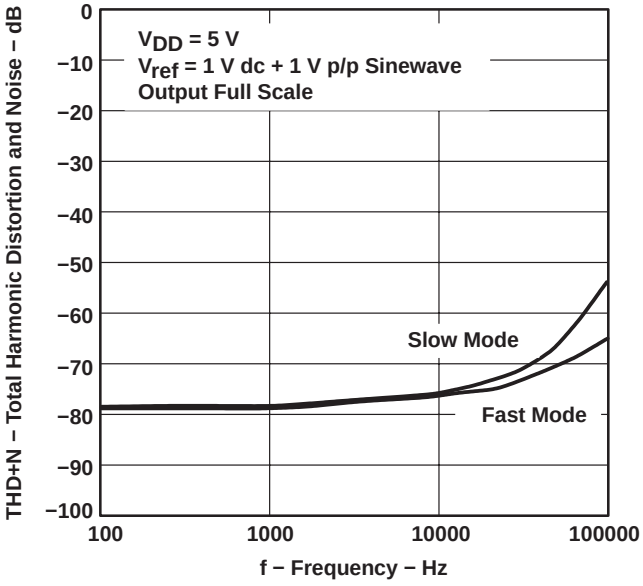


Figure 9

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION
vs
FREQUENCY**

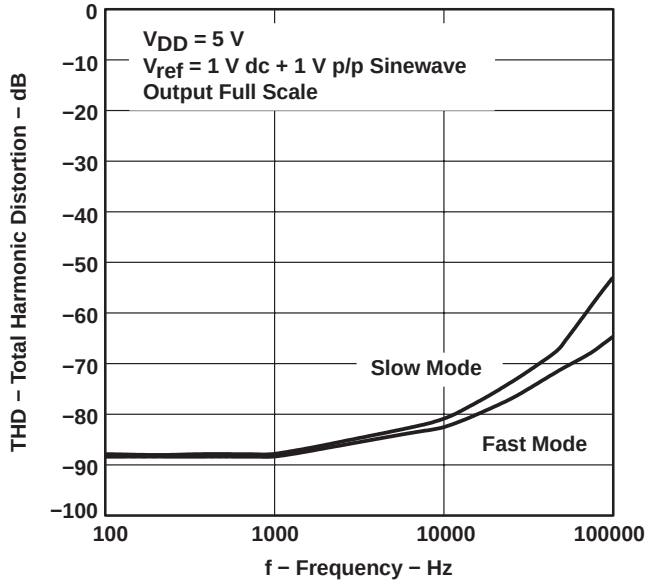


Figure 10

**DIFFERENTIAL NONLINEARITY
vs
DIGITAL OUTPUT CODE**

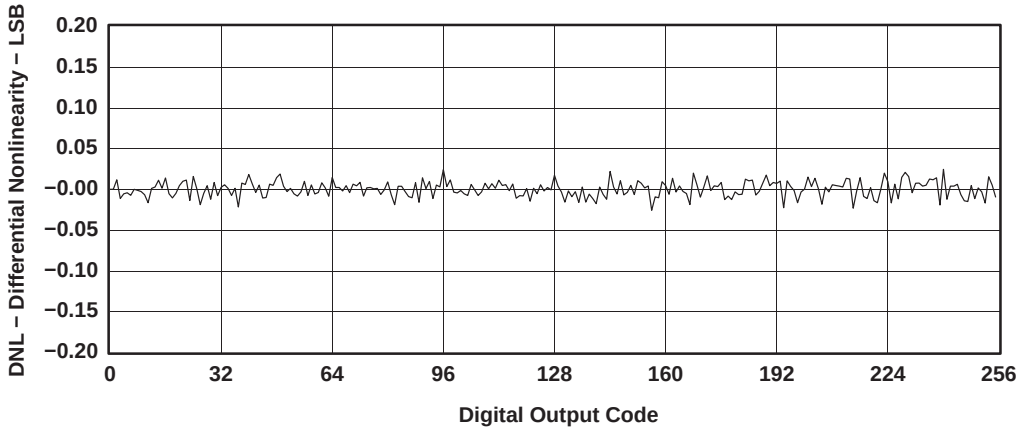


Figure 11

TYPICAL CHARACTERISTICS

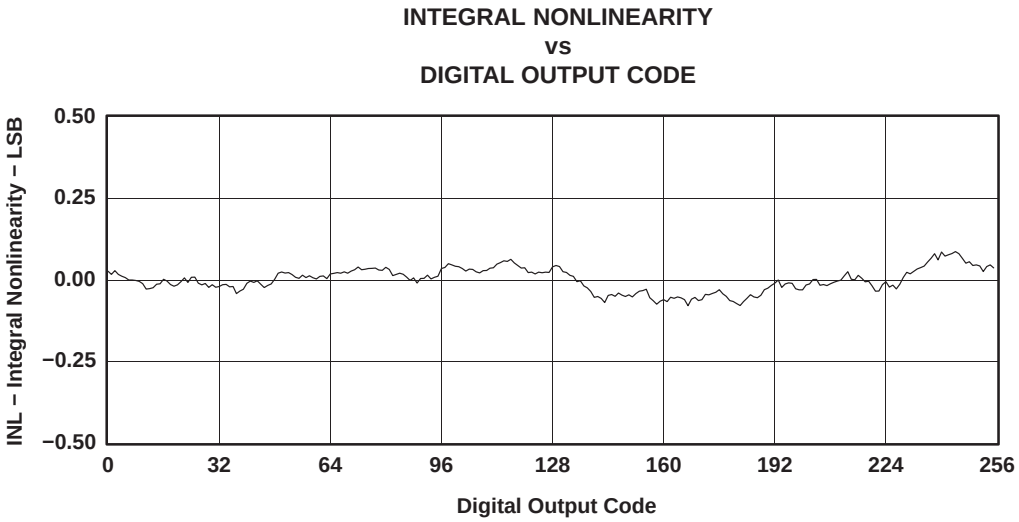


Figure 12

APPLICATION INFORMATION

general function

The TLV5624 is an 8-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{2^{n}}\ [\mathrm{V}]$$

where REF is the reference voltage and CODE is the digital input value within the range 0_{10} to 2^{n-1}, where n = 8 (bits). The 16-bit word, consisting of control bits and a new DAC value, is illustrated in the *data format* section. A power on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

The device has to be enabled with $\overline{\mathrm{CS}}$ set to low. A falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on high-low transitions of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5624 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four-wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). Figure 13 shows an example with two TLV5624s connected directly to a TMS320 DSP.

APPLICATION INFORMATION

serial interface (continued)

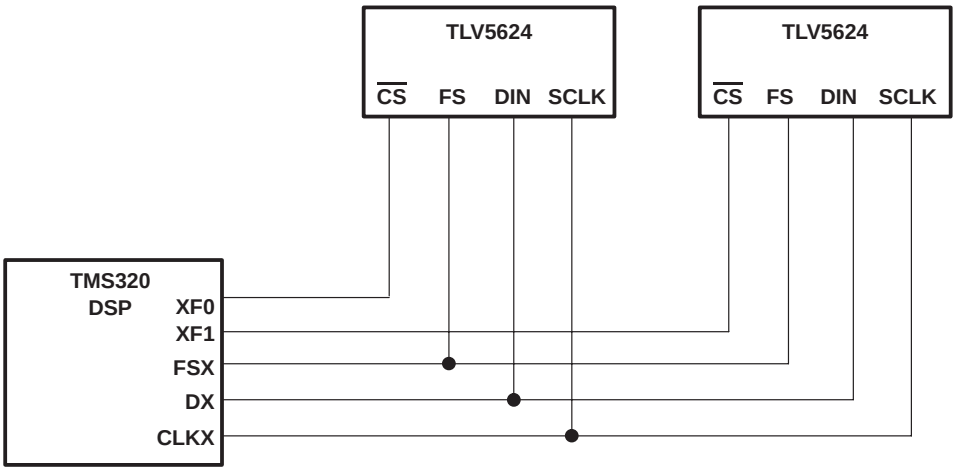


Figure 13. TMS320 Interface

If there is no need to have more than one device on the serial bus, then $\overline{CS}$ can be tied low. Figure 14 shows an example of how to connect the TLV5624 to TMS320, SPI™ or Microwire™ using only three pins.

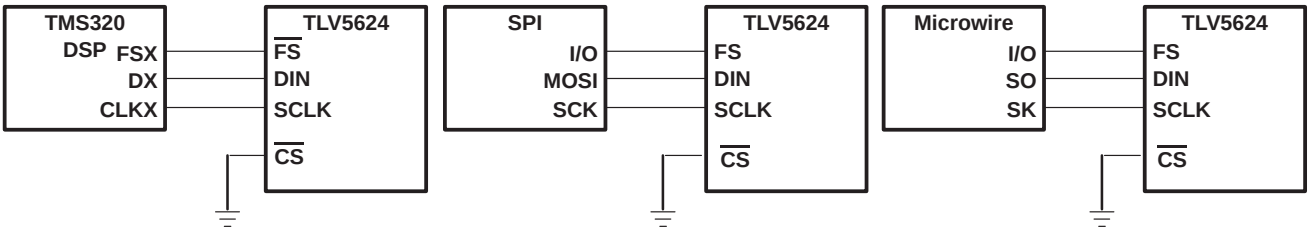


Figure 14. Three-Wire Interface

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI™ and Microwire™), two write operations must be performed to program the TLV5624. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the 16th falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.25 \text{ MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5624 has to be considered, too.

APPLICATION INFORMATION

data format

The 16-bit data word for the TLV5624 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	8 Data bits								0	0	0	0

SPD: Speed control bit 1 → fast mode 0 → slow mode
PWR: Power control bit 1 → power down 0 → normal operation

The following table lists the possible combination of the register select bits:

register select bits

R1	R0	REGISTER
0	0	Write data to DAC
0	1	Reserved
1	0	Reserved
1	1	Write data to control register

The meaning of the 12 data bits depends on the selected register. For the DAC register, bits D11...D4 determine the new DAC output value:

data bits: DAC

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
New DAC Value								0	0	0	0

If the control register is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

data bits: CONTROL

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	REF1	REF2

X: don't care

REF1 and REF0 determine the reference source and, if internal reference is selected, the reference voltage.

reference bits

REF1	REF0	REFERENCE
0	0	External
0	1	1.024 V
1	0	2.048 V
1	1	External

NOTE: A 0.1μF bypass capacitor must be installed on the reference pin (pin 6). If internal reference is used a 10 μF capacitor must also be installed for reference voltage stability.

CAUTION:
If external reference voltage is applied to the REF pin, external reference MUST be selected.

APPLICATION INFORMATION

Example:

- Set DAC output, select fast mode, select internal reference at 2.048 V:

  1. Set reference voltage to 2.048 V (CONTROL register):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

  2. Write new DAC value and update DAC output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New DAC output value								0	0	0	0

The DAC output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 15.

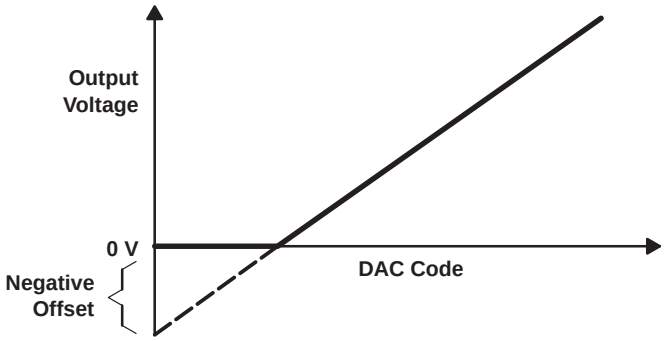


Figure 15. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1-μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 16 shows the ground plane layout and bypassing technique.

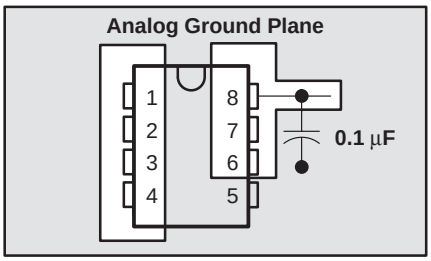


Figure 16. Power-Supply Bypassing

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

total harmonic distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV5624CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5624C
TLV5624CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5624C
TLV5624CDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5624C
TLV5624CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADR
TLV5624CDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADR
TLV5624CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADR
TLV5624CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADR
TLV5624ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5624I
TLV5624ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5624I
TLV5624IDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADS
TLV5624IDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADS
TLV5624IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADS
TLV5624IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADS
TLV5624IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5624I
TLV5624IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5624I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

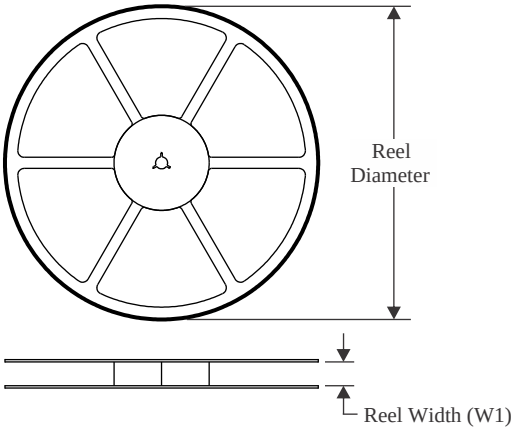
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

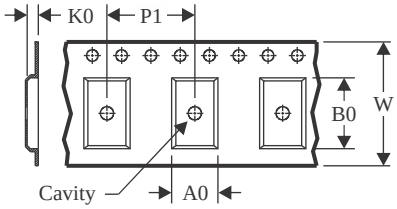
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

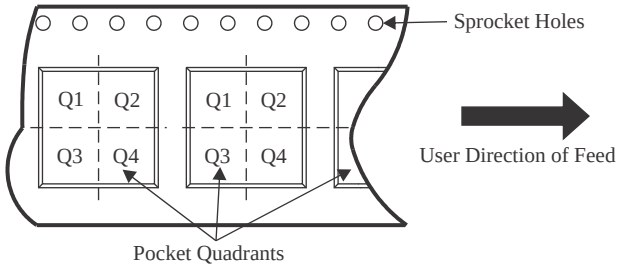


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

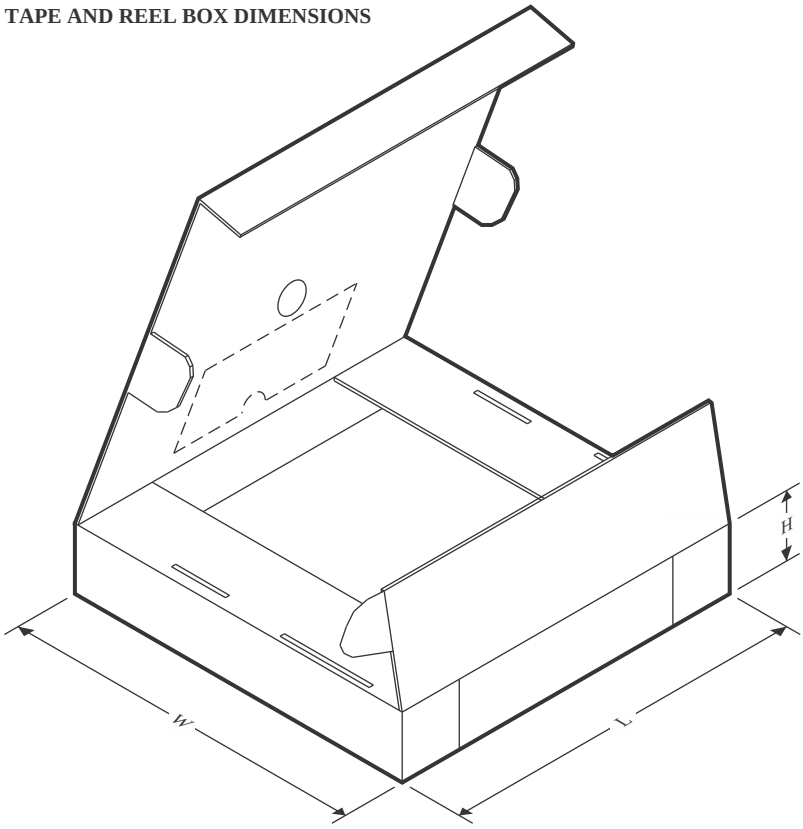
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5624CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5624IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5624IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

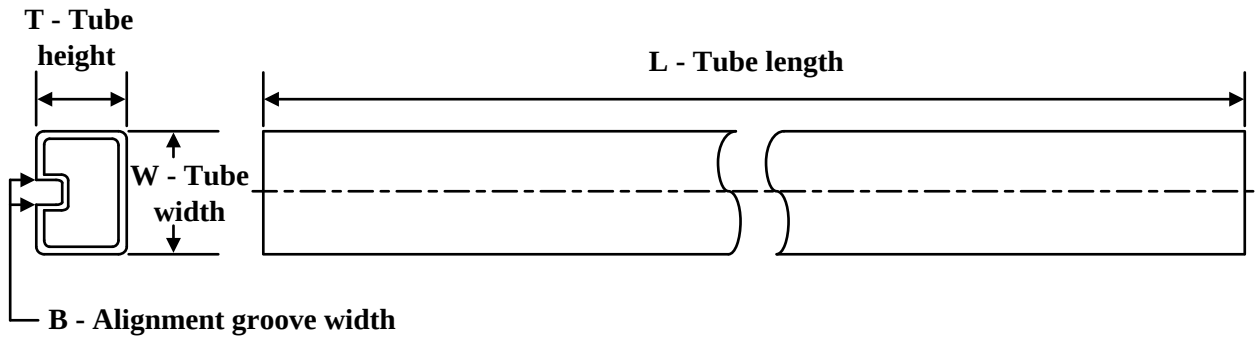
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

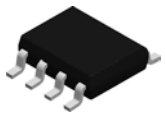
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5624CDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5624IDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5624IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5624CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5624CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5624CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLV5624CDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5624CDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5624ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV5624ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5624IDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5624IDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88

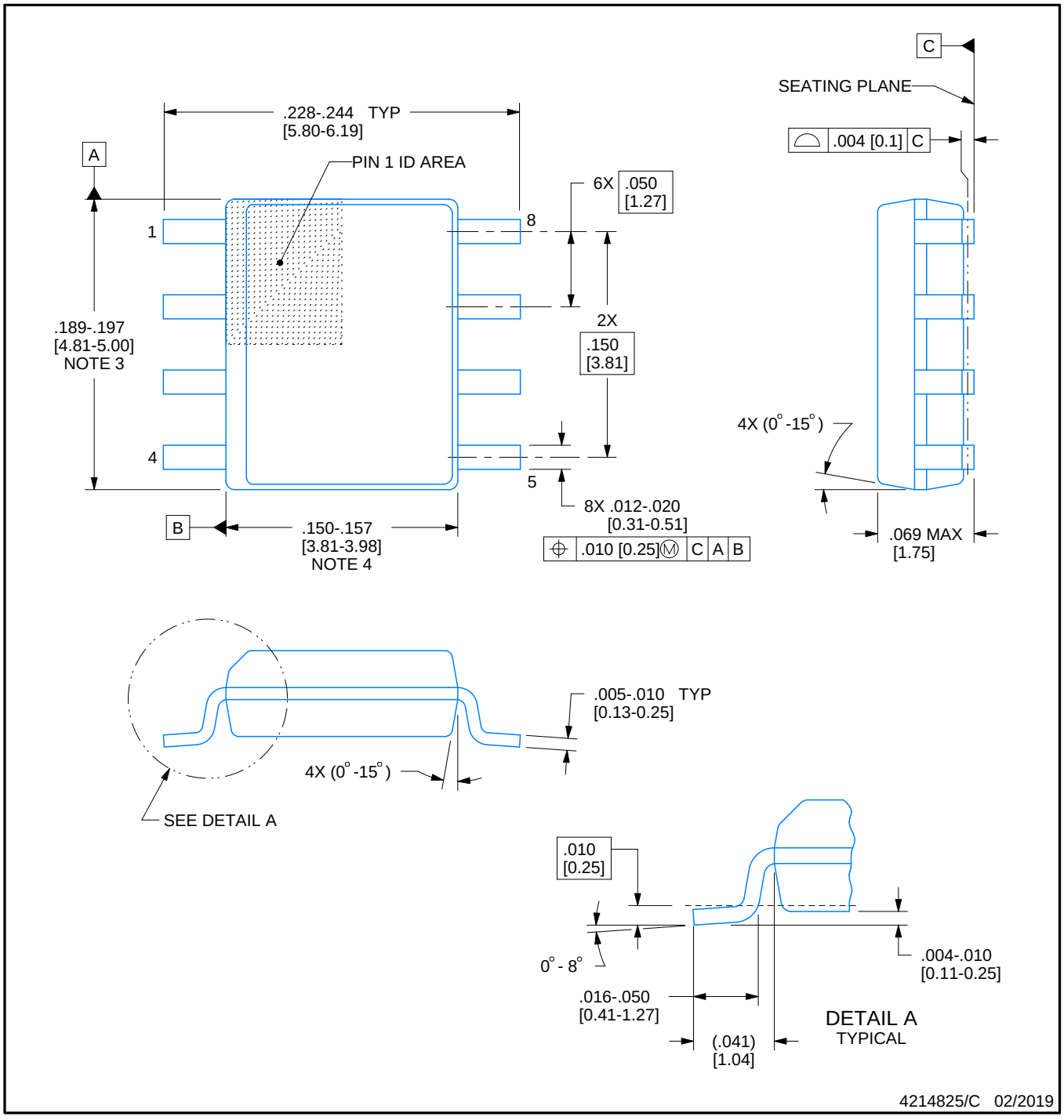


PACKAGE OUTLINE

D0008A

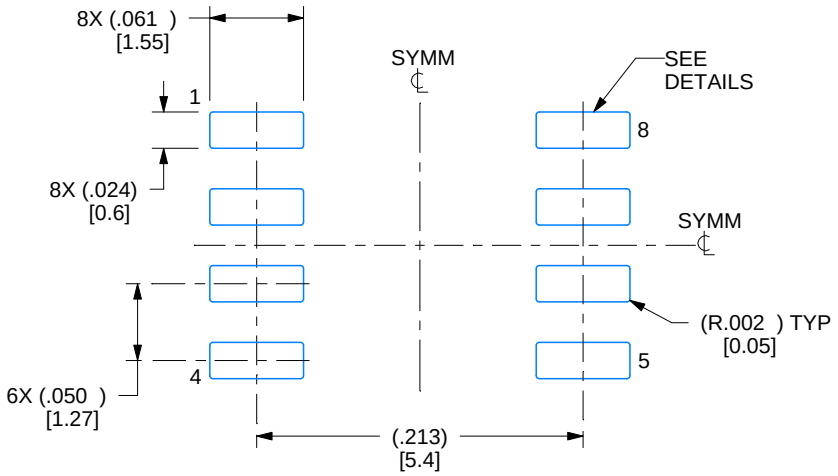
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

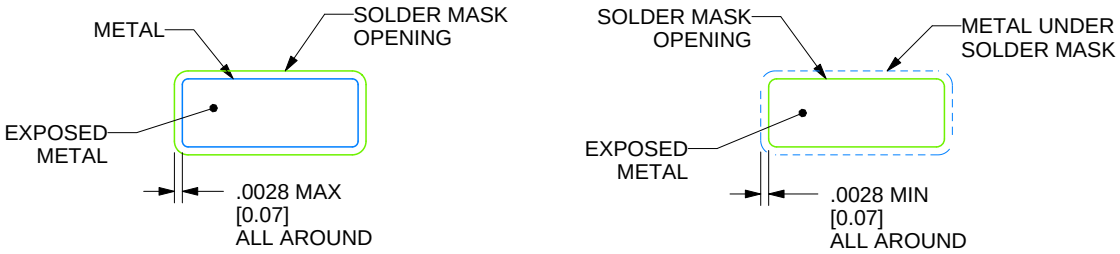


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

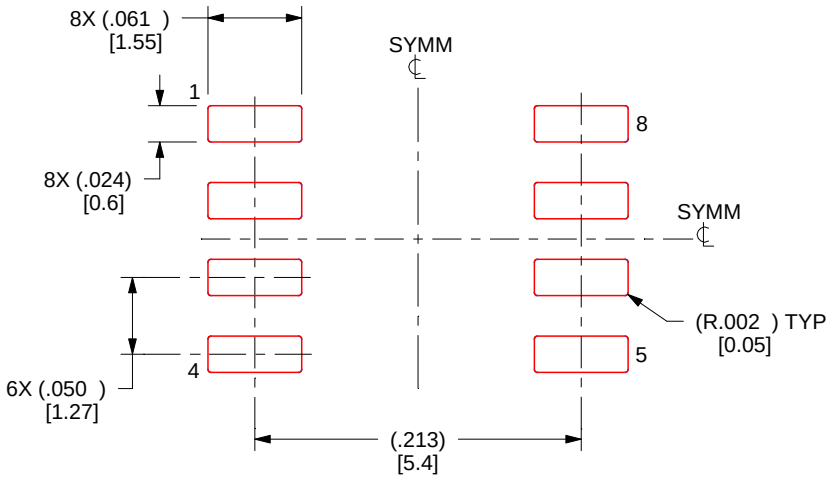
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

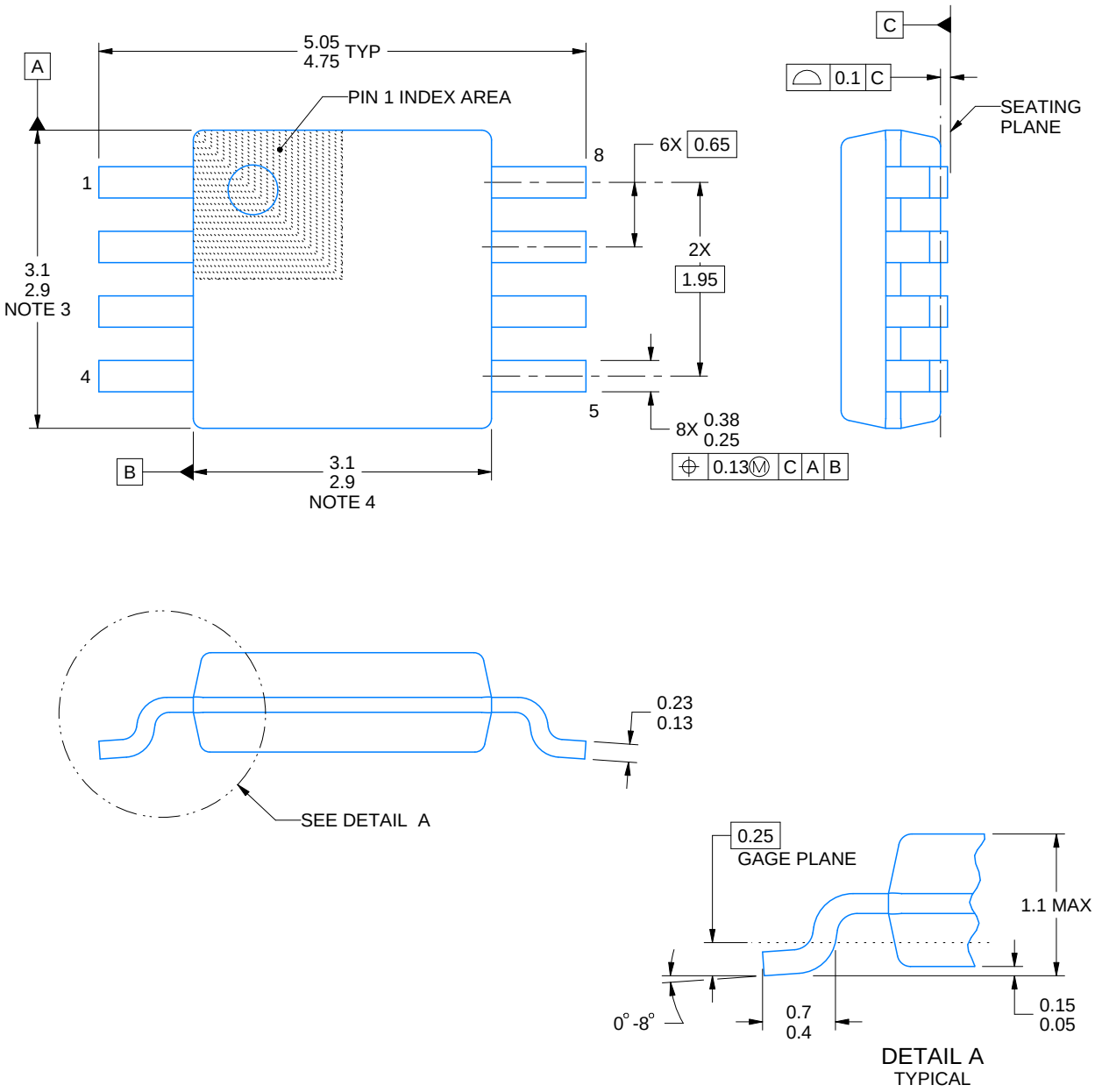
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

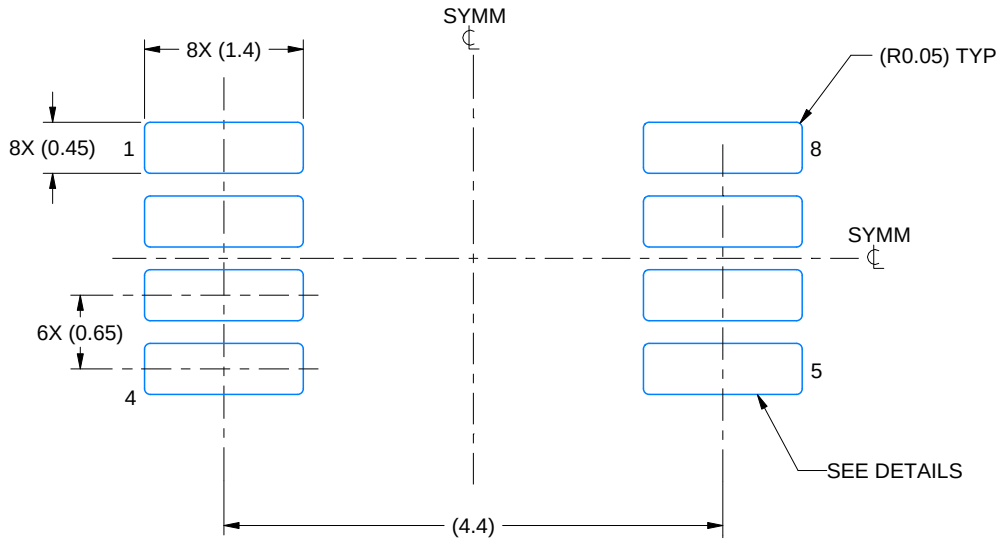
SMALL OUTLINE PACKAGE



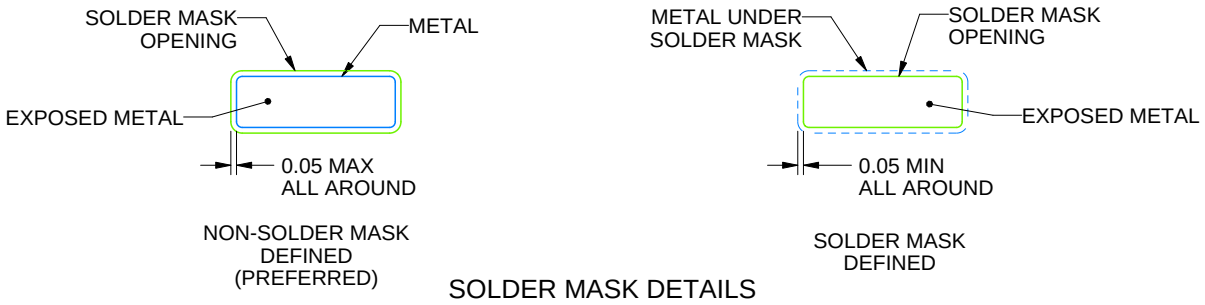
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

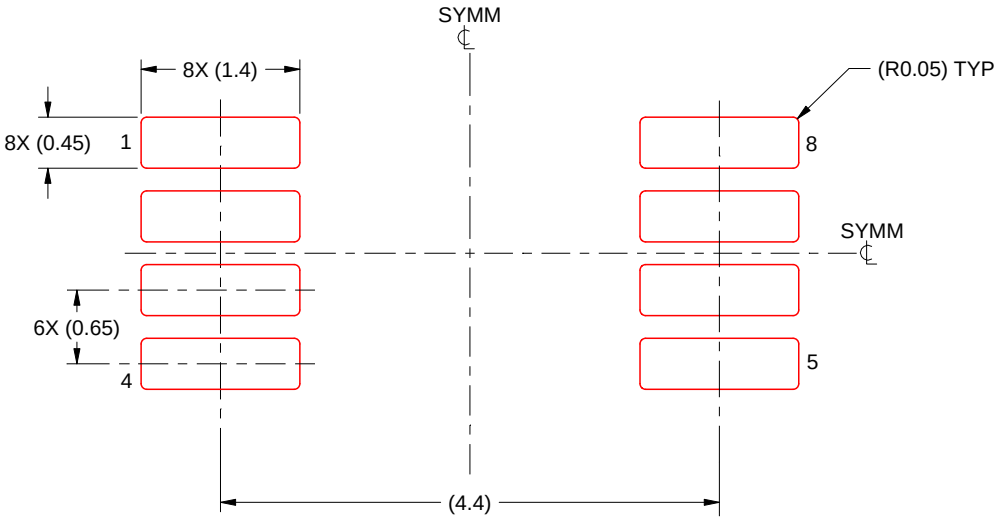


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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