TLV2231 Advanced, Rail-to-Rail, Low-Power, Single, LinCMOS™ Operational Amplifier

1 Features

- Output swing includes both supply rails
- Low noise: 15nV/√Hz typ at f = 1kHz
- Low input bias current: 1pA typ
- Fully specified for single-supply 3V and 5V operation
- Common-mode input voltage range includes negative rail
- High gain bandwidth: 2MHz at V_{DD} = 5V with 600Ω load
- High slew rate: 1.6V/μs at V_{DD} = 5V
- Wide supply voltage range: 2.7V to 10V

2 Applications

- Low-power audio preamplifier
- Multiplexed data-acquisition systems
- Test and measurement equipment
- Optical module
- Programmable logic controllers
- Server PSU

3 Description

The TLV2231 is a single low-voltage operational amplifier available in the SOT-23 package. The TLV2231 offers 2MHz of bandwidth and 1.6V/μs of slew rate for applications requiring good ac performance. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2231 is fully characterized at 3V and 5V and is optimized for low-voltage applications.

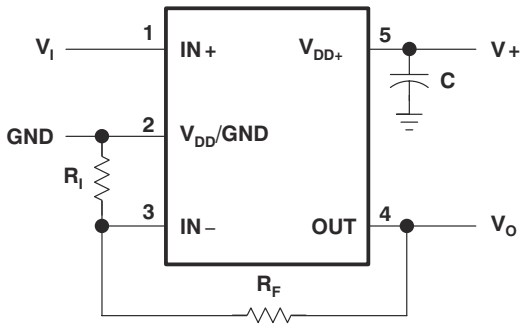
The TLV2231, with a high input impedance and low noise, is excellent for small-signal conditioning of high-impedance sources, such as piezoelectric transducers. As a result of the micropower dissipation levels combined with 3V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). The device also drives 600Ω loads for telecom applications.

With a total area of 5.6mm^2, the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, and minimizes noise pick-up from long printed circuit board (PCB) traces. TI also takes special care to provide a pinout that is optimized for board layout (see the following figure). Both inputs are separated by ground to prevent coupling or leakage paths. The OUT and IN– pins are on the same end of the board to provide negative feedback. Finally, gain setting resistors and the decoupling capacitor are easily placed around the package.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
TLV2231	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) See Section 4.
(2) For all available packages, see Section 10.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Surface-Mount Layout for a Fixed-Gain Noninverting Amplifier

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4 Available Options

T_A	V_{IO}MAX AT +25°C	PACKAGED DEVICES	SYMBOL
		SOT23 (DBV)(1)	
0°C to +70°C	3mV	TLV2231CDBV	VAEC
–40°C to +85°C	3mV	TLV2231IDBV	VAEI

(1) The DBV package is available in tape and reel only.

5 Pin Configuration and Functions

DBV PACKAGE
(TOP VIEW)

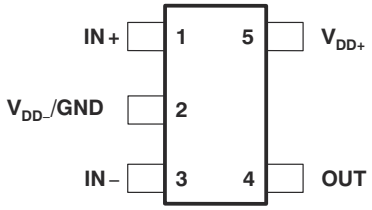


Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN–	3	Input	Inverting input
IN+	1	Input	Noninverting input
OUT	4	Output	Output
V_{DD+}	5	Power	Positive (highest) power supply
V_{DD-}/GND	2	Power	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			12	V
V_{ID}	Differential input voltage(3)		$-V_{DD}$	$+V_{DD}$	V
V_I	Input voltage range(2), any input		–0.3V	V_{DD}	V
I_I	Input current, each input		–5	5	mA
I_O	Output current		–50	50	mA
	Total current into V_{DD+}		–50	50	mA
	Total current out of V_{DD-}		–50	50	mA
	Duration of short-circuit current at (or less than) 25°C(4)			Unlimited	
	Continuous total power dissipation			See *Section 6.2*	
T_A	Operating free-air temperature	TLV2231C	0	70	°C
		TLV2231I	–40	85	
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1.6mm (1/16inch) from case for 10s, DBV package			260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to V_{DD-}.
(3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought to less than (V_{DD-}) – (0.3V).
(4) The output is able to be shorted to either supply. Limit temperature, supply voltages, or both to not exceed the maximum dissipation rating.

6.2 Dissipation Ratings

PACKAGE	$T_A \le +25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25°C$	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING
DBV	150mW	1.2mW/°C	96mW	78mW

6.3 Recommended Operating Conditions

		TLV2231C		TLV2231I		UNIT
		MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage(1)	2.7	10	2.7	10	V
V_I	Input voltage	V_{DD-}	$(V_{DD+}) - 1.3$	V_{DD-}	$(V_{DD+}) - 1.3$	V
V_{IC}	Common-mode input voltage	V_{DD-}	$(V_{DD+}) - (1.3)$	V_{DD-}	$(V_{DD+}) - (1.3)$	V
T_A	Operating free-air temperature	0	70	–40	85	°C

(1) All voltage values, except differential voltages, are with respect to V_{DD-}.

6.4 Electrical Characteristics: V_{DD} = 3V

at specified free-air temperature and V_{DD} = 3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV2231C, TLV2231I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0V, V_O = 0V, R_S = 50Ω		Full range		0.75	3	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0V, V_O = 0V, R_S = 50Ω		Full range		0.5		μV/°C
I_{IO}	Input offset current(2)	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0V, V_O = 0V, R_S = 50Ω		25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current(2)	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0V, V_O = 0V, R_S = 50Ω		25°C		1	60	pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω, $\lvert V_{IO}\rvert \le$ 5mV		25°C	0 to 2			V
V_{OH}	High-level output voltage	I_{OH} = –1mA		25°C		2.87		V
		I_{OH} = –2mA		25°C		2.74		
				Full range	2			
V_{OL}	Low-level output voltage	V_{IC} = 1.5V, I_{OL} = 50μA		25°C		10		mV
		V_{IC} = 1.5V, I_{OL} = 500μA		25°C		100		
				Full range			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5V, V_O = 1V to 2V	R_L = 600Ω(3)	25°C	1	1.6		V/mV
				Full range	0.3			
			R_L = 1MΩ(3)	25°C		250		
r_{id}	Differential input resistance			25°C		540		GΩ
r_{ic}	Common-mode input resistance			25°C		1		TΩ
c_{ic}	Common-mode input capacitance	f = 10kHz		25°C		1		pF
z_o	Open-loop output impedance	f = 1MHz, I_O = 0A		25°C		525		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 1.7V, V_O = 1.5V, R_S = 50Ω		25°C	54	70		dB
				Full range	54			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7V to 8V, V_{IC} = V_{DD}/2, no load		25°C	70	96		dB
				Full range	70			
I_{DD}	Supply current	V_O = 1.5V, no load		25°C		750	1200	μA
				Full range			1500	

(1) Full range for the TLV2231C is 0°C to 70°C. Full range for the TLV2231I is –40°C to +85°C.
(2) Specified by characterization.
(3) Referenced to 1.5V.

6.5 Operating Characteristics, V_{DD} = 3V

at specified free-air temperature and V_{DD} = 3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLV2231C, TLV2231I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1V to 1.9V, R_L = 600Ω(2), C_L = 100pF(2)	+25°C	0.24	0.25		V/µs
			Full range	0.24			V/µs
V_n	Equivalent input noise voltage	f = 1kHz	+25°C		16		nV/√Hz
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 10Hz	+25°C		1.8		µV
I_n	Equivalent input noise current		+25°C		2		fA/√Hz
THD+N	Total harmonic distortion plus noise		+25°C	See *Section 6.8*			
	Gain-bandwidth product	f = 10kHz, R_L = 600Ω(2), C_L = 100pF(2)	+25°C		1.9		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 1V, A_V = 1, R_L = 600Ω(2), C_L = 100pF(2)	+25°C		60		kHz
φm	Phase margin at unity gain	R_L = 600Ω(2), C_L = 100pF(2)	+25°C		50		°

(1) Full range is –40°C to +85°C.
(2) Referenced to 1.5V.

6.6 Electrical Characteristics, V_{DD} = 5V

at specified free-air temperature and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV2231C, TLV2231I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		0.71	3	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		0.5		μV/°C
I_{IO}	Input offset current(2)	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		0.5	60	pA
				Full range			150	pA
I_{IB}	Input bias current(2)	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		1	60	pA
				Full range			150	pA
V_{ICR}	Common-mode input voltage range	R_S = 50Ω, $\lvert V_{IO}\rvert \le$ 5mV		+25°C	0 to 4			V
V_{OH}	High-level output voltage	I_{OH} = –1mA		+25°C		4.9		V
		I_{OH} = –4mA		+25°C		4.6		V
				Full range	4			V
V_{OL}	Low-level output voltage	V_{IC} = 2.5V, I_{OL} = 500μA		+25°C		80		mV
		V_{IC} = 2.5V, I_{OL} = 1mA		+25°C		160		mV
				Full range			500	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5V, V_O = 1V to 4V	R_L = 600Ω(3)	+25°C	1	1.5		V/mV
				Full range	0.3			V/mV
			R_L = 1MΩ(3)	+25°C		400		V/mV
r_{id}	Differential input resistance			+25°C		540		GΩ
r_{ic}	Common-mode input resistance			+25°C		1		TΩ
c_{ic}	Common-mode input capacitance	f = 10kHz		+25°C		1		pF
z_o	Open-loop output impedance	f = 1MHz, I_O = 0A		+25°C		525		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 2.7V, V_O = 2.5V, R_S = 50Ω		+25°C	60	70		dB
				Full range	55			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4V to 8V, V_{IC} = V_{DD}/2, no load		+25°C	70	96		dB
				Full range	70			dB
I_{DD}	Supply current	V_O = 2.5V, no load		+25°C		850	1300	μA
				Full range			1600	μA

(1) Full range for the TLV2231C is 0°C to 70°C. Full range for the TLV2231I is –40°C to +85°C.
(2) Specified by characterization.
(3) Referenced to 2.5V.

6.7 Operating Characteristics, V_{DD} = 5V

at specified free-air temperature and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLV2231C, TLV2231I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5V to 3.5V, R_L = 600Ω(2), C_L = 100pF(2)	+25°C	1	1.6		V/µs
			Full range	0.7			V/µs
V_n	Equivalent input noise voltage	f = 1kHz	+25°C		15		nV/√Hz
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 10Hz	+25°C		1.8		µV
I_n	Equivalent input noise current		+25°C		2		fA/√Hz
THD+N	Total harmonic distortion plus noise		+25°C	See *Section 6.8*			
	Gain-bandwidth product	f = 10kHz, R_L = 600Ω(2), C_L = 100pF(2)	+25°C		2		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 1V, A_V = 1, R_L = 600Ω(2), C_L = 100pF(2)	+25°C		300		kHz
φm	Phase margin at unity gain	R_L = 600Ω(2), C_L = 100pF(2)	+25°C		48		°

(1) Full range is –40°C to +85°C.
(2) Referenced to 2.5V.

6.8 Typical Characteristics

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Table 6-1. Table of Graphs

V_{IO}	Input offset voltage	Distribution	Figure 6-1, Figure 6-2
		vs Common-mode input voltage	Figure 6-3, Figure 6-4
αV_{IO}	Input offset voltage temperature coefficient	Distribution	Figure 6-5, Figure 6-6
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	Figure 6-7
V_{OH}	High-level output voltage	vs High-level output current	Figure 6-8, Figure 6-10
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 6-9, Figure 6-11
I_{OS}	Short-circuit output current	vs Free-air temperature	Figure 6-12
A_{VD}	Large-signal differential voltage amplification	vs Frequency	Figure 6-13, Figure 6-14
CMRR	Common-mode rejection ratio	vs Frequency	Figure 6-15
		vs Free-air temperature	Figure 6-16
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	Figure 6-17, Figure 6-18
		vs Free-air temperature	Figure 6-19
I_{DD}	Supply current	vs Supply voltage	Figure 6-20
V_O	Inverting large-signal pulse response	vs Time	Figure 6-21, Figure 6-22
V_O	Voltage-follower large-signal pulse response	vs Time	Figure 6-23, Figure 6-24
V_O	Inverting small-signal pulse response	vs Time	Figure 6-25, Figure 6-26
V_O	Voltage-follower small-signal pulse response	vs Time	Figure 6-27, Figure 6-28
V_n	Equivalent input noise voltage	vs Frequency	Figure 6-29, Figure 6-30
	Noise voltage (referred to input)	Over a 10-second period	Figure 6-31
THD + N	Total harmonic distortion plus noise	vs Frequency	Figure 6-32
φ_m	Phase margin	vs Load capacitance	Figure 6-33

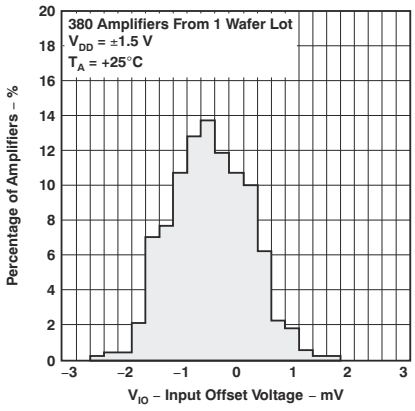


Figure 6-1. Distribution of TLV2231 Input Offset Voltage

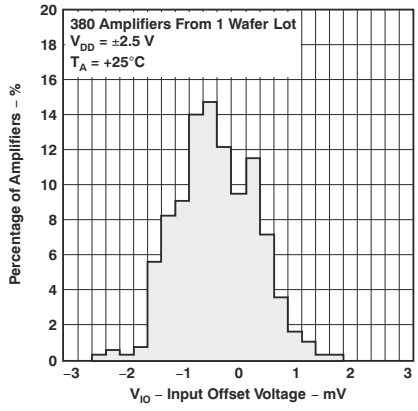
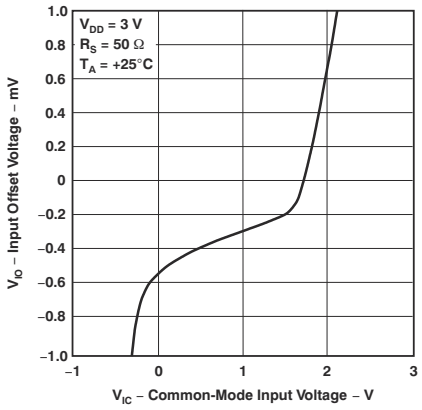


Figure 6-2. Distribution of TLV2231 Input Offset Voltage

6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices



Load referenced to 1.5V

Figure 6-3. Input Offset Voltage vs Common-Mode Input Voltage

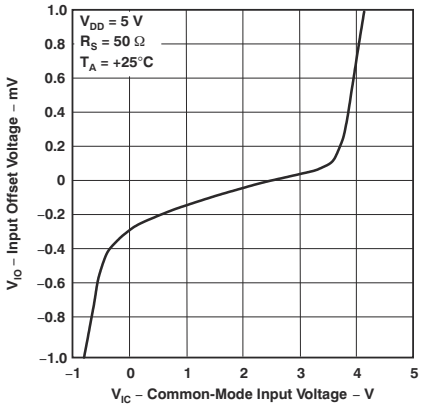


Figure 6-4. Input Offset Voltage vs Common-Mode Input Voltage

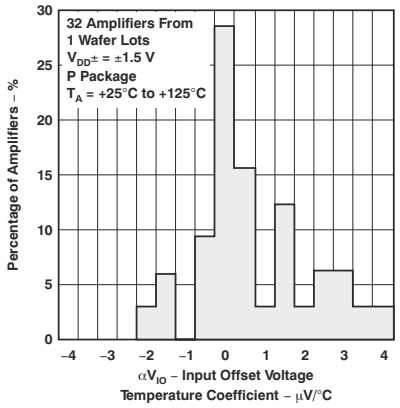


Figure 6-5. Distribution of TLV2231 Input Offset voltage Temperature Coefficient

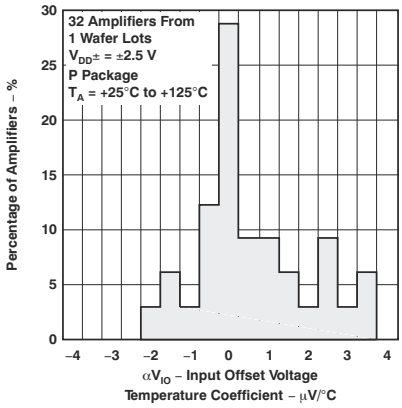


Figure 6-6. Distribution of TLV2231 Input Offset Voltage Temperature Coefficient

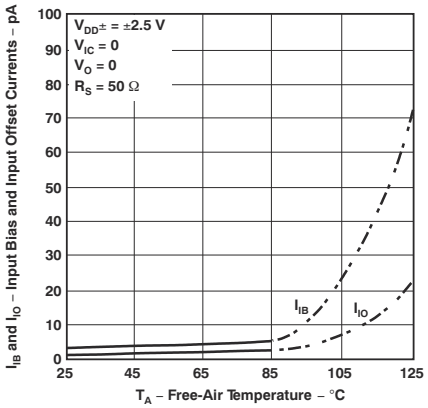
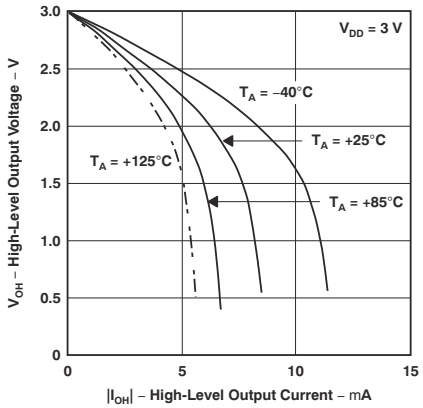


Figure 6-7. Input Bias and Input Offset Currents vs Free-Air Temperature

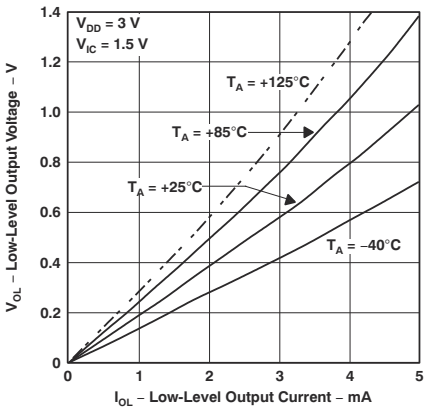


Load referenced to 1.5V

Figure 6-8. High-Level Output Voltage vs High-Level Output Current

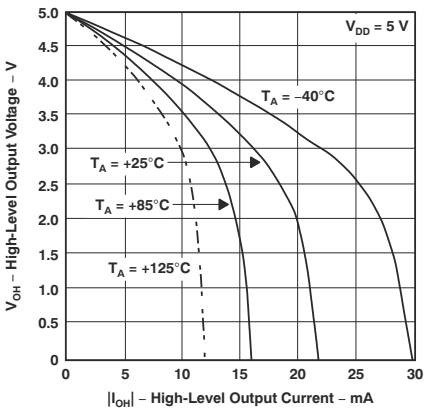
6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices



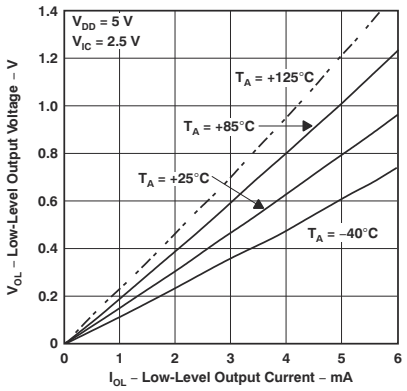
Load referenced to 1.5V

Figure 6-9. Low-level Output Voltage vs Low-Level Output Current



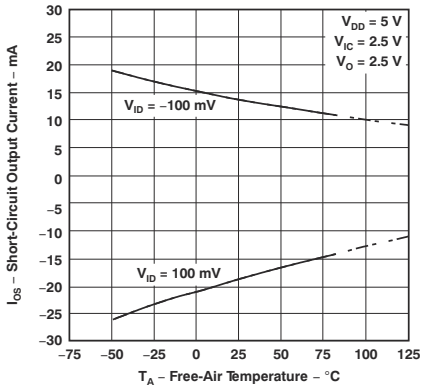
Load referenced to 2.5V

Figure 6-10. High-Level Output Voltage vs High-Level Output Current



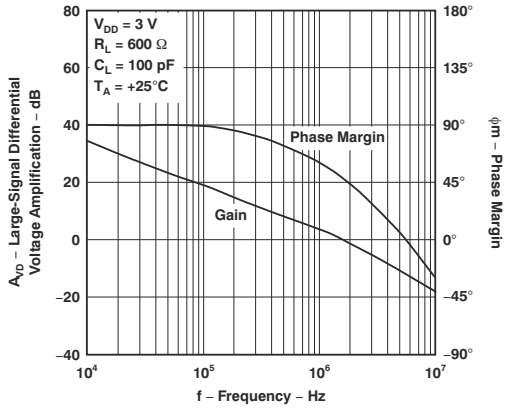
Load referenced to 2.5V

Figure 6-11. Low-Level Output Voltage vs Low-Level Output Current



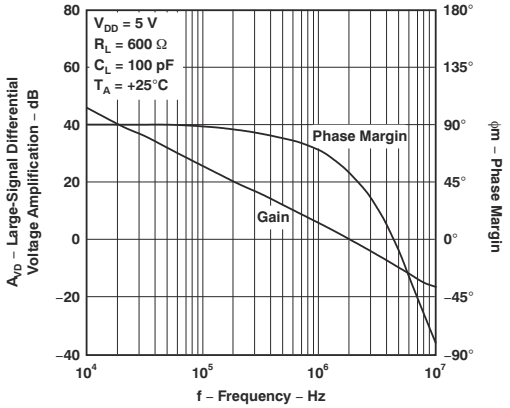
Load referenced to 2.5V

Figure 6-12. Short-Circuit Output Current vs Free-Air Temperature



Load referenced to 1.5V

Figure 6-13. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

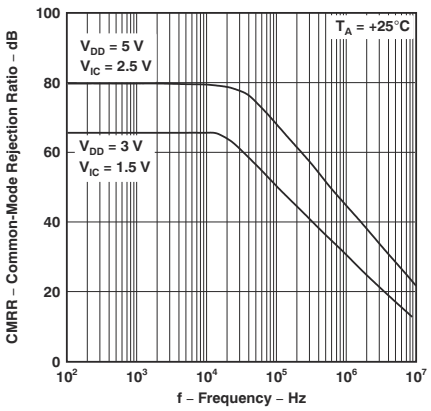


Load referenced to 2.5V

Figure 6-14. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

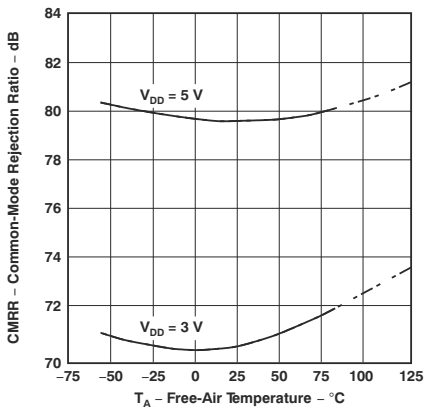
6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices



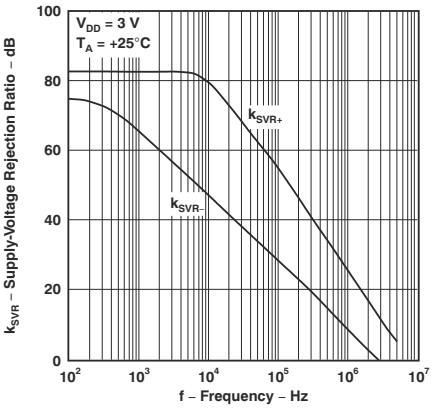
For V_{DD} = 3V, load referenced to 1.5V, for V_{DD} = 5V, load referenced to 2.5V

Figure 6-15. Common-Mode Rejection Ratio vs Frequency



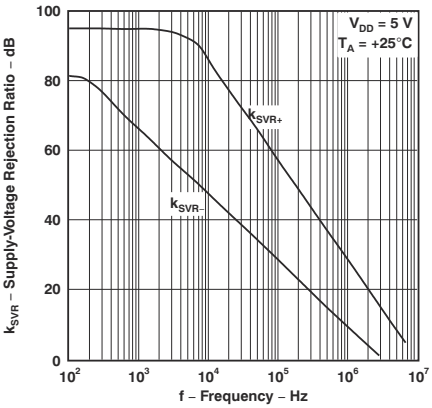
For V_{DD} = 3V, load referenced to 1.5V, for V_{DD} = 5V, load referenced to 2.5V

Figure 6-16. Common-Mode Rejection Ratio vs Free-Air Temperature



Load referenced to 1.5V

Figure 6-17. Supply-Voltage Rejection Ratio vs Frequency



Load referenced to 2.5V

Figure 6-18. Supply-Voltage Rejection Ratio vs Frequency

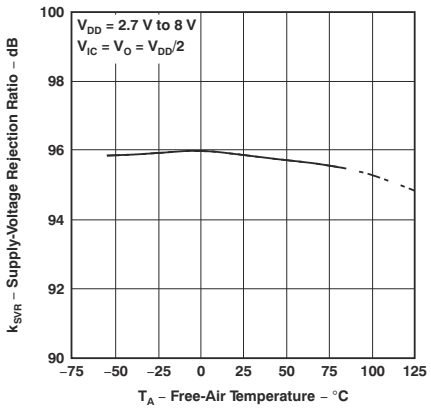


Figure 6-19. Supply-Voltage Rejection Ratio vs Free-Air Temperature

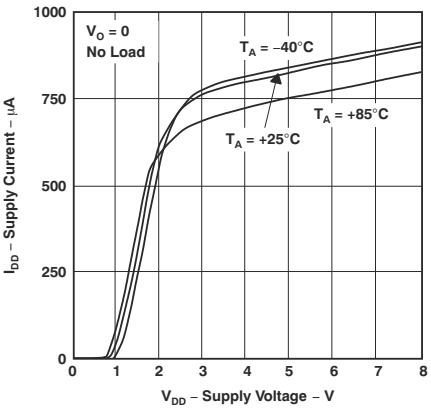


Figure 6-20. Supply Current vs Supply Voltage

6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

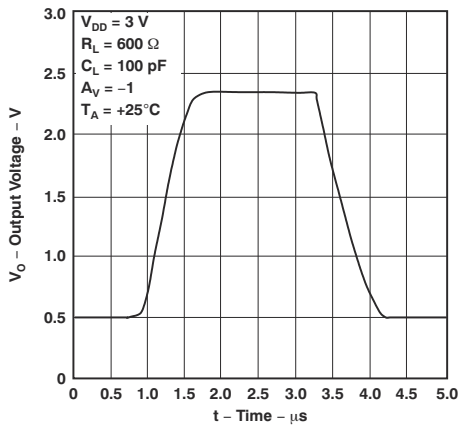
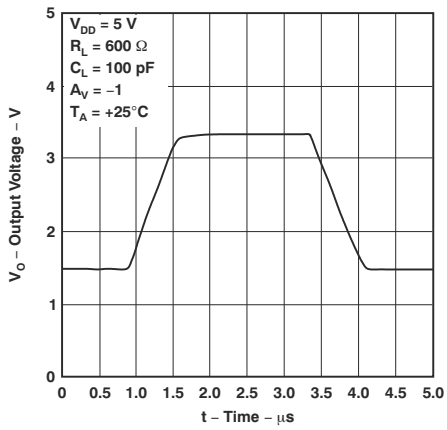
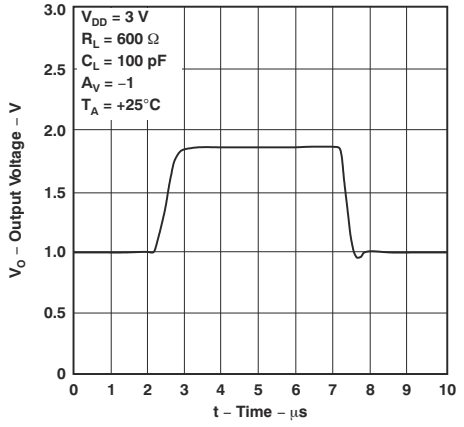


Figure 6-21. Inverting Large-Signal Pulse Response



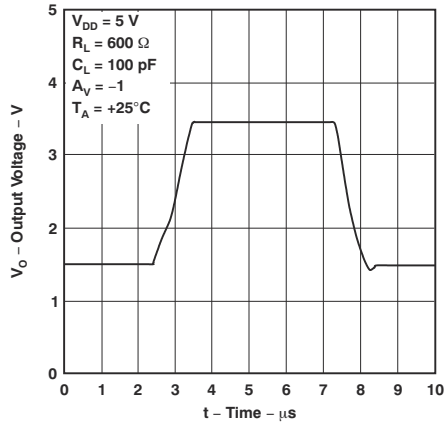
Load referenced to 2.5V

Figure 6-22. Inverting Large-Signal Pulse Response



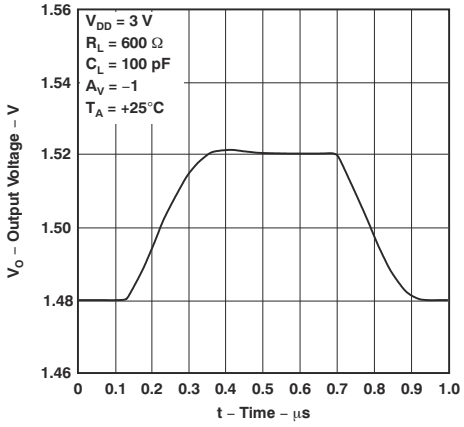
Load referenced to 1.5V

Figure 6-23. Voltage-Follower Large-Signal Pulse Response



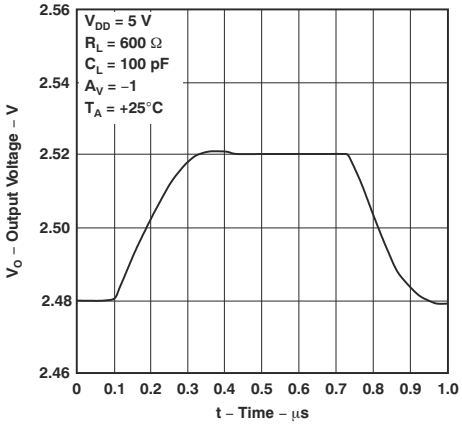
Load referenced to 2.5V

Figure 6-24. Voltage-Follower Large-Signal Pulse Response



Load referenced to 1.5V

Figure 6-25. Inverting Small-Signal Pulse Response

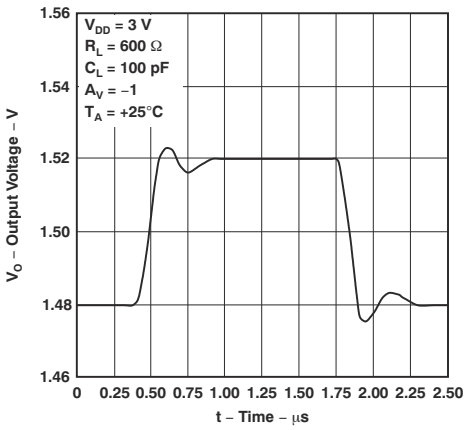


Load referenced to 2.5V

Figure 6-26. Inverting Small-Signal Pulse Response

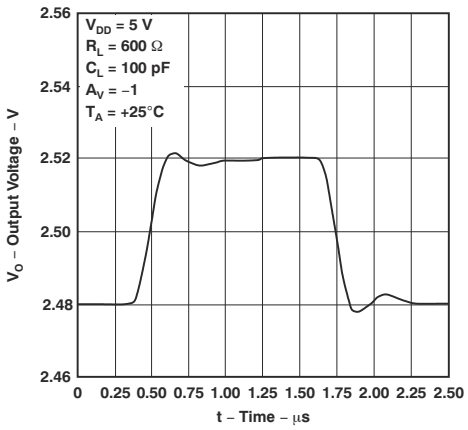
6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices



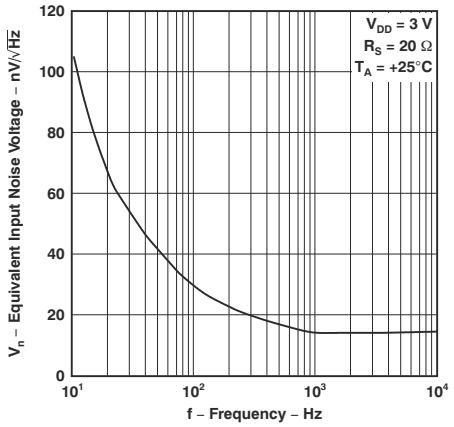
Load referenced to 1.5V

Figure 6-27. Voltage-Follower Small-Signal Pulse Response



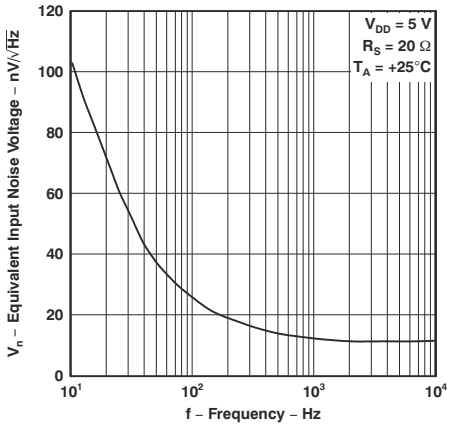
Load referenced to 2.5V

Figure 6-28. Voltage-Follower Small-Signal Pulse Response



Load referenced to 1.5V

Figure 6-29. Equivalent Input Noise Voltage vs Frequency



Load referenced to 2.5V

Figure 6-30. Equivalent Input Noise Voltage vs Frequency

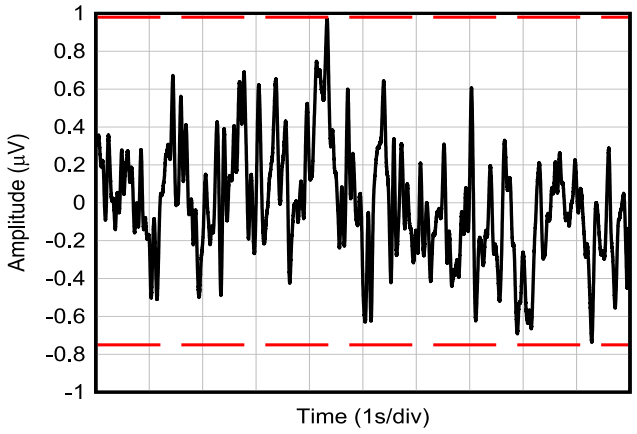
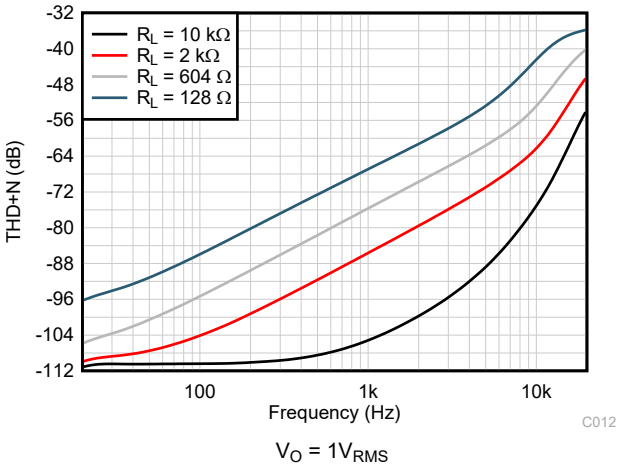


Figure 6-31. Input Noise Voltage Over a 10-Second Period



V_O = 1V_{RMS}

Figure 6-32. Total Harmonic Distortion Plus Noise vs Frequency

6.8 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

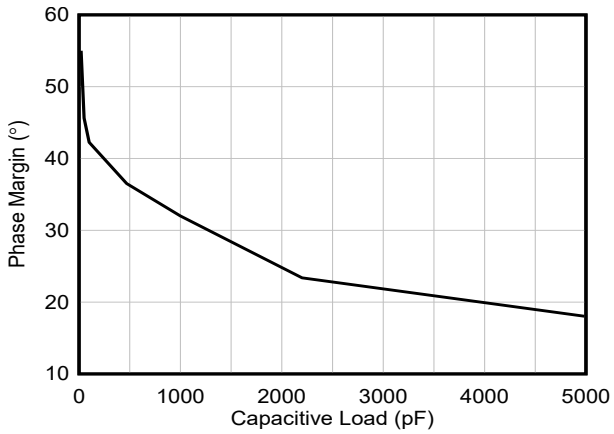


Figure 6-33. Phase Margin vs Load Capacitance

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving Large Capacitive Loads

The TLV2231 features a resistive output stage capable of driving moderate capacitive loads. By leveraging an isolation resistor, the device is easily configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 7-1 and Figure 7-2. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

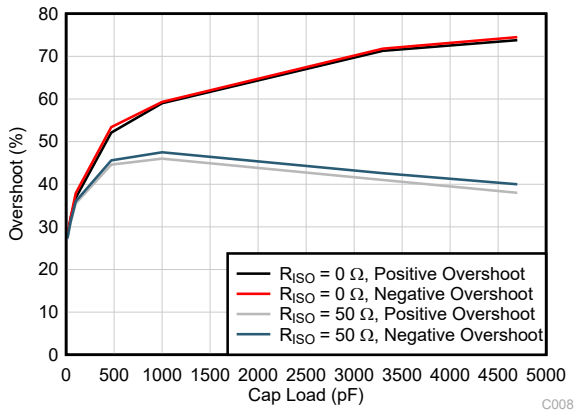


Figure 7-1. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = 1)

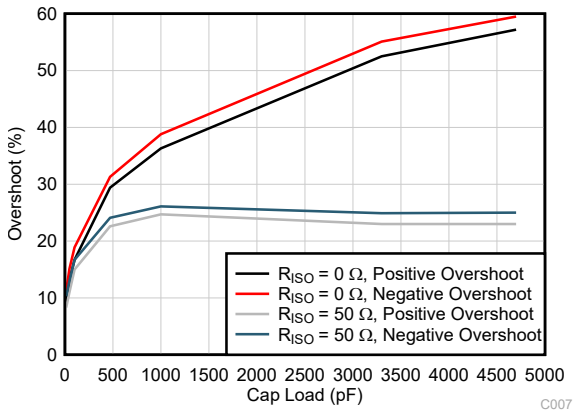


Figure 7-2. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output; see Figure 7-3. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created. Thus a gain error is introduced at the output and a slight reduction the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is typically negligible at low output levels. A high capacitive load drive makes the TLV2231 an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit in Figure 7-3 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

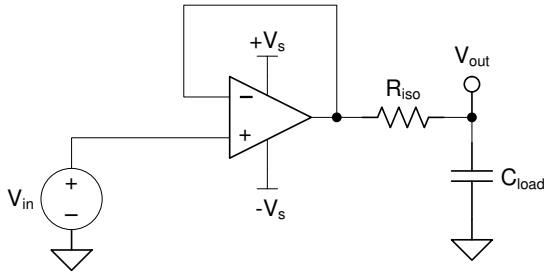


Figure 7-3. Extending Capacitive Load Drive With the TLV2231

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2001) to Revision E (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Applications*, *Pin Configuration and Functions*, *Specifications*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Deleted TLV2231Y device and associated content from data sheet	1
• Deleted "Macromodel Included" from *Features*	1
• Deleted equivalent schematic	2
• Deleted input offset voltage long-term drift and associated table note	4
• Deleted common-mode input voltage range typical value	4
• Deleted common-mode input voltage range for full temperature range	4
• Changed differential input resistance typical value from $10^{12}\Omega$ to 540GΩ	4
• Changed unit of common-mode input resistance from $10^{12}\Omega$ to 1TΩ	4
• Changed common-mode input capacitance typical value from 6pF to 1pF	4
• Changed output impedance from closed-loop to open-loop	4
• Changed output impedance test condition from A_V = 1 to I_O = 0A	4
• Changed output impedance from 156Ω to 525Ω	4
• Changed CMRR minimum value for room temperature from 60dB to 54dB	4
• Changed CMRR minimum value for full temperature range from 55dB to 54dB	4
• Added table note 2 to input bias current and input offset current	4
• Changed slew rate typical value for room temperature from 1.25V/µs to 0.25V/µs	5

- Changed slew rate minimum value for room temperature from 0.75V/µs to 0.24V/µs....5
- Changed slew rate minimum value for full temperature range from 0.5V/µs to 0.24V/µs....5
- Deleted equivalent input noise voltage for f = 10Hz....5
- Deleted peak-to-peak equivalent input noise voltage for f = 0.1Hz to 1Hz....5
- Changed peak-to-peak equivalent input noise voltage for f = 0.1Hz to 10Hz from 1.5µV to 1.8µV....5
- Changed equivalent input noise current typical value from 0.6fA/$\sqrt{Hz}$ to 2fA/$\sqrt{Hz}$ 5
- Deleted THD+N test conditions and changed values to "see *Typical Characteristics*"....5
- Deleted settling time....5
- Deleted gain margin....5
- Deleted input offset voltage long-term drift and associated table note....6
- Deleted common-mode input voltage range typical value....6
- Deleted common-mode input voltage range for full temperature range....6
- Changed differential input resistance typical value from $10^{12}\Omega$ to 540GΩ....6
- Changed common-mode input resistance from $10^{12}\Omega$ to 1TΩ....6
- Changed common-mode input capacitance from 6pF to 1pF....6
- Changed output impedance from closed-loop to open-loop....6
- Changed output impedance test condition from A_V = 1 to I_O = 0A....6
- Changed output impedance typical value from 138Ω to 525Ω....6
- Added table note to input bias current and input offset current....6
- Deleted equivalent input noise voltage for f = 10Hz....7
- Deleted peak-to-peak equivalent input noise voltage for f = 0.1Hz to 1Hz....7
- Changed peak-to-peak equivalent input noise voltage for f = 0.1Hz to 10Hz from 1.5µV to 1.8µV....7
- Changed equivalent input noise current typical value from 0.6fA/$\sqrt{Hz}$ to 2fA/$\sqrt{Hz}$ 7
- Deleted THD+N test conditions and changed values to "see *Typical Characteristics*"....7
- Deleted settling time....7
- Deleted gain margin....7
- Deleted Figures 9, 10, 12, 16, 17, 19–21, 24–27, 34, 35, 48–55, ...8
- Updated Figure 6-31, 6-32, and 6-33....8
- Updated *Driving Large Capacitive Loads* section....15
- Deleted *Macromodel Information* section....15

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2231IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VAEI
TLV2231IDBVR.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TLV2231IDBVR	VAEI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

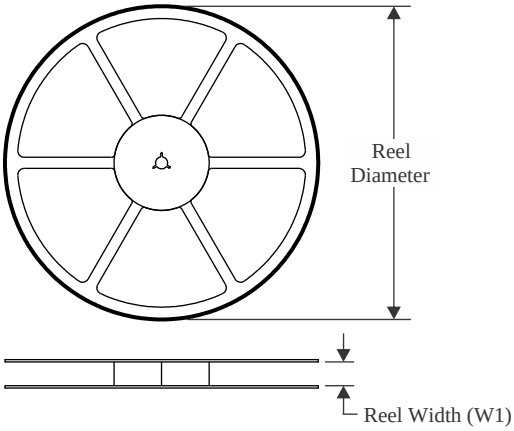
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

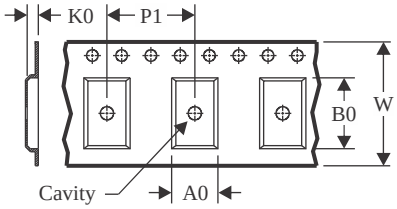
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

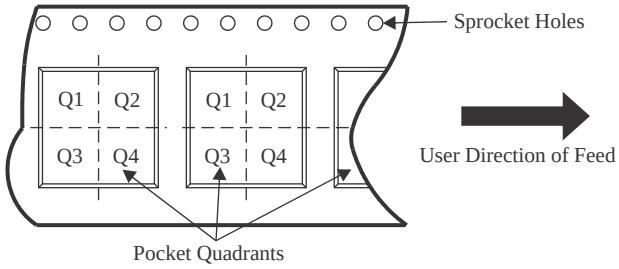


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

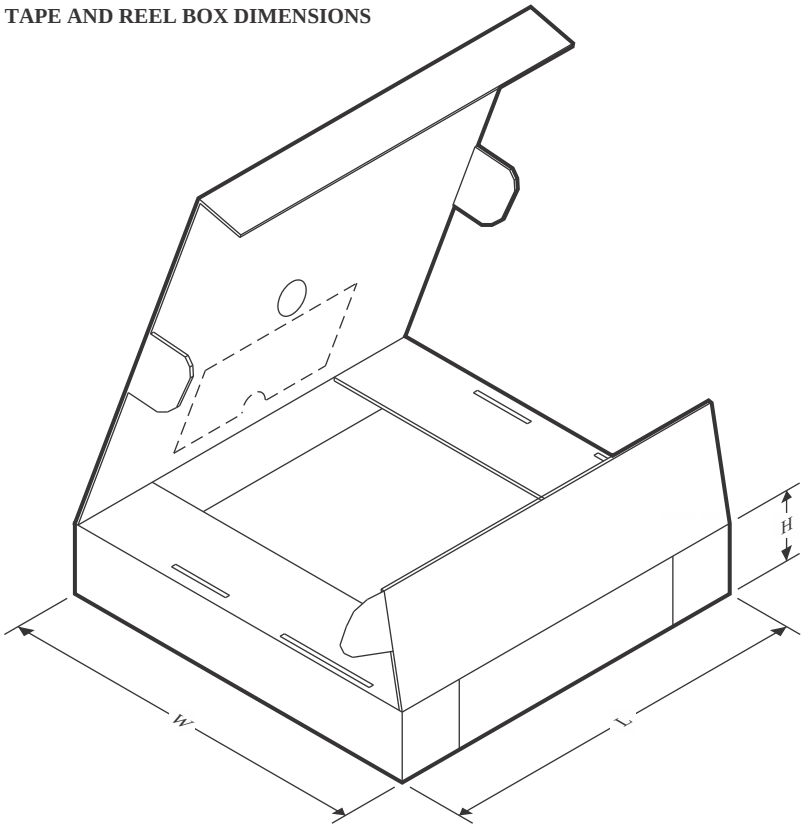
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2231IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

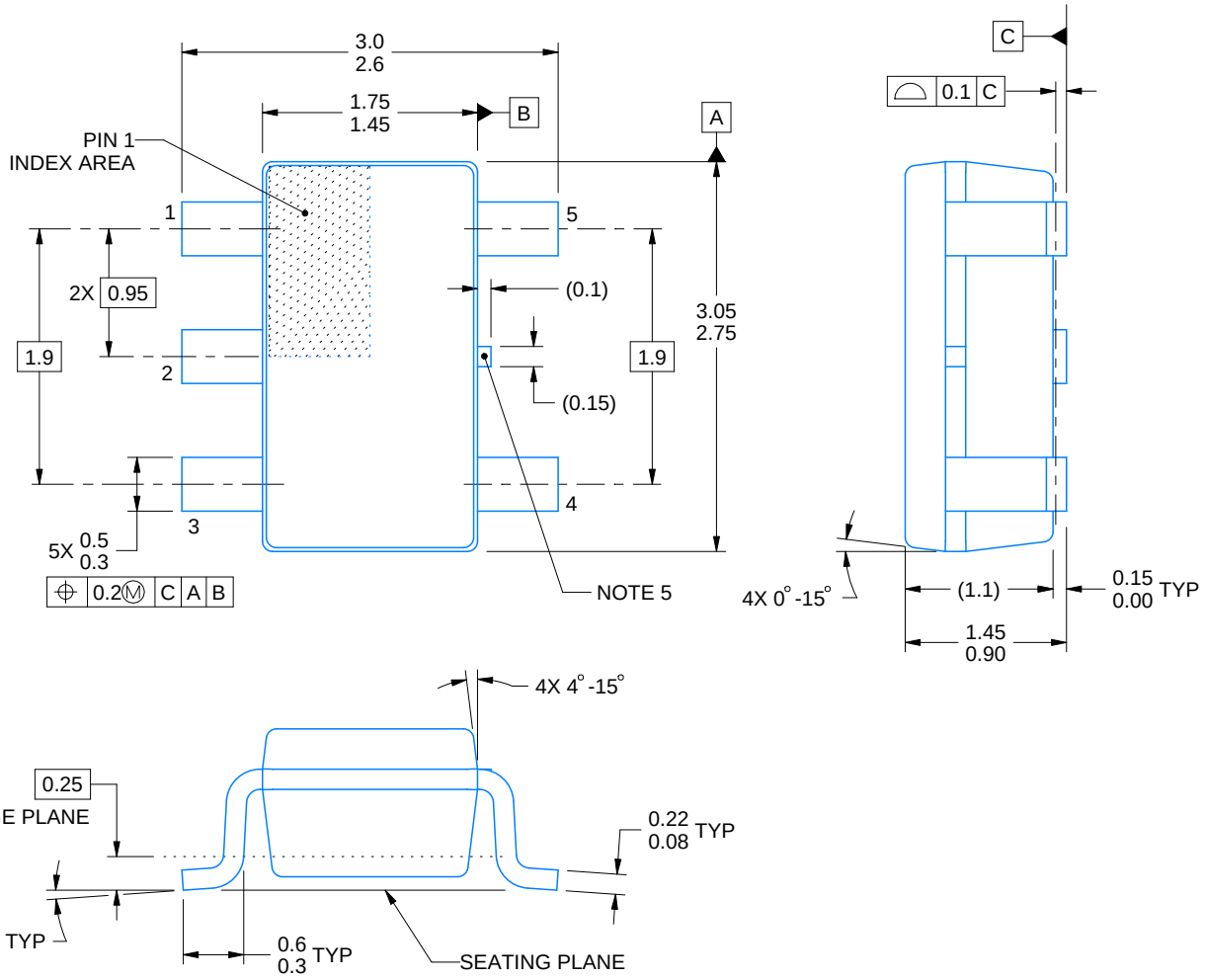
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2231IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

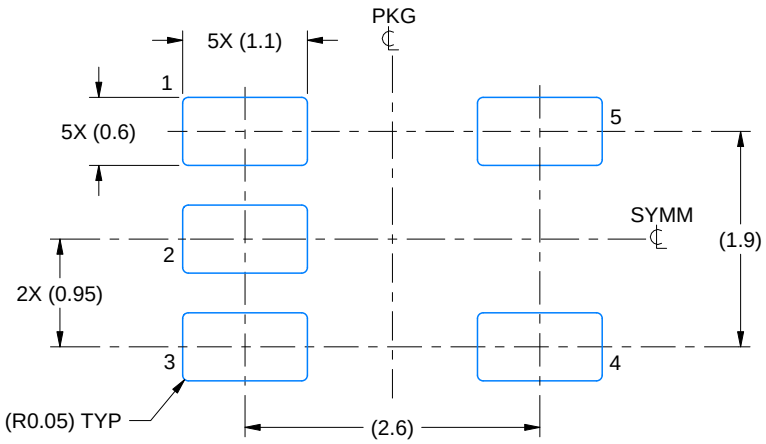
SMALL OUTLINE TRANSISTOR



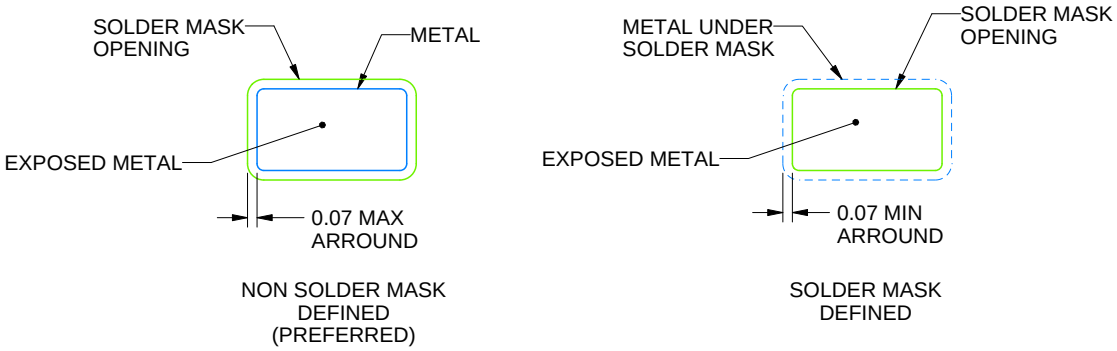
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

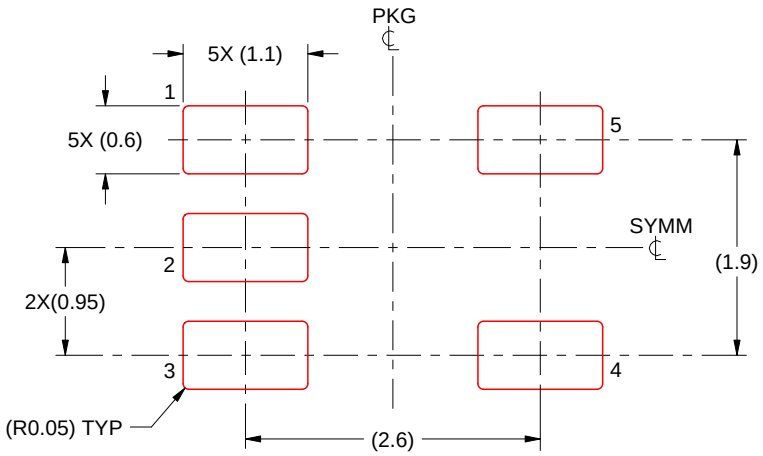


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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