- **Qualified for Automotive Applications**
- **Direct Upgrades to TL05x, TL07x, and TL08x BiFET Operational Amplifiers**
- **Greater Than 2× Bandwidth (10 MHz) and 3× Slew Rate (45 V/μs) Than TL07x**
- **Ensured Maximum Noise Floor 17 nV/√Hz**
- **On-Chip Offset Voltage Trimming for Improved DC Performance**
- **Wider Supply Rails Increase Dynamic Signal Range to ±19 V**

description/ordering information

The TLE207x series of JFET-input operational amplifiers more than double the bandwidth and triple the slew rate of the TL07x and TL08x families of BiFET operational amplifiers. Texas Instruments Excalibur process yields a typical noise floor of 11.6 nV/√Hz, 17-nV/√Hz ensured maximum, offering immediate improvement in noise-sensitive circuits designed using the TL07x. The TLE207x also has wider supply voltage rails, increasing the dynamic signal range for BiFET circuits to ±19 V. On-chip zener trimming of offset voltage yields precision grades for greater accuracy in dc-coupled applications. The TLE207x are pin-compatible with lower performance BiFET operational amplifiers for ease in improving performance in existing designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or very low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TLE207x family of BiFET amplifiers are Texas Instruments highest performance BiFETs, with tighter input offset voltage and ensured maximum noise specifications. Designers requiring less stringent specifications but seeking the improved ac characteristics of the TLE207x should consider the TLE208x operational amplifier family.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

ORDERING INFORMATION†

T_A	V_{IO}max AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	2 mV	SOIC – D	Tape and reel	TLE2071AQDRQ1	2071AQ
	4 mV	SOIC – D	Tape and reel	TLE2071QDRQ1	2071Q1
	3.5 mV	SOIC – D	Tape and reel	TLE2072AQDRQ1	2072AQ
	6 mV	SOIC – D	Tape and reel	TLE2072QDRQ1	2072Q1
	4 mV	SOP – DW	Tape and reel	TLE2074AQDWRQ1§	TLE2074AQ1
	7 mV	SOP – DW	Tape and reel	TLE2074QDWRQ1§	TLE2074Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

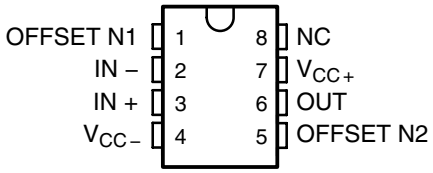
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

§ Product Preview

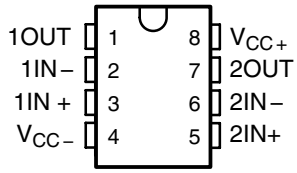
description/ordering information (continued)

The TLE207x are fully specified at ±15 V and ±5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC- and TLV-prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate and bandwidth requirements and output loading.

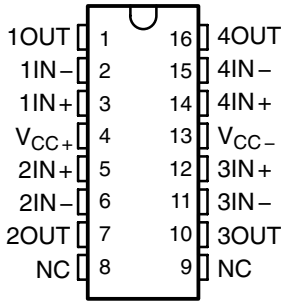
TLE2071 AND TLE2071A
D PACKAGE
(TOP VIEW)



TLE2072 AND TLE2072A
D PACKAGE
(TOP VIEW)

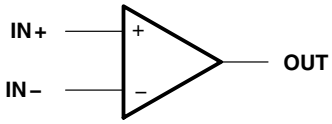


TLE2074 AND TLE2074A
DW PACKAGE
(TOP VIEW)

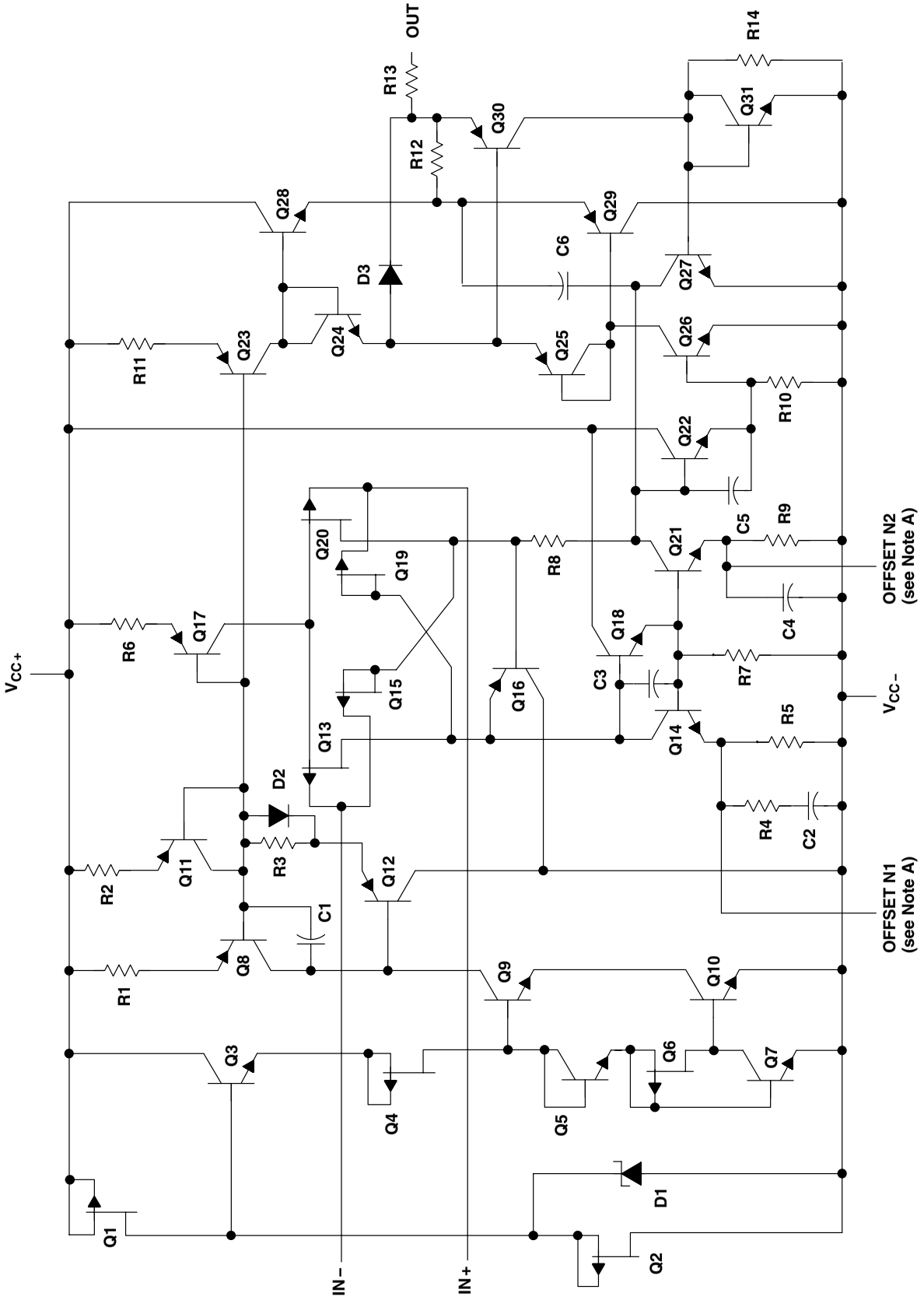


NC – No internal connection

symbol



equivalent schematic



NOTES: A. OFFSET N1 AND OFFSET N2 are only availiable on the TLE2071x devices.

equivalent schematic (continued)

ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	**TLE2071**	**TLE2072**	**TLE2074**
Transistors	33	57	114
Resistors	25	37	74
Diodes	8	5	10
Capacitors	6	11	22

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 19 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –19 V
Differential input voltage range, V_{ID} (see Note 2) . . . . . V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) . . . . . V_{CC+} to V_{CC-}
Input current, I_I (each input) . . . . . ±1 mA
Output current, I_O (each output) . . . . . ±80 mA
Total current into V_{CC+} . . . . . 160 mA
Total current out of V_{CC-} . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Maximum Junction Temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Note 4): D package . . . . . 126°C/W
DW package . . . . . 75°C/W
Operating free-air temperature range, T_A: Q suffix . . . . . –40°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 3 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	–0.8	5	V
	$V_{CC\pm}$ = ±15 V	–10.8	15	
Operating free-air temperature, T_A		–40	125	°C

TLE2071-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.34	4		0.3	2	mV
				Full range			9			7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2			3.2	20	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			60			60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.3			−3.3			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is −40°C to 125°C.

TLE2071-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		–35			–35		mA
			V_{ID} = –1 V			45			45		

† Full range is –40°C to 125°C.

TLE2071-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = –1, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		25°C		35			35		V/μs
				Full range	20			20			
SR–	Negative slew rate			25°C		38			38		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = –1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ ,	A_{VD} = –1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56			56		

† Full range is –40°C to 125°C.

TLE2071-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.49	4		0.47	2	mV
				Full range			9			7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2			3.2	20	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			60			60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is −40°C to 125°C.

TLE2071-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–30	–45		–30	–45		mA
			V_{ID} = –1 V		30	48		30	48		

† Full range is –40°C to 125°C.

TLE2071-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071-Q1			TLE2071A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = –1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	22			22			
SR–	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = –1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = –1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57			57		

† Full range is –40°C to 125°C.

TLE2072-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.9	6		0.65	3.5	mV
				Full range			10			8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3			2.3	20	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			60			60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.3			−3.3			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			

† Full range is −40°C to 125°C.

TLE2072-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0,	R_S = 50 Ω	Full range	80			80			dB
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		–35			–35		mA
			V_{ID} = –1 V			45			45		

† Full range is –40°C to 125°C.

TLE2072-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = –1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18			18			
SR–	Negative slew rate			25°C		38			38		V/μs
				Full range	18			18			
t_s	Settling time	A_{VD} = –1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ ,	A_{VD} = –1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56			56		

† Full range is –40°C to 125°C.

TLE2072-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	6		0.7	3.5	mV
				Full range			10			8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4			2.4	20	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			60			60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is −40°C to 125°C.

TLE2072-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–30	–45		–30	–45		mA
			V_{ID} = –1 V		30	48		30	48		

† Full range is –40°C to 125°C.

TLE2072-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072-Q1			TLE2072A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = –1, C_L = 100 pF,	25°C	28	40		28	40		V/μs
				Full range	20			20			
SR–	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = –1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = –1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57			57		

† Full range is –40°C to 125°C.

TLE2074-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50Ω		25°C		–1.6	7		–0.5	4	mV
					Full range			11			9	
α_{VIO}	Temperature coefficient of input offset voltage				Full range		10.1			10.1	30	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
					Full range			20			20	nA
I_{IB}	Input bias current				25°C		20	175		20	175	pA
					Full range			60			60	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	5 to –1	5 to –1.9		5 to –1	5 to –1.9		V
					Full range	5 to –0.8			5 to –0.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = –200 µA		25°C	3.8	4.1		3.8	4.1		V
					Full range	3.6			3.6			
			I_O = –2 mA		25°C	3.5	3.9		3.5	3.9		
					Full range	3.3			3.3			
			I_O = –20 mA		25°C	1.5	2.3		1.5	2.3		
					Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	–3.8	–4.2		–3.8	–4.2		V
					Full range	–3.6			–3.6			
			I_O = 2 mA		25°C	–3.5	–4.1		–3.5	–4.1		
					Full range	–3.3			–3.3			
			I_O = 20 mA		25°C	–1.5	–2.4		–1.5	–2.4		
					Full range	–1.4			–1.4			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
					Full range	78			78			
				R_L = 2 kΩ	25°C	90	100		90	100		
					Full range	88			88			
				R_L = 10 kΩ	25°C	95	106		95	106		
					Full range	93			93			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
					Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			

† Full range is –40°C to 125°C.

TLE2074-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		–35			–35		mA
			V_{ID} = –1 V			45			45		

† Full range is –40°C to 125°C.

TLE2074-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = –1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18			18			
SR–	Negative slew rate			25°C		38			38		V/μs
				Full range	18			18			
t_s	Settling time	A_{VD} = –1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = –1, C_L = 25 pF	25°C		2.8			2.8		MHz
f_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56			56		

† Full range is –40°C to 125°C.

TLE2074-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	7		–0.5	4	mV
					Full range			11			9	
α_{VIO}	Temperature coefficient of input offset voltage				Full range		10.1			10.1	30	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
					Full range			20			20	nA
I_{IB}	Input bias current				25°C		25	175		25	175	pA
					Full range			60			60	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	15 to –11	15 to –11.9		15 to –11	15 to –11.9		V
					Full range	15 to –10.8			15 to –10.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = –200 µA		25°C	13.8	14.1		13.8	14.1		V
					Full range	13.6			13.6			
			I_O = –2 mA		25°C	13.5	13.9		13.5	13.9		
					Full range	13.3			13.3			
			I_O = –20 mA		25°C	11.5	12.3		11.5	12.3		
					Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	–13.8	–14.2		–13.8	–14.2		V
					Full range	–13.6			–13.6			
			I_O = 2 mA		25°C	–13.5	–14		–13.5	–14		
					Full range	–13.3			–13.3			
			I_O = 20 mA		25°C	–11.5	–12.4		–11.5	–12.4		
					Full range	–11.4			–11.4			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
					Full range	78			78			
				R_L = 2 kΩ	25°C	90	109		90	109		
					Full range	88			88			
				R_L = 10 kΩ	25°C	95	118		95	118		
					Full range	93			93			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		7.5			7.5		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
					Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			

† Full range is –40°C to 125°C.

TLE2074-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–30	–45		–30	–45		mA
			V_{ID} = –1 V		30	48		30	48		

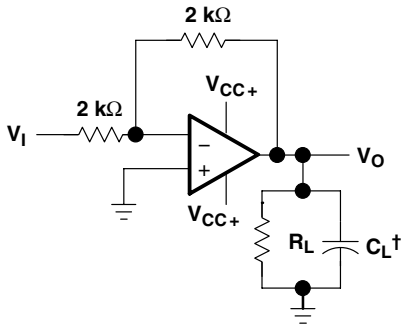
† Full range is –40°C to 125°C.

TLE2074-Q1 operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074-Q1			TLE2074A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = –1, C_L = 100 pF,	25°C	25	40		25	40		V/μs
				Full range	17			17			
SR–	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = –1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = –1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57			57		

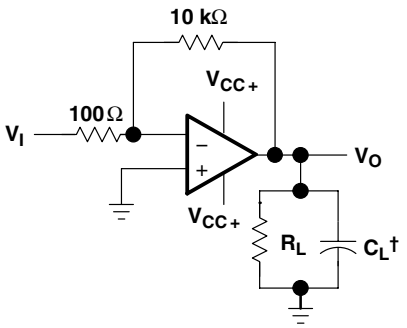
† Full range is –40°C to 125°C.

PARAMETER MEASUREMENT INFORMATION



† Includes fixture capacitance

Figure 1. Slew-Rate Test Circuit



† Includes fixture capacitance

Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

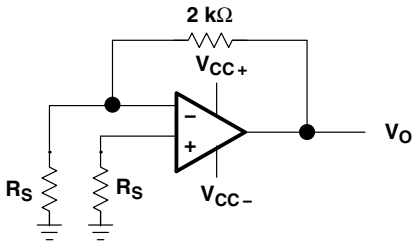


Figure 3. Noise-Voltage Test Circuit

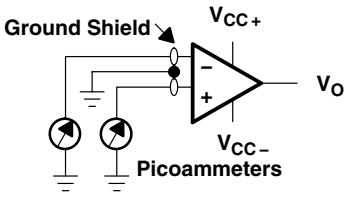


Figure 4. Input-Bias and Offset-Current Test Circuit

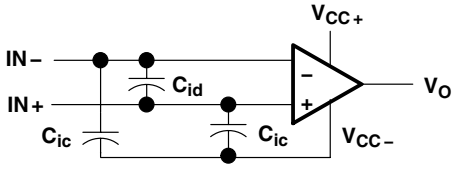


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE207x and TLE207xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7, 8
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	9, 10, 11
I_{IO}	Input offset current	vs Free-air temperature	12, 13
I_{IB}	Input bias current	vs Free-air temperature vs Total supply voltage	12, 13 14
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	15
V_O	Output voltage	vs Differential input voltage	16, 17
V_{OM+}	Maximum positive peak output voltage	vs Output current	18
V_{OM-}	Maximum negative peak output voltage	vs Output current	19
V_{OM}	Maximum peak output voltage	vs Free-air temperature vs Supply voltage	20, 21 22
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
V_O	Output voltage	vs Settling time	24
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Free-air temperature	25 26, 27
A_{VD}	Small-signal differential voltage amplification	vs Frequency	28, 29
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	30 31
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	32 33
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	34, 35, 36 37, 38, 39 40 – 45
I_{OS}	Short-circuit output current	vs Supply voltage vs Elapsed time vs Free-air temperature	46 47 48
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	49, 50 51 52
V_n	Equivalent Input noise voltage (spectral density)	vs Frequency	53
V_n	Input referred noise voltage	vs Noise bandwidth Over a 10-second time interval	54 55
	Third-octave spectral noise density	vs Frequency bands	56
THD + N	Total harmonic distortion plus noise	vs Frequency	57, 58
B_1	Unity-gain bandwidth	vs Load capacitance	59
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	60 61
	Gain margin	vs Load capacitance	62
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	63 64 65
	Phase shift	vs Frequency	28, 29
	Noninverting large-signal pulse response	vs Time	66
	Small-signal pulse response	vs Time	67
z_o	Closed-loop output impedance	vs Frequency	68
	Crosstalk attenuation	vs Frequency	69

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLE2071 INPUT OFFSET VOLTAGE

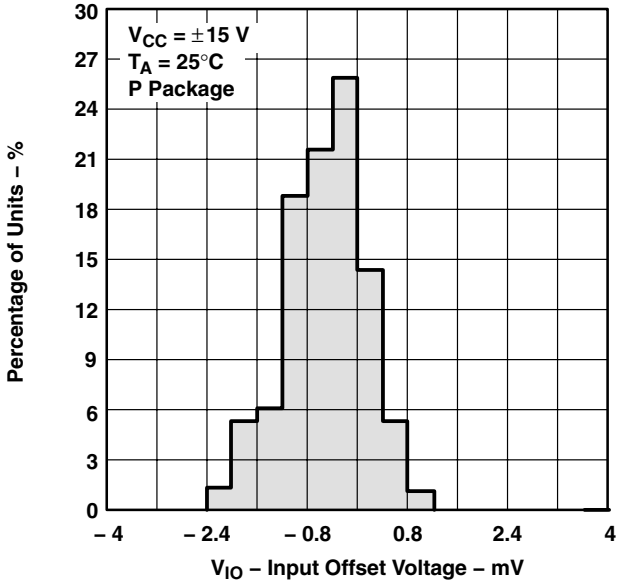


Figure 6

DISTRIBUTION OF TLE2072 INPUT OFFSET VOLTAGE

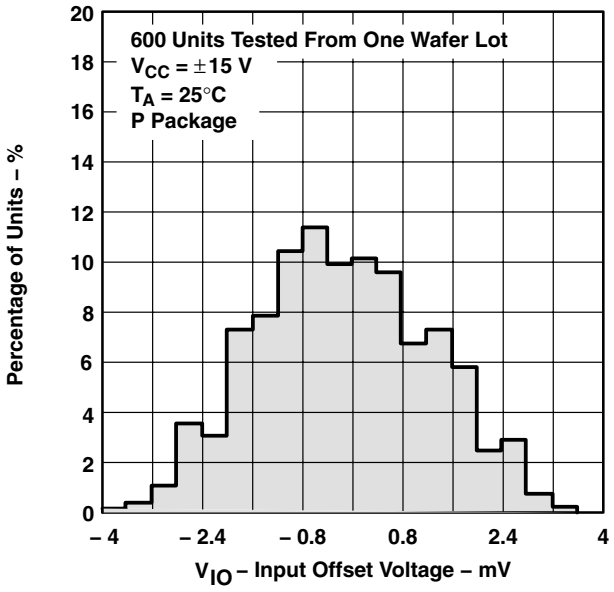


Figure 7

DISTRIBUTION OF TLE2074 INPUT OFFSET VOLTAGE

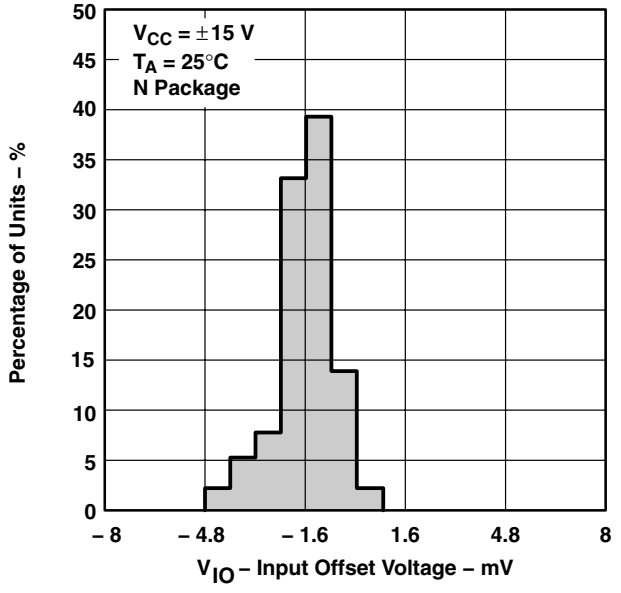


Figure 8

DISTRIBUTION OF TLE2071 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

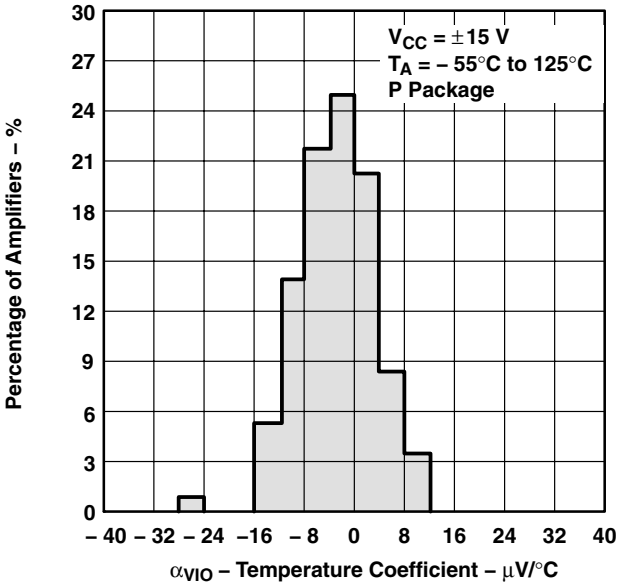


Figure 9

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLE2072 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

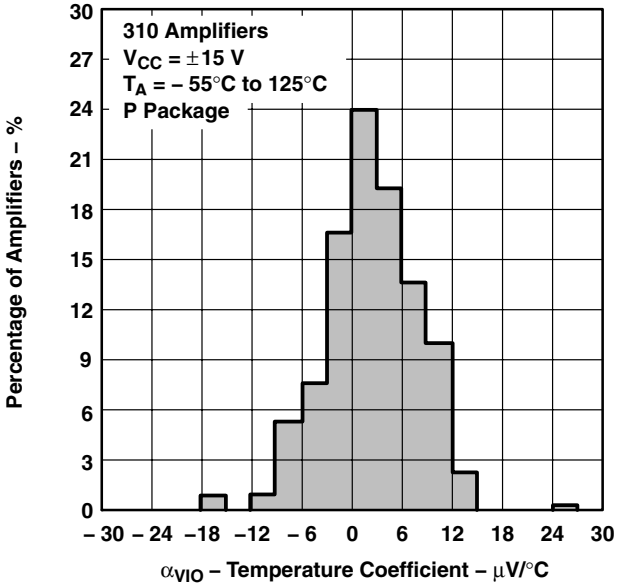


Figure 10

DISTRIBUTION OF TLE2074 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

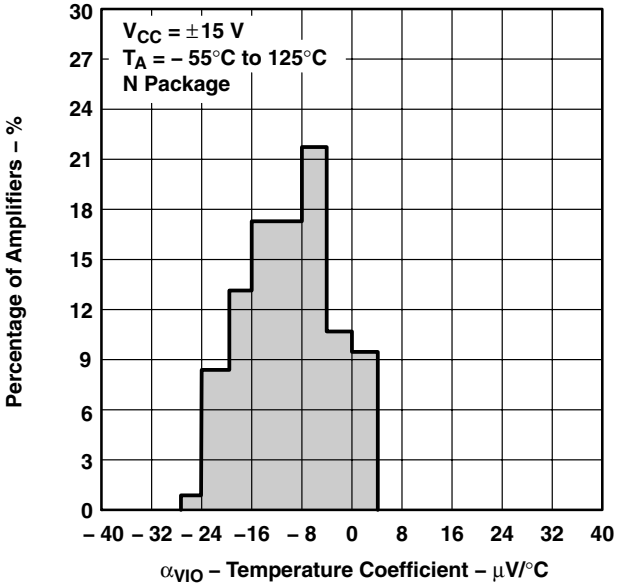


Figure 11

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT† vs FREE-AIR TEMPERATURE

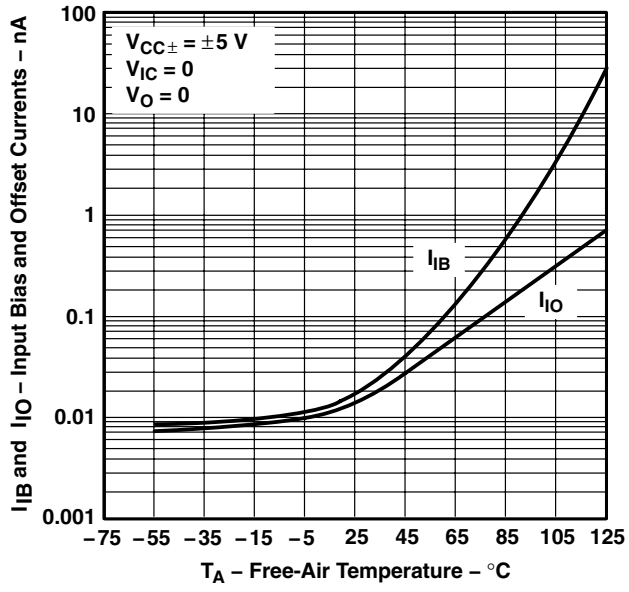


Figure 12

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT† vs FREE-AIR TEMPERATURE

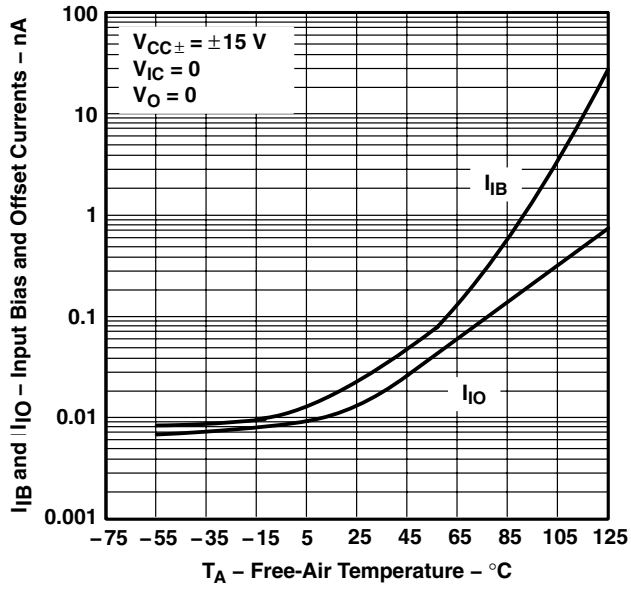


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs TOTAL SUPPLY VOLTAGE

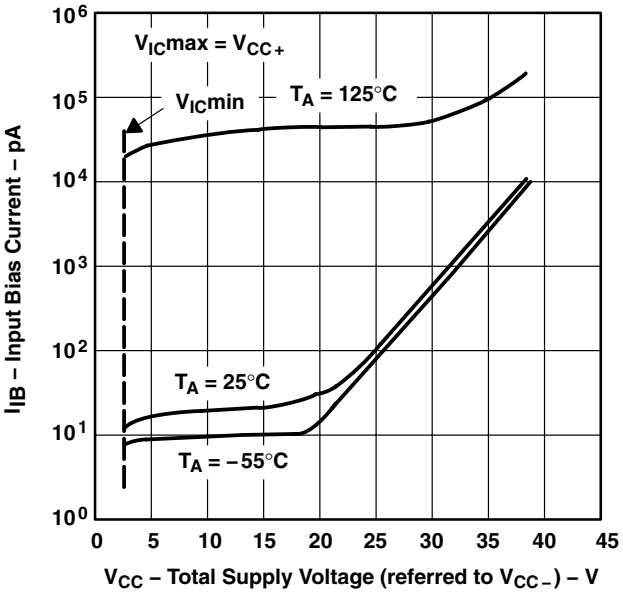


Figure 14

COMMON-MODE INPUT VOLTAGE RANGE† vs FREE-AIR TEMPERATURE

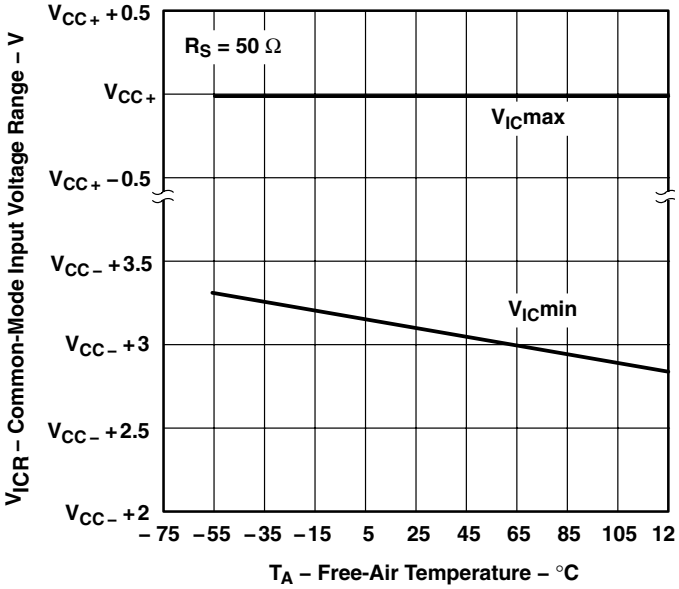


Figure 15

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

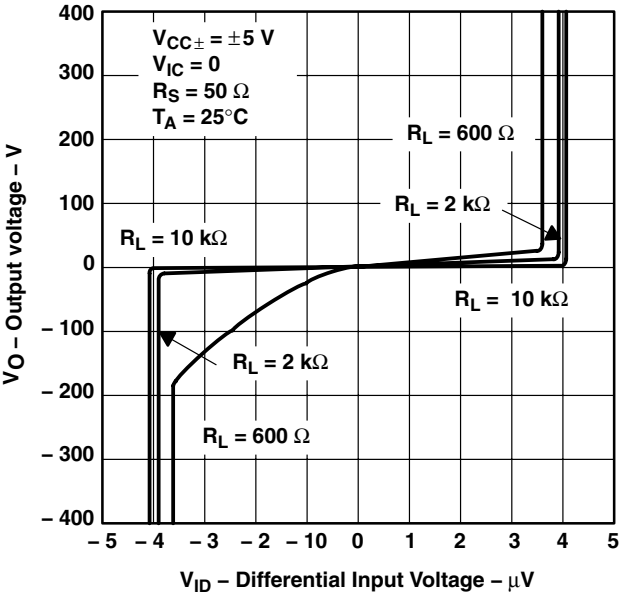


Figure 16

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

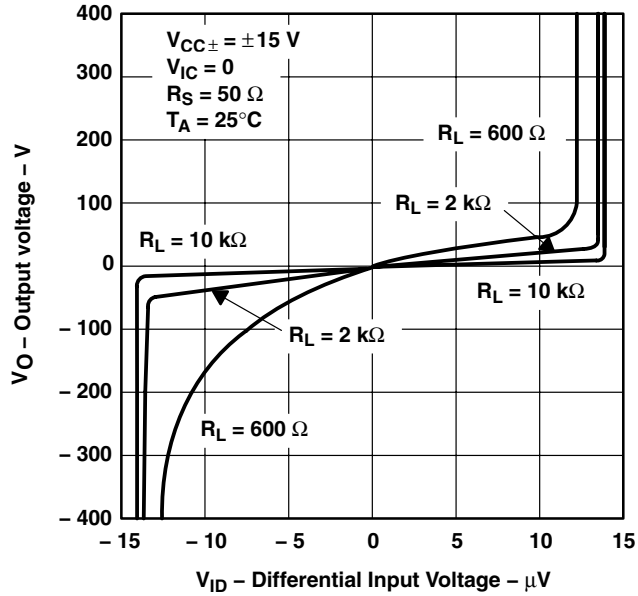


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

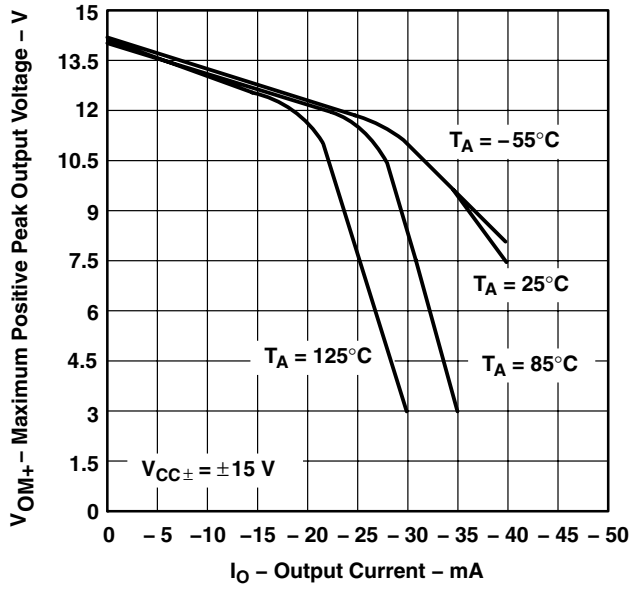


Figure 18

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

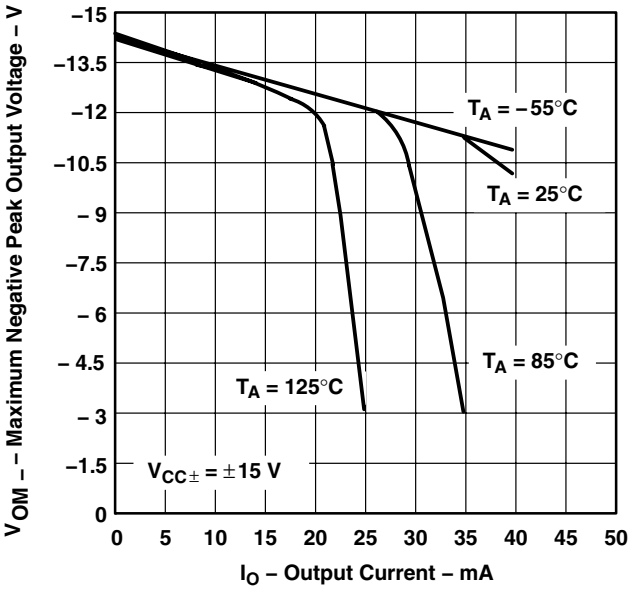


Figure 19

MAXIMUM PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

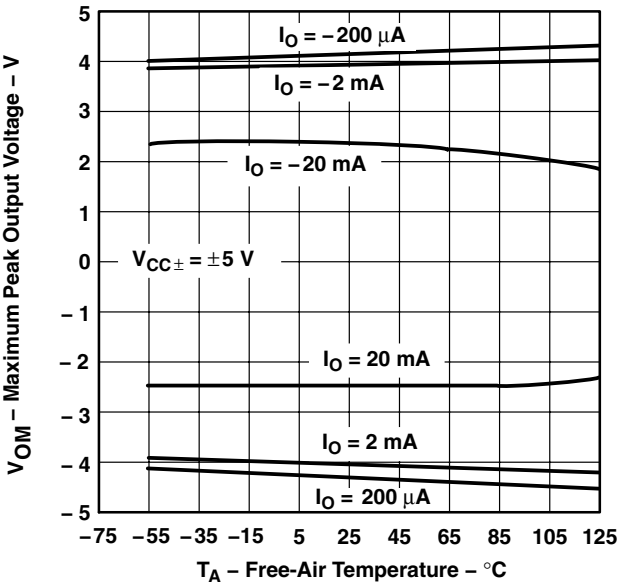


Figure 20

MAXIMUM PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

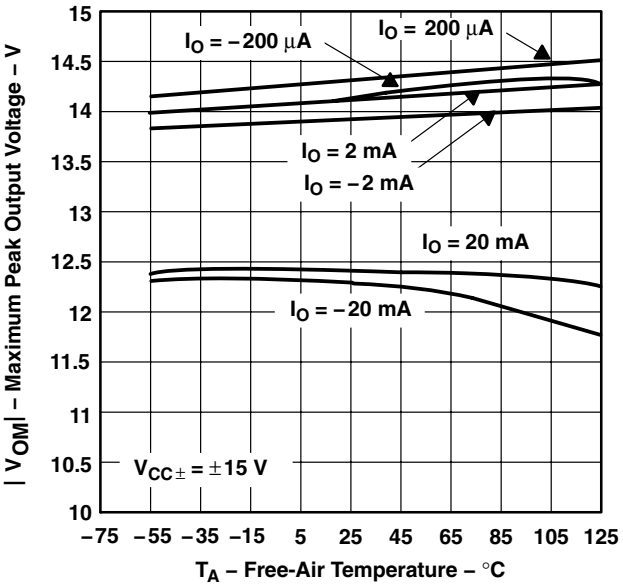


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

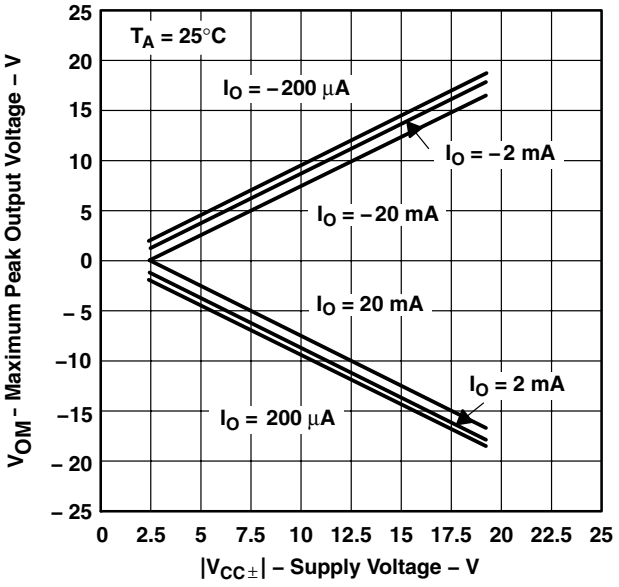


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE† vs FREQUENCY

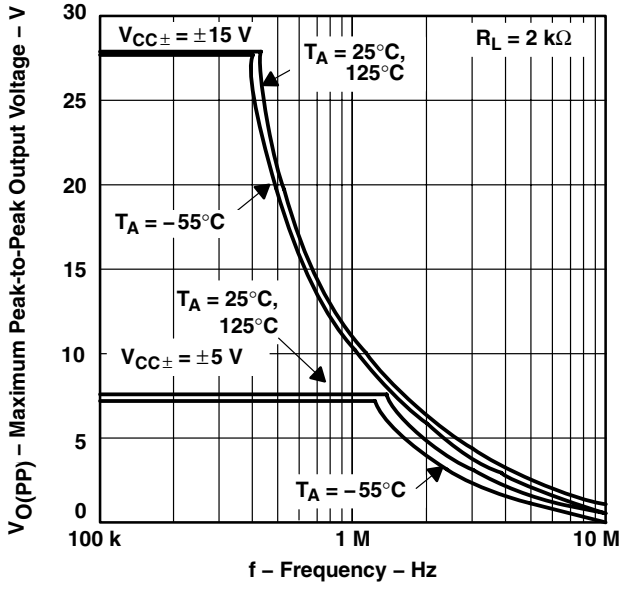


Figure 23

OUTPUT VOLTAGE vs SETTLING TIME

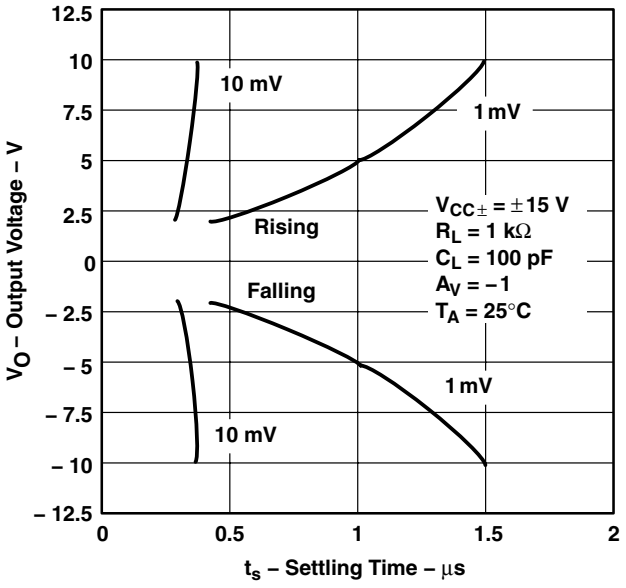


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

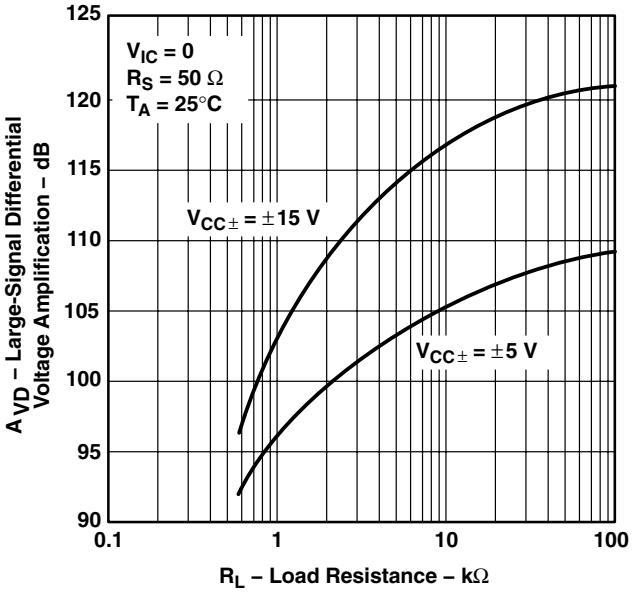


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

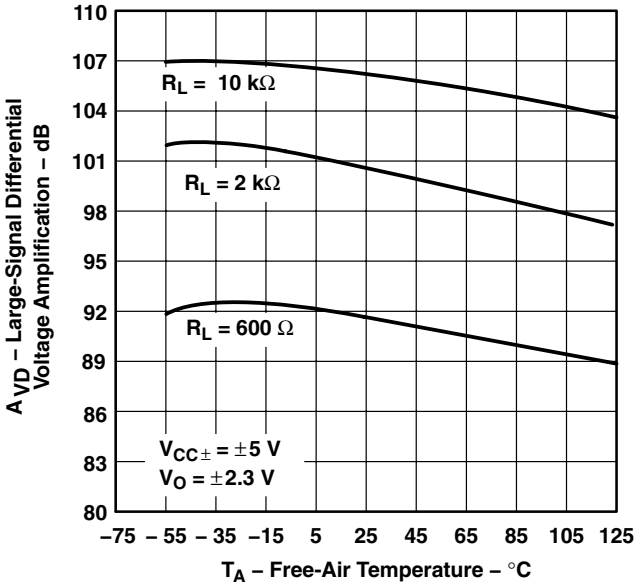


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

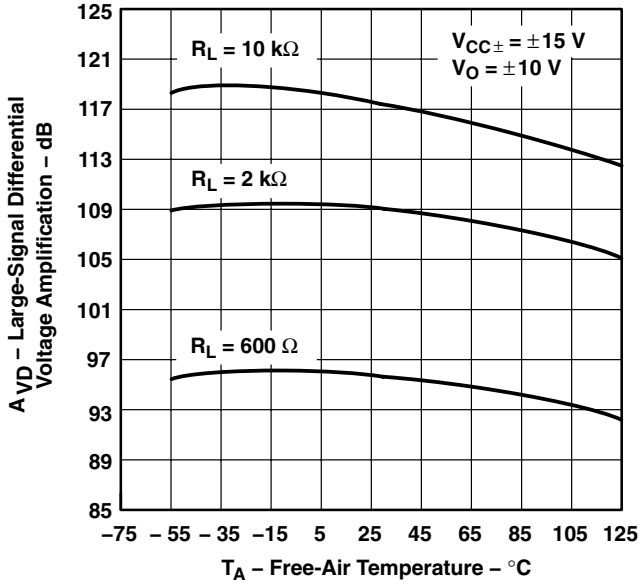


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

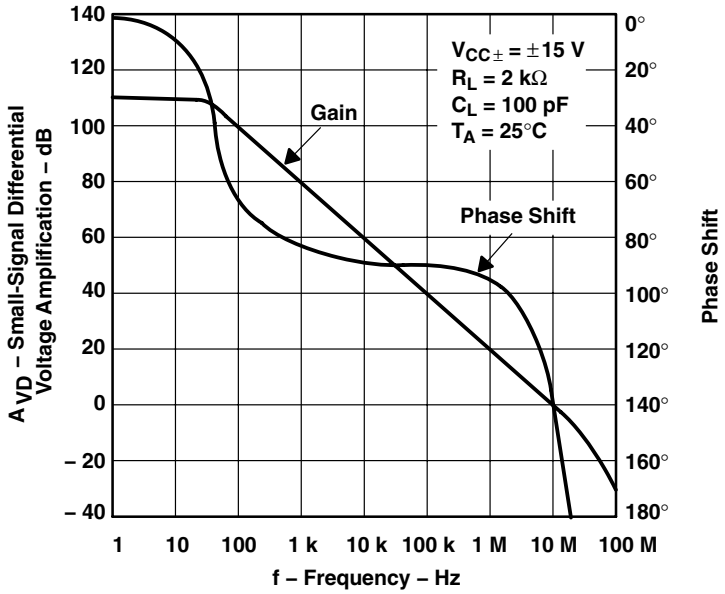


Figure 28

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

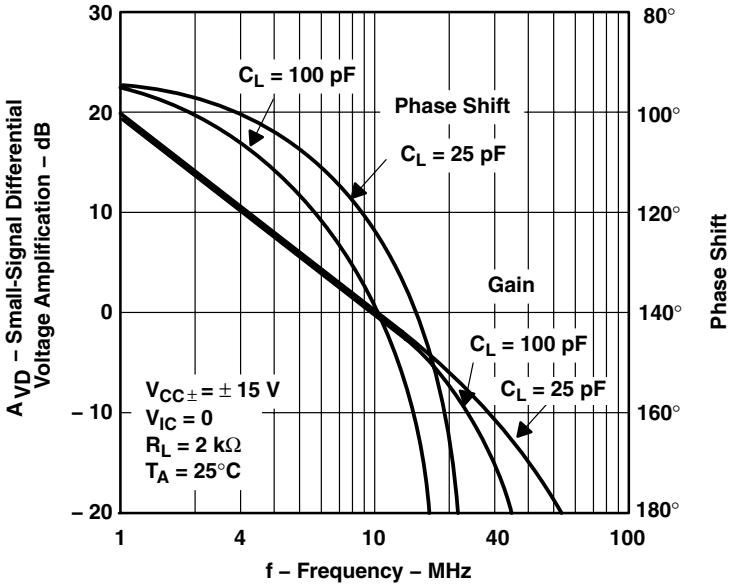


Figure 29

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

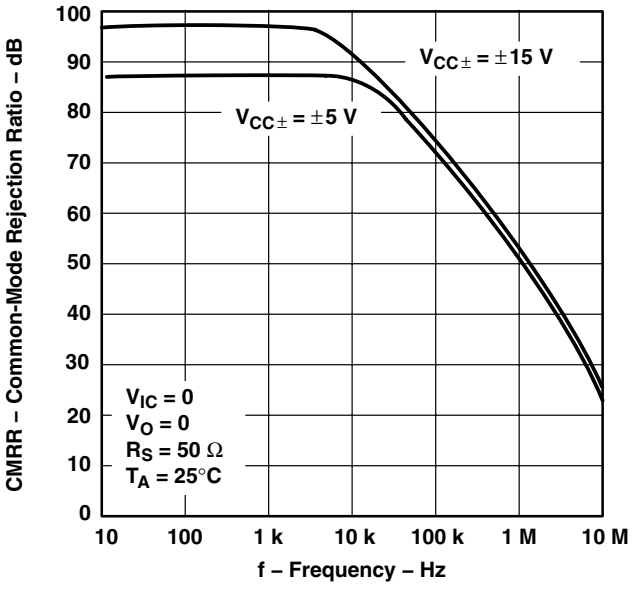


Figure 30

COMMON-MODE REJECTION RATIO† vs FREE-AIR TEMPERATURE

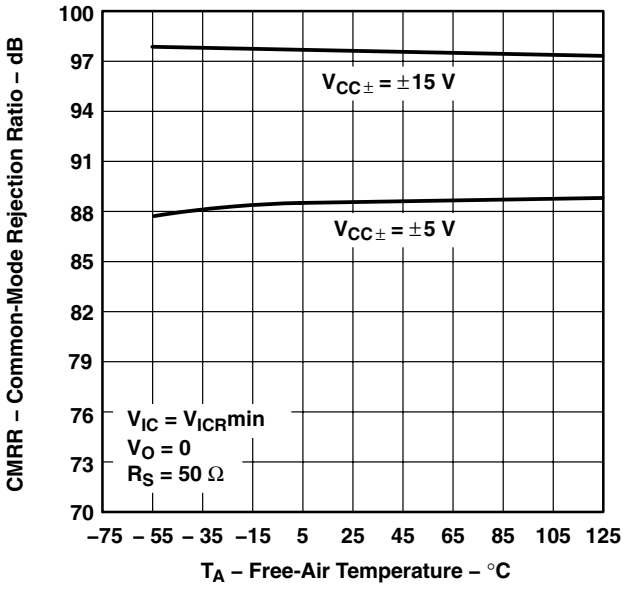


Figure 31

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

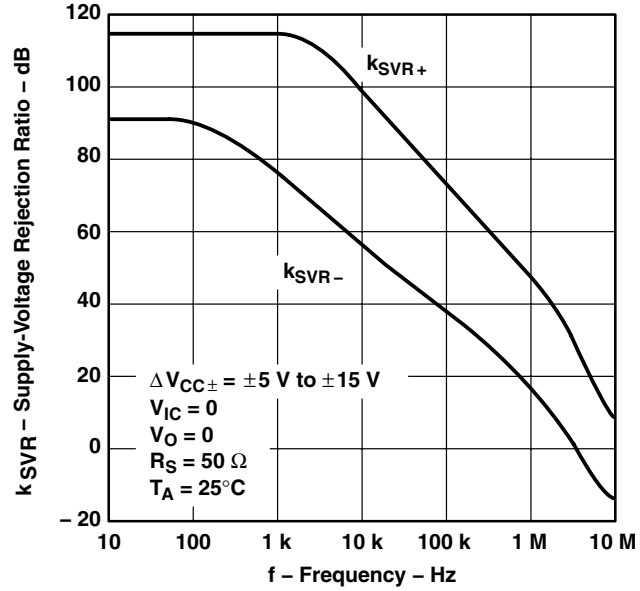


Figure 32

SUPPLY-VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

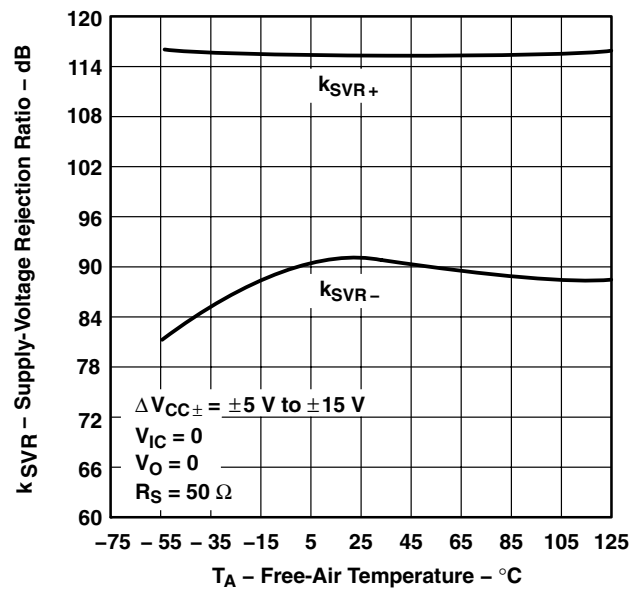


Figure 33

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLE2071
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

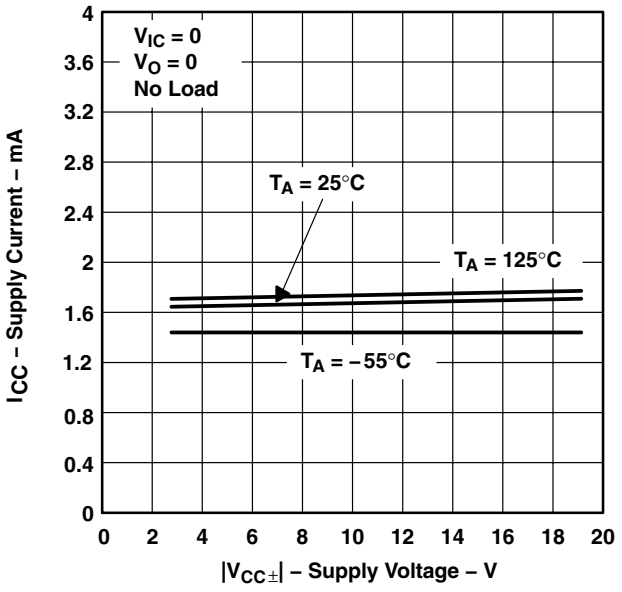


Figure 34

TLE2072
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

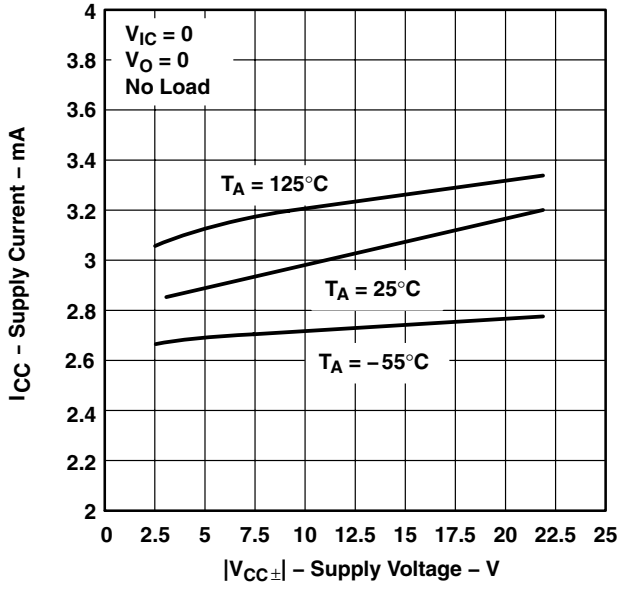


Figure 35

TLE2074
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

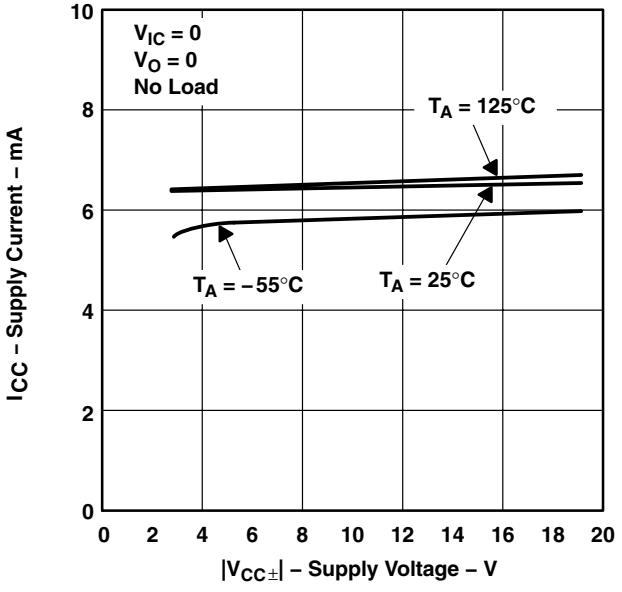


Figure 36

TLE2071
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

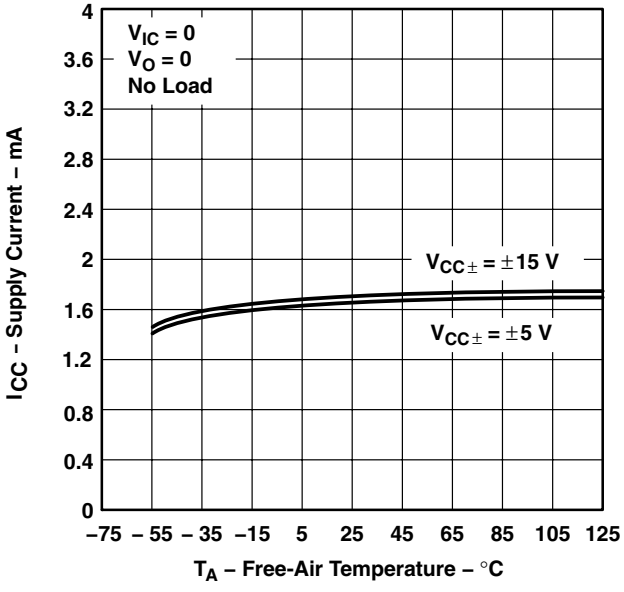


Figure 37

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**TLE2072
SUPPLY CURRENT† vs FREE-AIR TEMPERATURE**

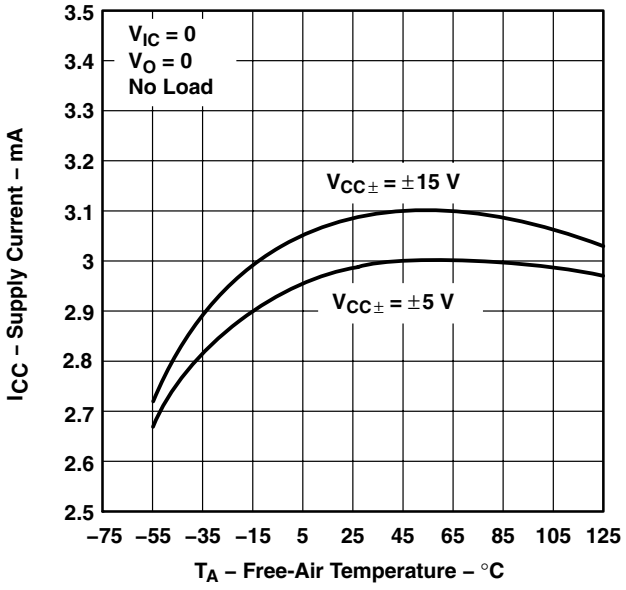


Figure 38

**TLE2074
SUPPLY CURRENT† vs FREE-AIR TEMPERATURE**

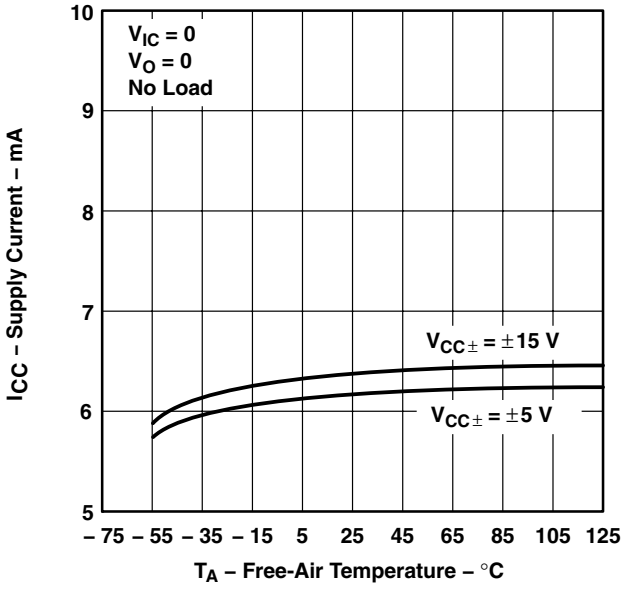


Figure 39

**TLE2071
SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE**

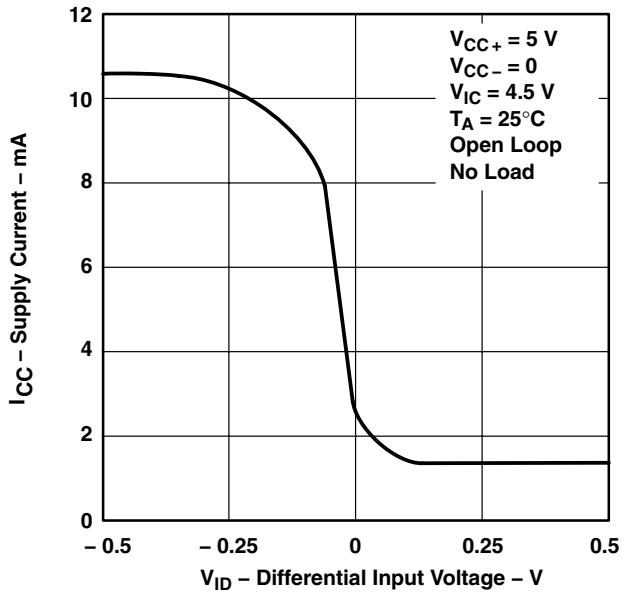


Figure 40

**TLE2072
SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE**

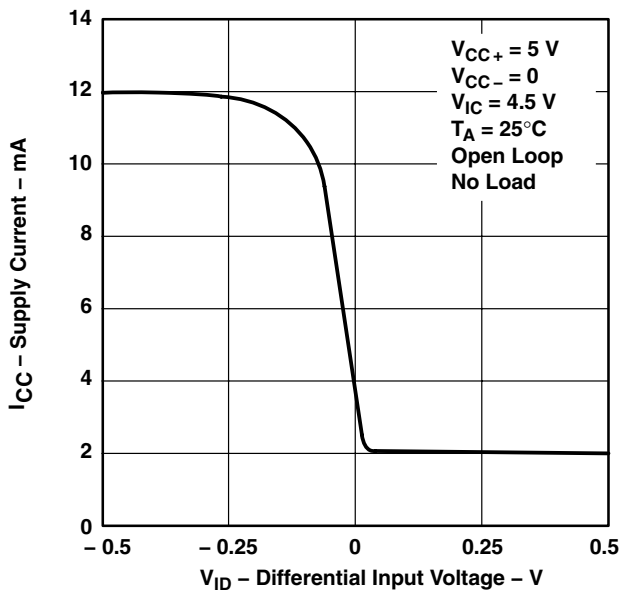


Figure 41

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**TLE2074
SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE**

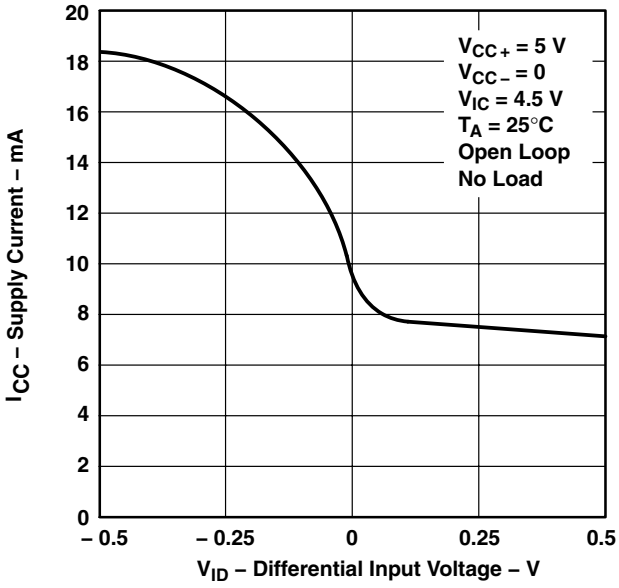


Figure 42

**TLE2071
SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE**

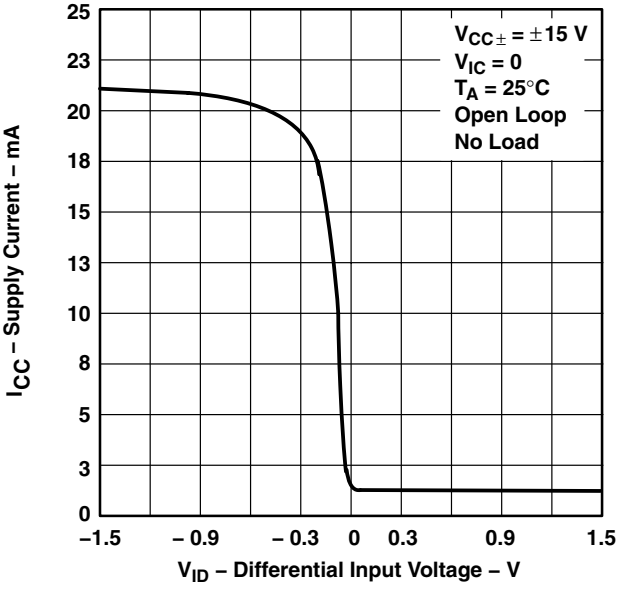


Figure 43

**TLE2072
SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE**

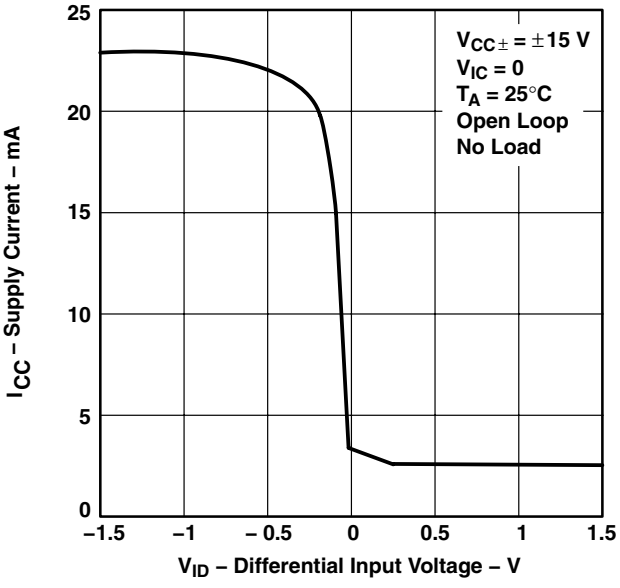


Figure 44

**TLE2074
SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE**

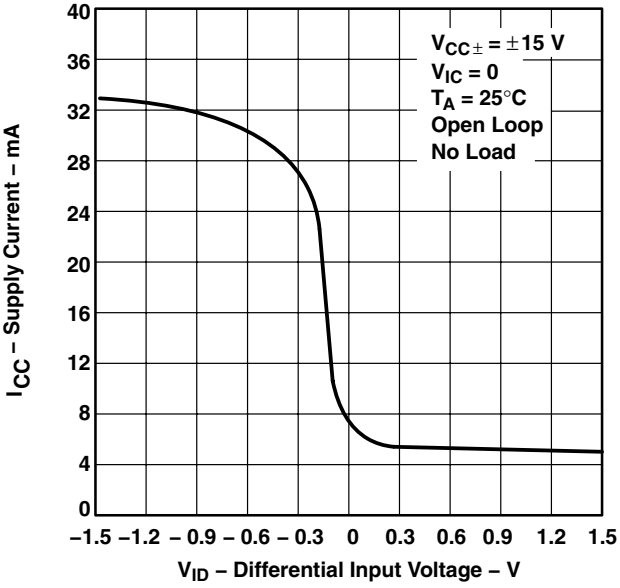


Figure 45

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

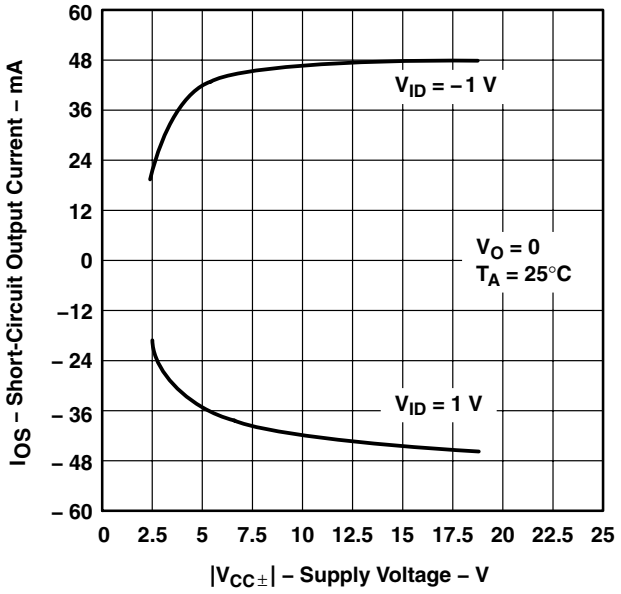


Figure 46

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

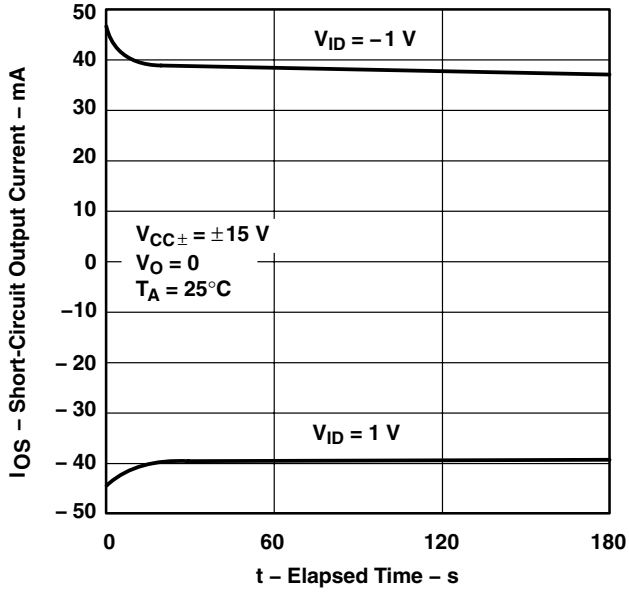


Figure 47

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

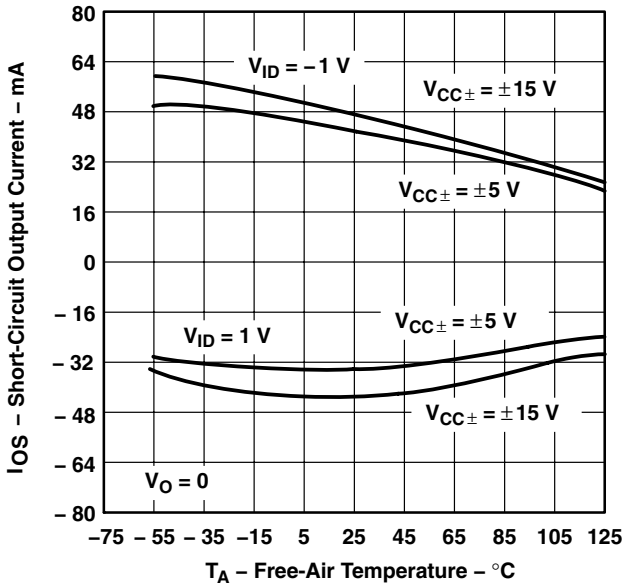


Figure 48

SLEW RATE† vs FREE-AIR TEMPERATURE

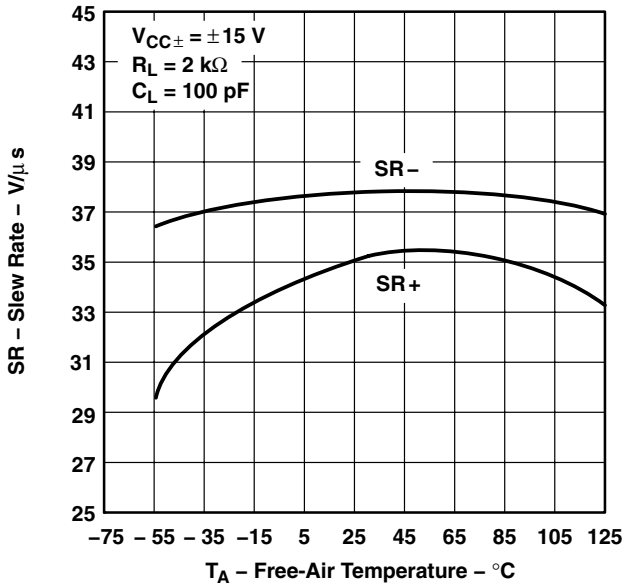


Figure 49

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SLEW RATE† vs FREE-AIR TEMPERATURE

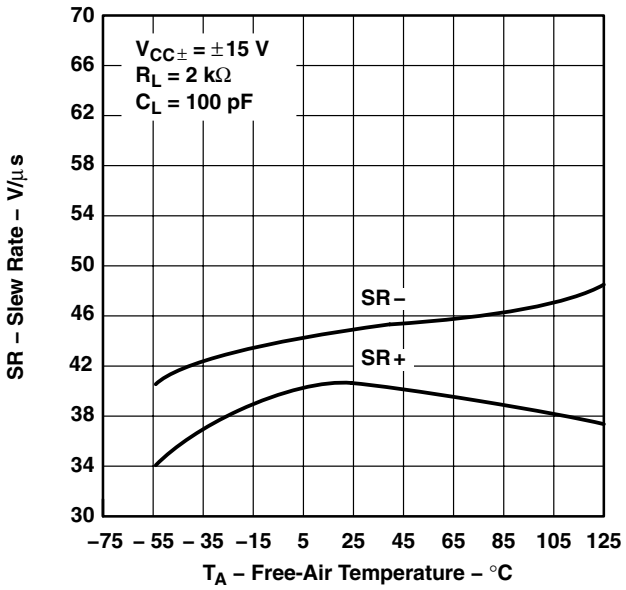


Figure 50

SLEW RATE vs LOAD RESISTANCE

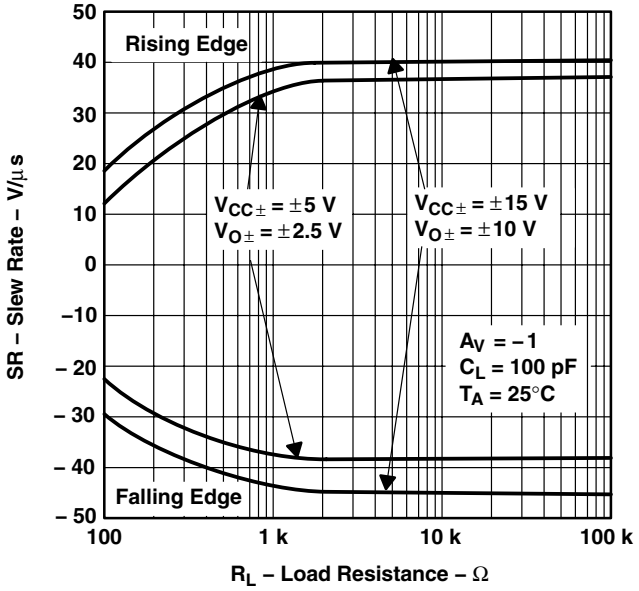


Figure 51

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

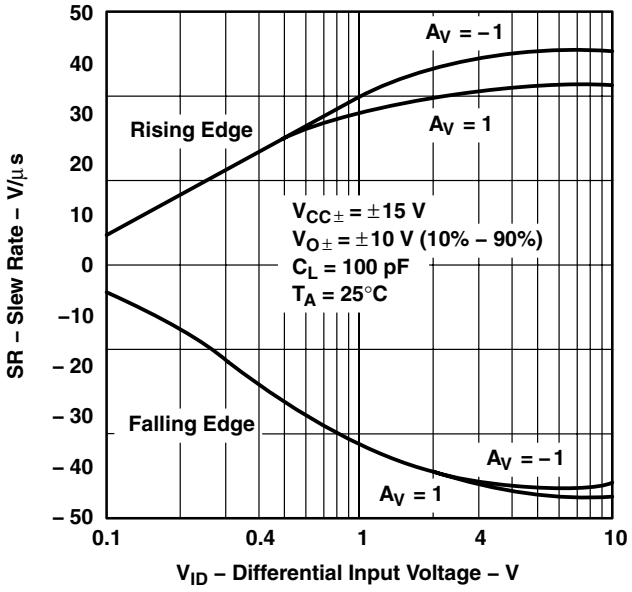


Figure 52

EQUIVALENT INPUT NOISE VOLTAGE (SPECTRAL DENSITY) vs FREQUENCY

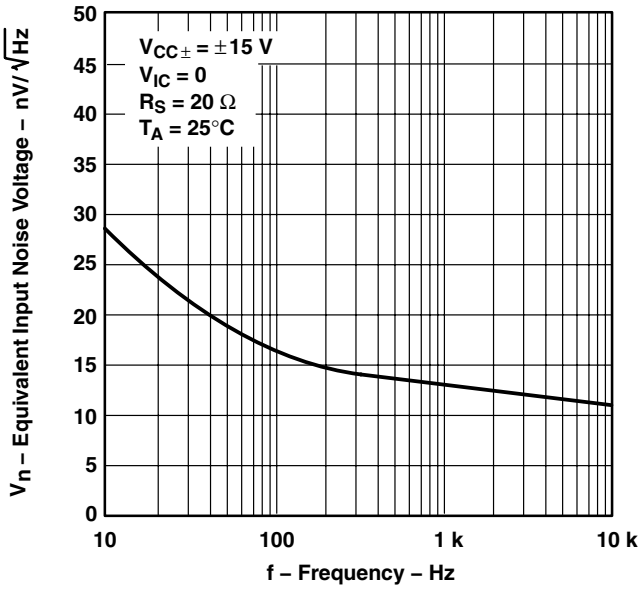


Figure 53

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

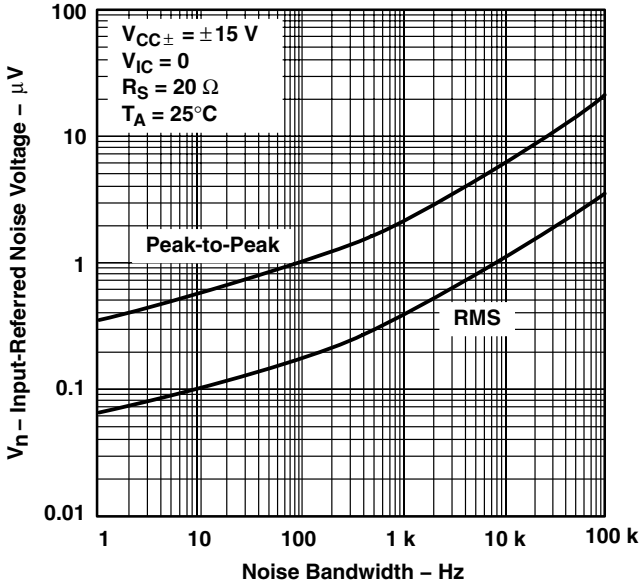


Figure 54

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

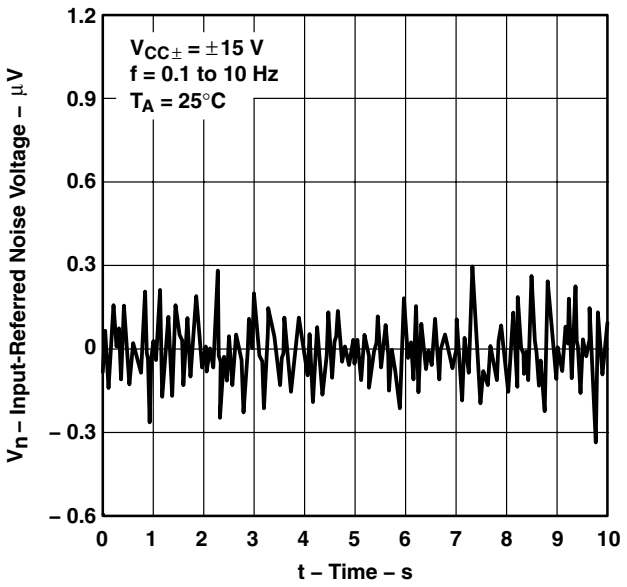


Figure 55

THIRD-OCTAVE SPECTRAL NOISE DENSITY vs FREQUENCY BANDS

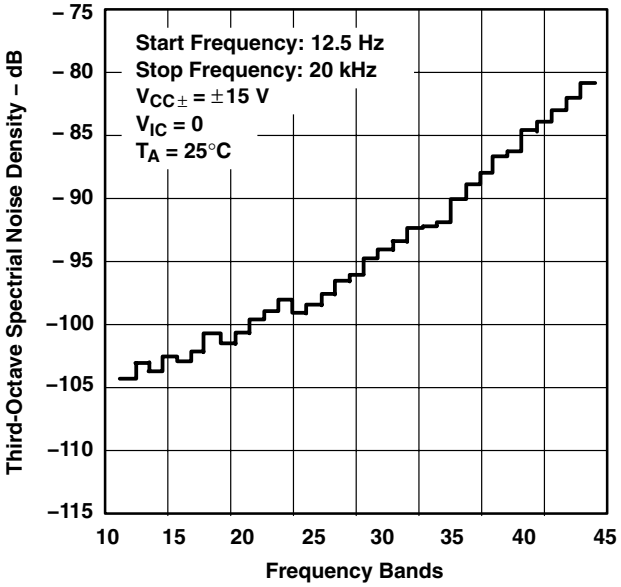


Figure 56

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

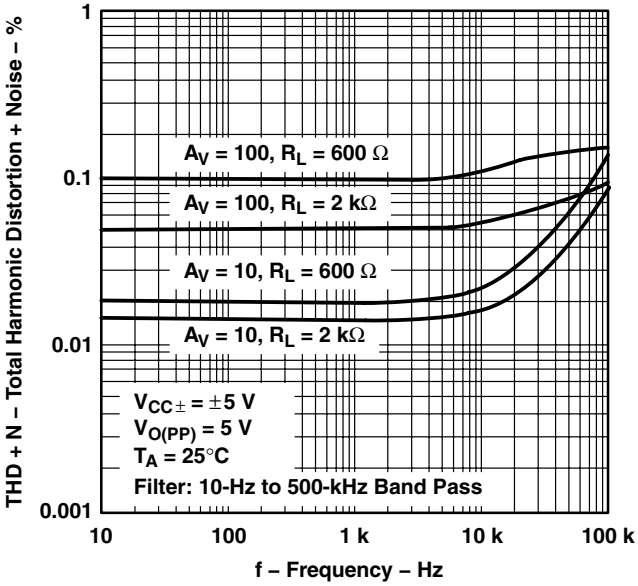


Figure 57

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

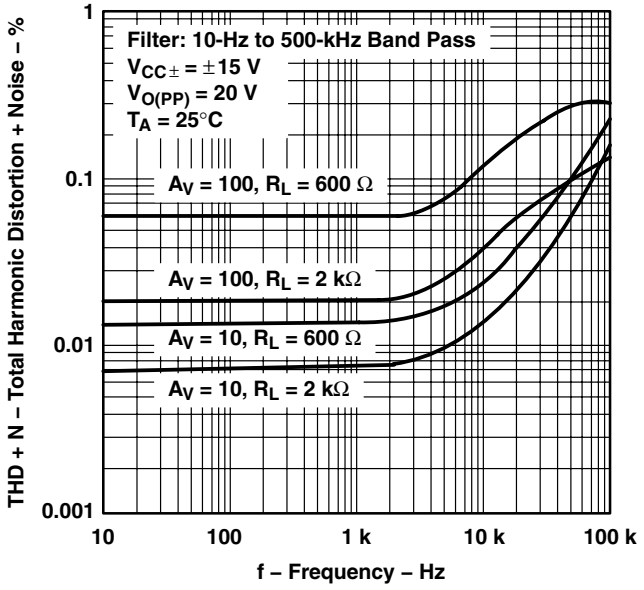


Figure 58

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

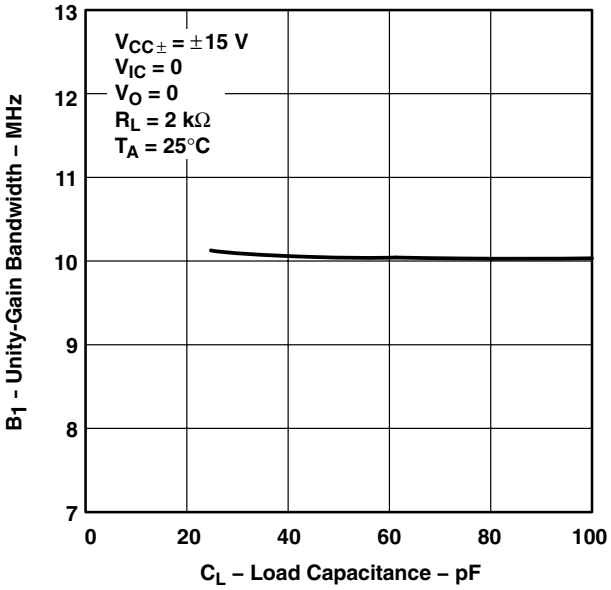


Figure 59

GAIN-BANDWIDTH PRODUCT† vs FREE-AIR TEMPERATURE

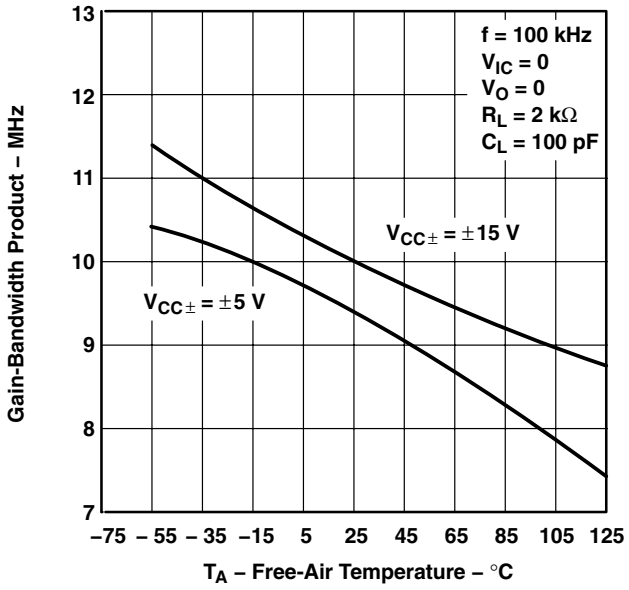


Figure 60

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

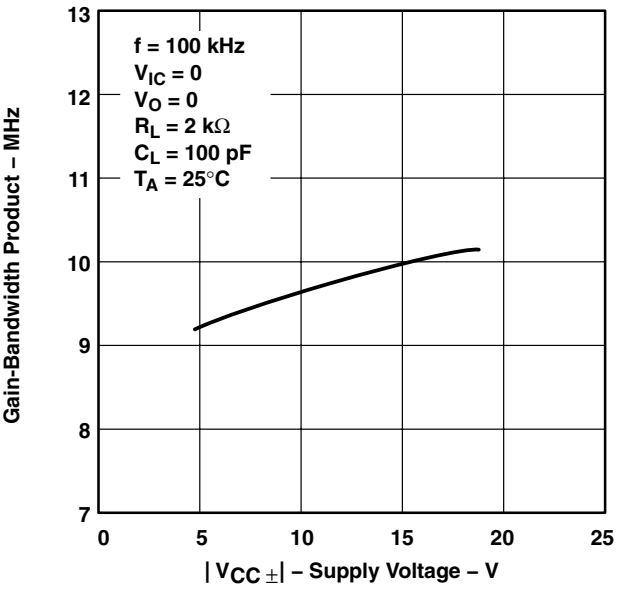


Figure 61

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

GAIN MARGIN vs LOAD CAPACITANCE

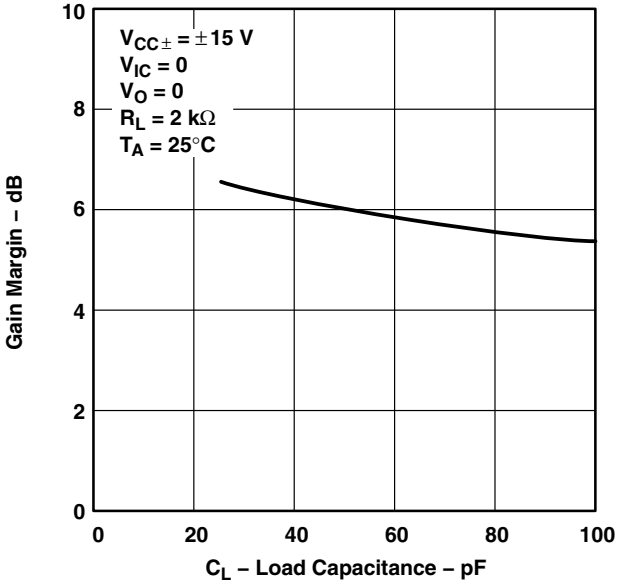


Figure 62

PHASE MARGIN† vs FREE-AIR TEMPERATURE

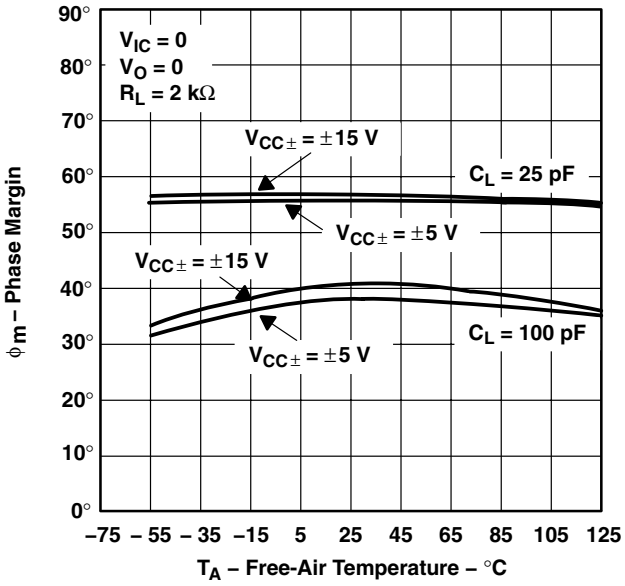


Figure 63

PHASE MARGIN vs SUPPLY VOLTAGE

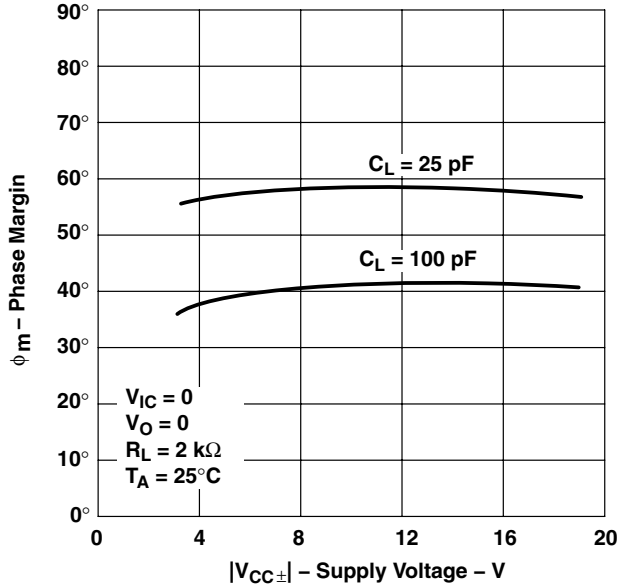


Figure 64

PHASE MARGIN vs LOAD CAPACITANCE

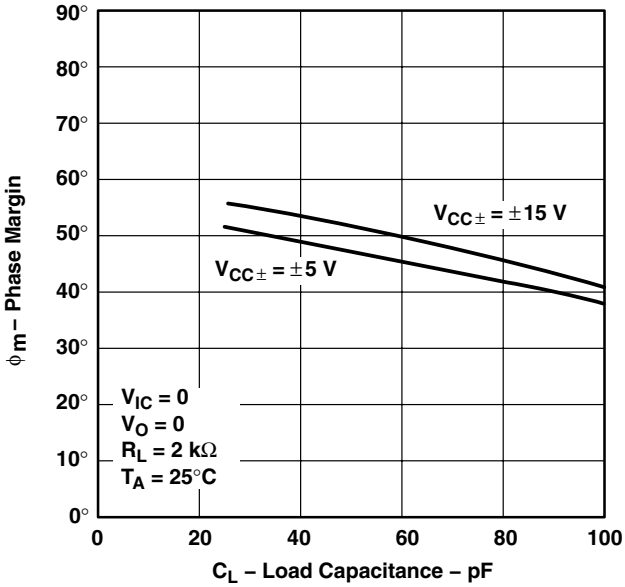


Figure 65

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NONINVERTING LARGE-SIGNAL PULSE RESPONSE†

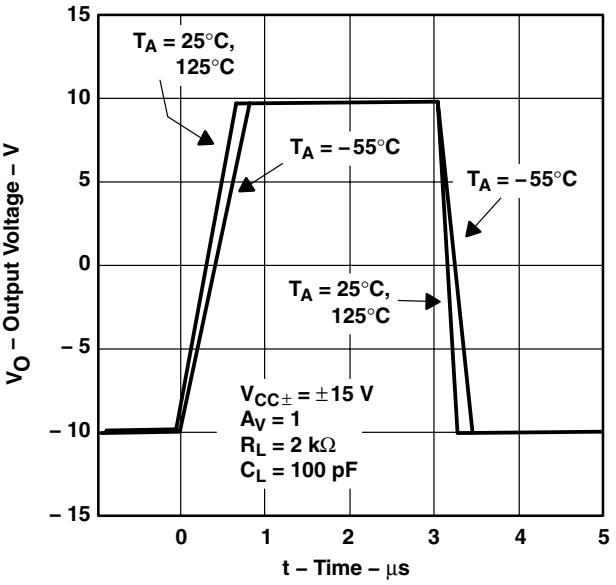


Figure 66

SMALL-SIGNAL PULSE RESPONSE

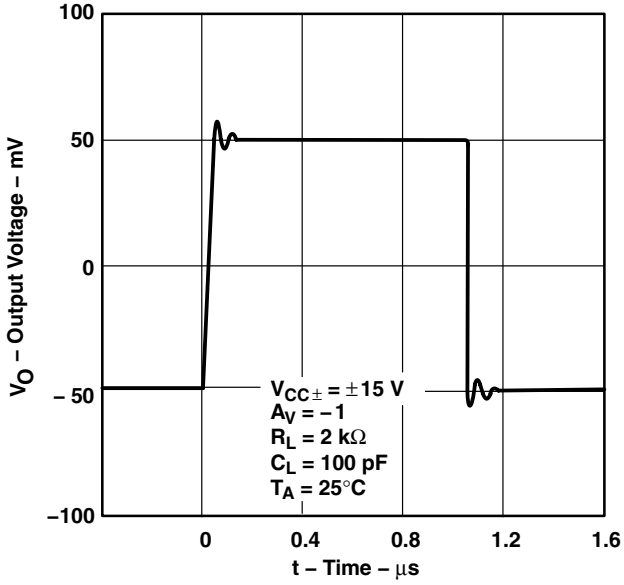


Figure 67

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

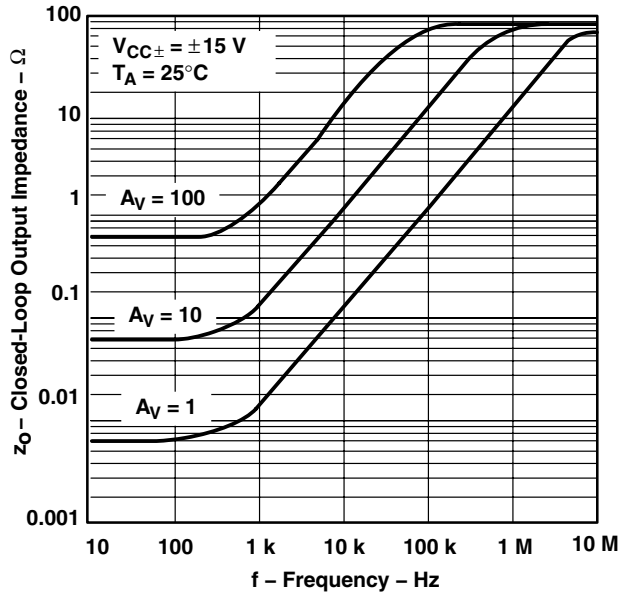


Figure 68

TLE2072 AND TLE2074 CROSSTALK ATTENUATION vs FREQUENCY

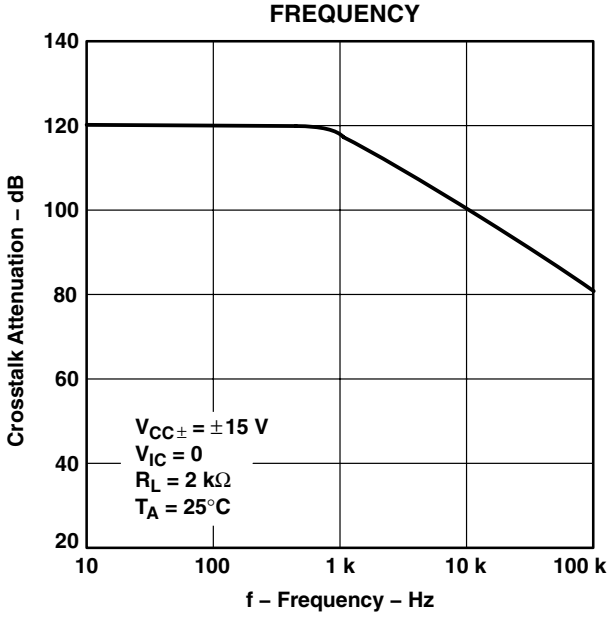


Figure 69

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input characteristics

The TLE207x, TLE207xA, and TLE207xB are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction. Because of the extremely high input impedance and resulting low bias current requirements, the TLE207x, TLE207xA, and TLE207xB are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 70). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

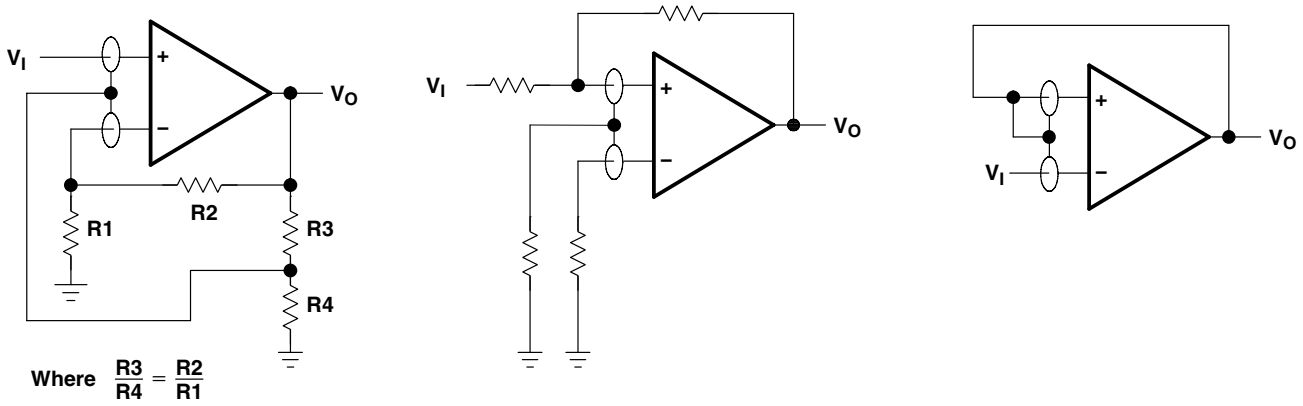


Figure 70. Use of Guard Rings

TLE2071 input offset voltage nulling

The TLE2071 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 71 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left unconnected.

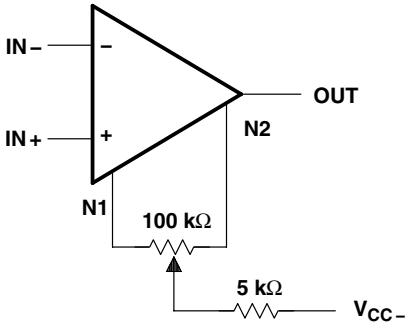


Figure 71. Input Offset Voltage Nulling

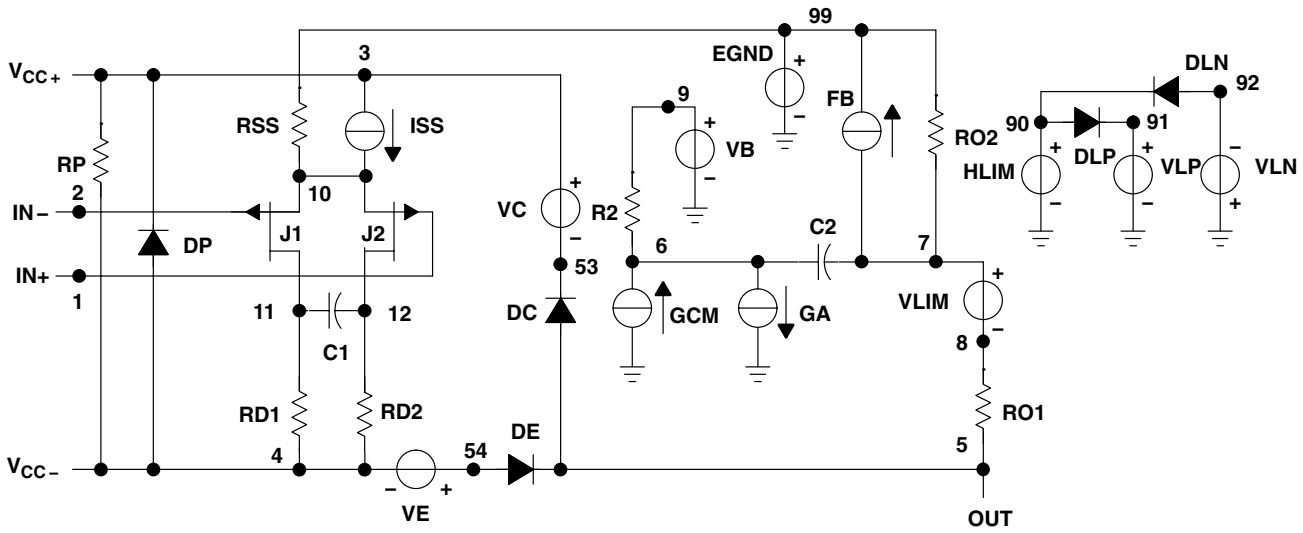
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 4) and subcircuit Figure 72 were generated using the TLE207x typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLE2074 1 2 3 4 5
C1      11      12      2.2E–12
C2       6       7      10.00E–12
DC       5      53      DX
DE      54       5      DX
DLP     90      91      DX
DLN     92      90      DX
DP       4       3      DX
EGND    99       0      POLY (2) (3,0) (4,0) 0 .5 .5
FB       7      99      POLY (5) VB VC VE VLP VLN 0
 + 5.607E6 –6E6 6E6 6E6 –6E6
GA       6       0      11 12 333.0E–6
GCM      0       6      10 99 7.43E–9
ISS      3      10      DC 400.0E–6
HLIM    90       0      VLIM 1K
J1      11       2      10 JX
J2      12       1      10 JX
R2       6       9      100.0E3
RD1      4      11      3.003E3
RD2      4      12      3.003E3
R01      8       5      80
R02      7      99      80
RP       3       4      27.30E3
RSS     10      99      500.0E3
VB       9       0      DC 0
VC       3      53      DC 2.20
VE      54       4      DC 2.20
VLIM     7       8      DC 0
VLP     91       0      DC 45
VLN      0      92      DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO=–.6)
.ENDS
```

Figure 72. Boyle Macromodel and Subcircut

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2071AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2071AQ
TLE2071AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2071AQ
TLE2071AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2071AQ
TLE2071AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2071AQ
TLE2072AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2072AQ
TLE2072AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2072AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLE2071A-Q1, TLE2072A-Q1 :

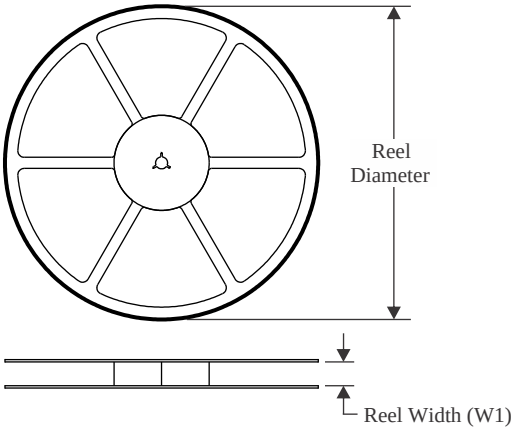
- Catalog : TLE2071A, TLE2072A
- Military : TLE2071AM, TLE2072AM

NOTE: Qualified Version Definitions:

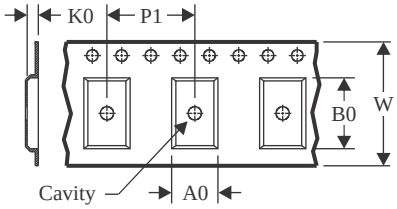
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

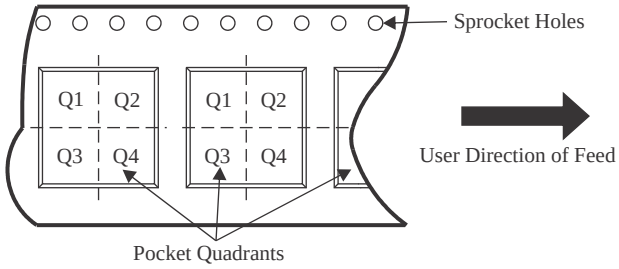


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

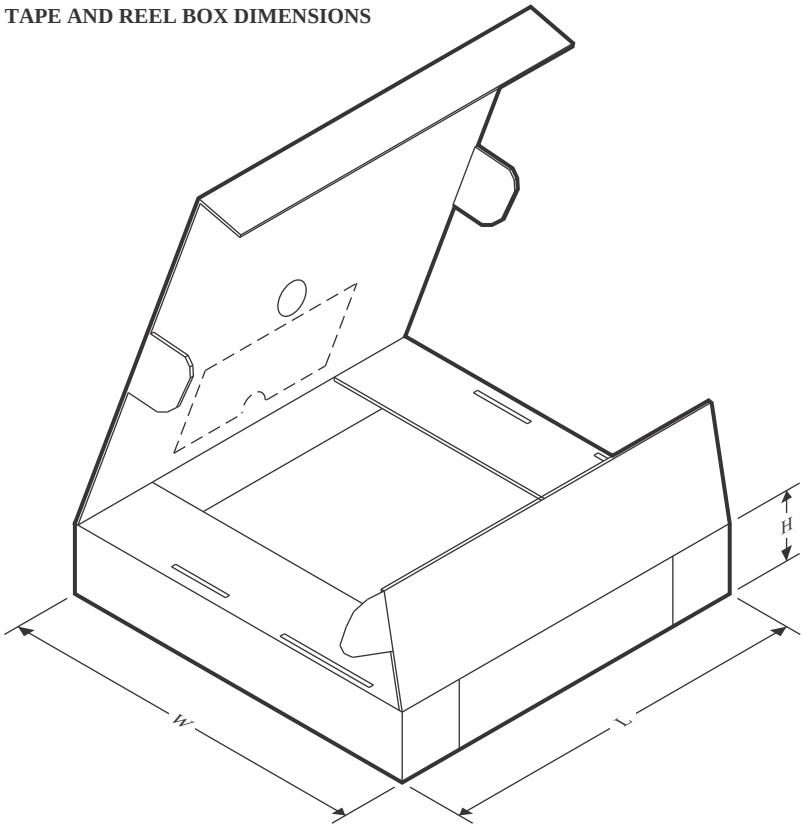
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

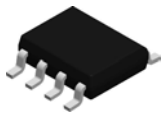
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2072AQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2072AQDRG4Q1	SOIC	D	8	2500	353.0	353.0	32.0

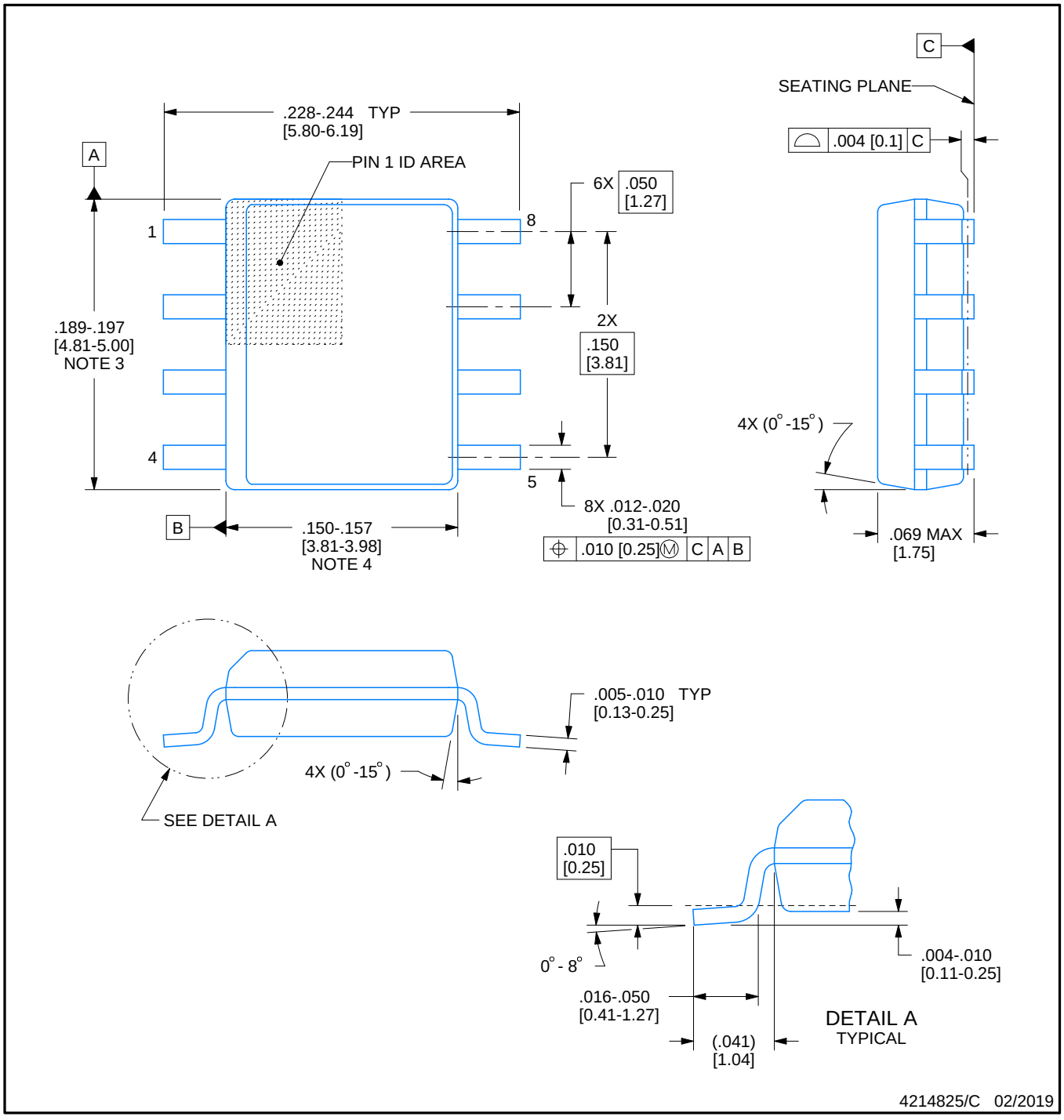


PACKAGE OUTLINE

D0008A

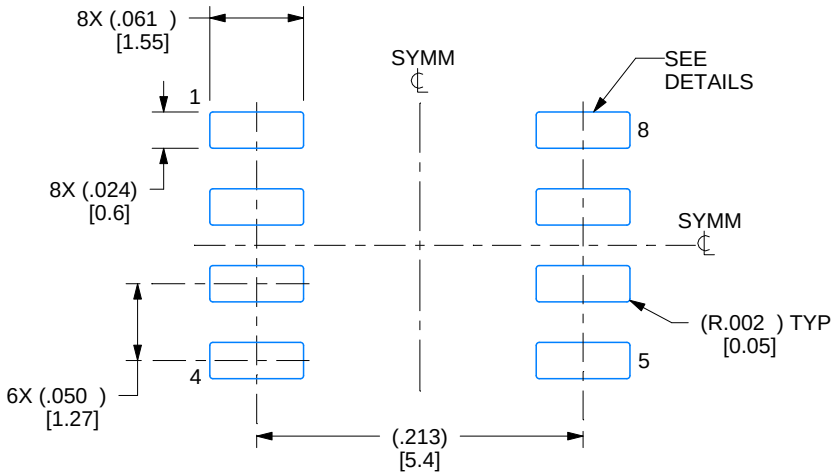
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

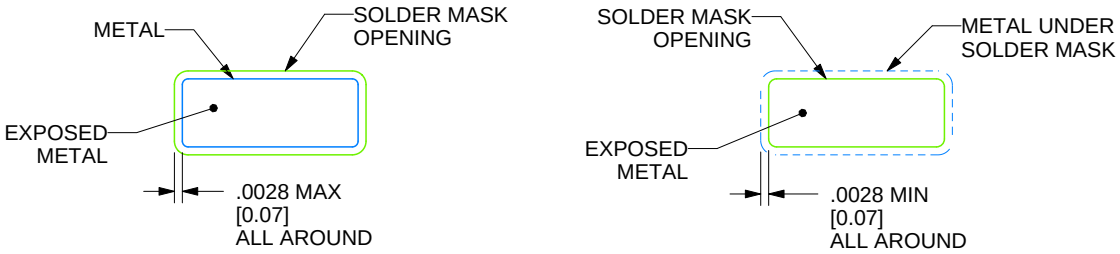


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

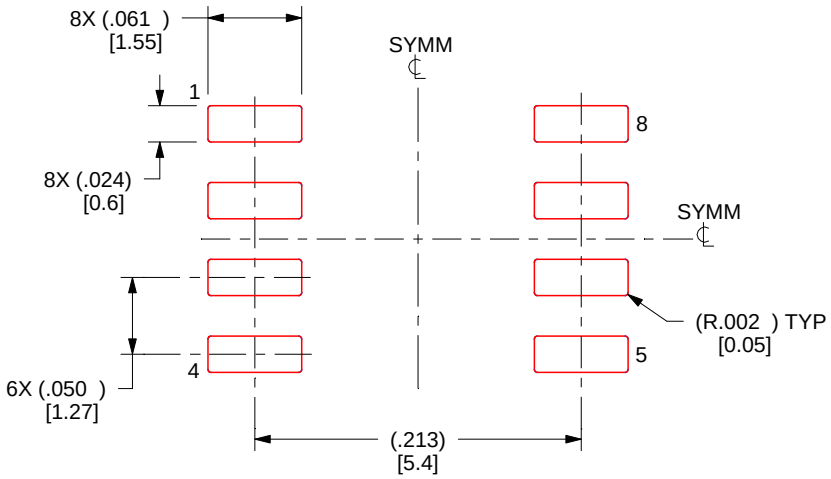
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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