

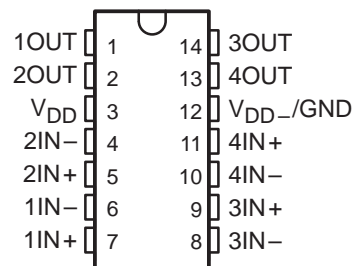
# LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

TLC354

SLCS116B – SEPTEMBER 1985 – REVISED FEBRUARY 1997

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages**  
1.4 V to 18 V
- **Very Low Supply Current Drain**  
300  $\mu$ A Typ at 5 V  
130  $\mu$ A Typ at 1.4 V
- **Built-In ESD Protection**
- **High Input Impedance . . .  $10^{12} \Omega$  Typ**
- **Extremely Low Input Bias Current**  
5 pA Typ
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23  $\mu$ V/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM339**

D, N, OR PW PACKAGE  
(TOP VIEW)



symbol (each comparator)



## description

This device is fabricated using LinCMOS™ technology and consists of four independent differential voltage comparators; each is designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than  $10^{12} \Omega$ ), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC354 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC354C is characterized for operation from 0°C to 70°C. The TLC354I is characterized for operation over the industrial temperature range of -40° to 85°C. The TLC354M is characterized for operation over the full military temperature range -55°C to 125°C.

AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	5 mV	TLC354CD	TLC354CN	TLC354CPW	TLC354Y
-40°C to 85°C	5 mV	TLC354ID	TLC354IN	—	—
-55°C to 125°C	5 mV	TLC354MD	TLC354MN	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC354CDR).



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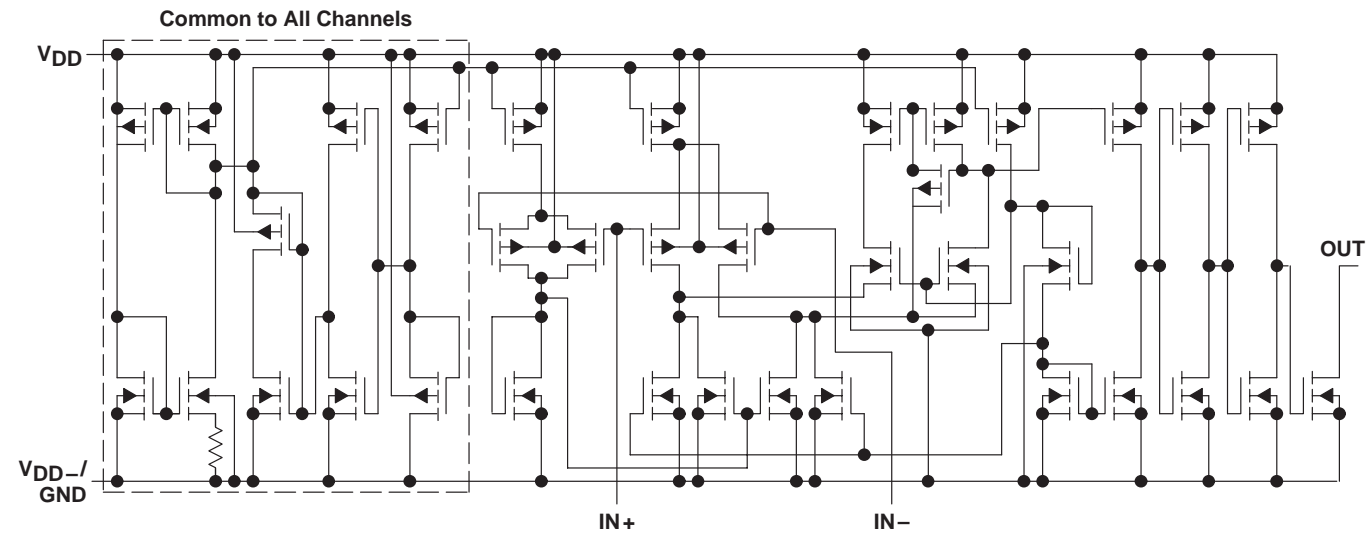
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TLC354
LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

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equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Parameters include Supply voltage (VDD), Differential input voltage (VID), Input voltage (VI), Input voltage range, Output voltage (VO), Input current (II), Output current (IO), Duration of output short circuit, Continuous total dissipation, and Operating free-air temperature range (TA) for TLC354C, TLC354I, and TLC354M. Storage temperature range and Lead temperature are also listed.

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

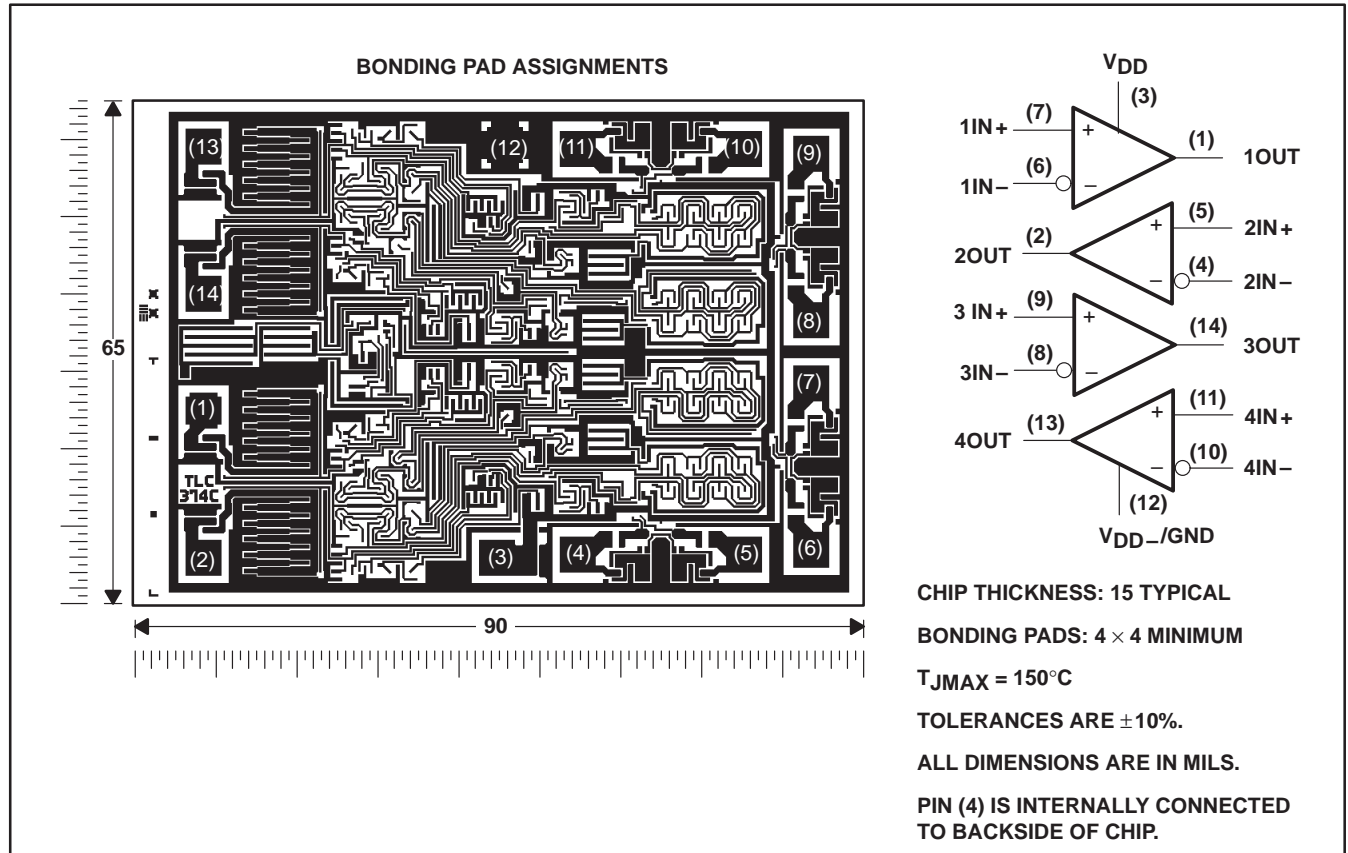
- NOTES: 1. All voltage values except differential voltages are with respect to network ground.
- 2. Differential voltages are at IN+ with respect to IN-.
- 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

Table with 7 columns: PACKAGE, TA ≤ 25°C POWER RATING, DERATING FACTOR, DERATE ABOVE TA, TA = 70°C POWER RATING, TA = 85°C POWER RATING, TA = 125°C POWER RATING. Rows are listed for packages D, N, and PW.

### TLC364Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC354C. Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.



## TLC354

## LinCMOS™ QUADRUPLÉ DIFFERENTIAL COMPARATORS

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## recommended operating conditions

		TLC354C		TLC354I		TLC354M		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD}$		1.4	16	1.4	16	1.4	16	V
Common-mode input voltage, $V_{IC}$	$V_{DD} = 1.4\text{ V}$	0	0.2	0	0.2	0	0.2	V
	$V_{DD} = 5\text{ V}$	0	3.5	0	3.5	0	3.5	
	$V_{DD} = 10\text{ V}$	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, $T_A$		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature,  $V_{DD} = 1.4\text{ V}$ 

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC354C			TLC354I			TLC354M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		$V_{IC} = V_{ICRmin}$ , See Note 4	25°C		2	5		2	5		2	5	mV
			Full range			6.5			7			10	
$I_{IO}$ Input offset current			25°C		1			1			1		pA
			MAX			0.3			1			10	nA
$I_{IB}$ Input bias current			25°C		5			5			5		pA
			MAX			0.6			2			20	nA
$V_{ICR}$ Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
$I_{OH}$ High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1			0.1			0.1		nA
		$V_{OH} = 15\text{ V}$	Full range			1			1			1	μA
$V_{OL}$ Low-level output voltage	$V_{ID} = -0.5\text{ V}$ , $I_{OL} = 0.6\text{ mA}$		25°C		100	200		100	200		100	200	mV
			Full range			200			200			200	
$I_{OL}$ Low-level output current	$V_{ID} = -0.5\text{ V}$ , $V_{OL} = 300\text{ mV}$		25°C	1	1.6		1	1.6		1	1.6		mA
$I_{DD}$ Supply current (four comparators)	$V_{ID} = 0.5\text{ V}$ , No load		25°C		130	300		130	300		130	300	μA
			Full range			400			400			400	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC354C, –40°C to 85°C for TLC354I, and –55°C to 125°C for the TLC354M. MAX is 70°C for TLC354C, 85°C TLC354I, and 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER		TEST CONDITIONS		T <sub>A</sub> <sup>†</sup>	TLC354C			TLC354I			TLC354M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>IC</sub> = V <sub>ICRmin</sub> , See Note 5	25°C		2	5		2	5		2	5	mV	
			Full range			6.5			7			10		
I <sub>IO</sub>	Input offset current		25°C		1			1			1		pA	
			MAX			0.3			1			10	nA	
I <sub>IB</sub>	Input bias current		25°C		5			5			5		pA	
			MAX			0.6			2			20	nA	
V <sub>ICR</sub>	Common-mode input voltage range		25°C		0 to V <sub>DD</sub> −1			0 to V <sub>DD</sub> −1			0 to V <sub>DD</sub> −1		V	
			Full range		0 to V <sub>DD</sub> −1.5			0 to V <sub>DD</sub> −1.5			0 to V <sub>DD</sub> −1.5			
I <sub>OH</sub>	High-level output current	V <sub>ID</sub> = 1 V	V <sub>OH</sub> = 5 V	25°C		0.1			0.1			0.1		nA
			V <sub>OH</sub> = 15 V	Full range			1			1			1	
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = −1 V, I <sub>OL</sub> = 4 mA	25°C		150	400		150	400		150	400	mV	
			Full range			700			700			700		
I <sub>OL</sub>	Low-level output current	V <sub>ID</sub> = −1 V, V <sub>OL</sub> = 1.5 mV	25°C		6	16		6	16		6	16	mA	
I <sub>DD</sub>	Supply current (four comparators)	V <sub>ID</sub> = 1 V, No load	25°C		0.3	0.6		0.3	0.6		0.3	0.6	mA	
			Full range			0.8			0.8			0.8		

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70 °C for TLC354C, –40°C to 85°C for TLC354I, and –55°C to 125°C for the TLC354M. MAX is 70°C for TLC354C, 85°C TLC354I, and 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

**switching characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS		TLC354C, TLC354I TLC354M			UNIT
			MIN	TYP	MAX	
Response time	R <sub>L</sub> connected to 5 V through 5.1 kΩ, C <sub>L</sub> = 15 pF‡,      See Note 6	100-mV input step with 5-mV overdrive	650			ns
		TTL-level input step	200			

‡  $C_L$  includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

# TLC354

## LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 1.4\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLC354Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR} \text{ min, See Note 4}$		2	5	mV
$I_{IO}$ Input offset current			1		pA
$I_{IB}$ Input bias current			5		pA
$V_{ICR}$ Common-mode input voltage range		0 to 0.2			V
$I_{OH}$ High-level output current	$V_{ID} = 1\text{ V, } V_{OH} = 5\text{ V}$		0.1		nA
$V_{OL}$ Low-level output voltage	$V_{ID} = -0.5\text{ V, } I_{OL} = 0.6\text{ mA}$		100	200	mV
$I_{OL}$ Low-level output current	$V_{ID} = -0.5\text{ V, } V_{OL} = 300\text{ mV}$	1	1.6		mA
$I_{DD}$ Supply current (four comparators)	$V_{ID} = 0.5\text{ V, No load}$		130	300	$\mu\text{A}$

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-k $\Omega$  resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLC354Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR} \text{ min, See Note 5}$		2	5	mV
$I_{IO}$ Input offset current			1		pA
$I_{IB}$ Input bias current			5		pA
$V_{ICR}$ Common-mode input voltage range		0 to $V_{DD}-1$			V
$I_{OH}$ High-level output current	$V_{ID} = 1\text{ V, } V_{OH} = 5\text{ V}$		0.1		nA
$V_{OL}$ Low-level output voltage	$V_{ID} = -1\text{ V, } I_{OL} = 4\text{ mA}$		150	400	mV
$I_{OL}$ Low-level output current	$V_{ID} = -1\text{ V, } V_{OL} = 1.5\text{ mV}$	6	16		mA
$I_{DD}$ Supply current (four comparators)	$V_{ID} = 1\text{ V, No load}$		0.3	0.6	mA

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-k $\Omega$  resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

**switching characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS		TLC354Y			UNIT
			MIN	TYP	MAX	
Response time	$R_L$ connected to 5 V through 5.1 k $\Omega$ , $C_L = 15\text{ pF}^\ddagger$ , See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

$^\ddagger C_L$  includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

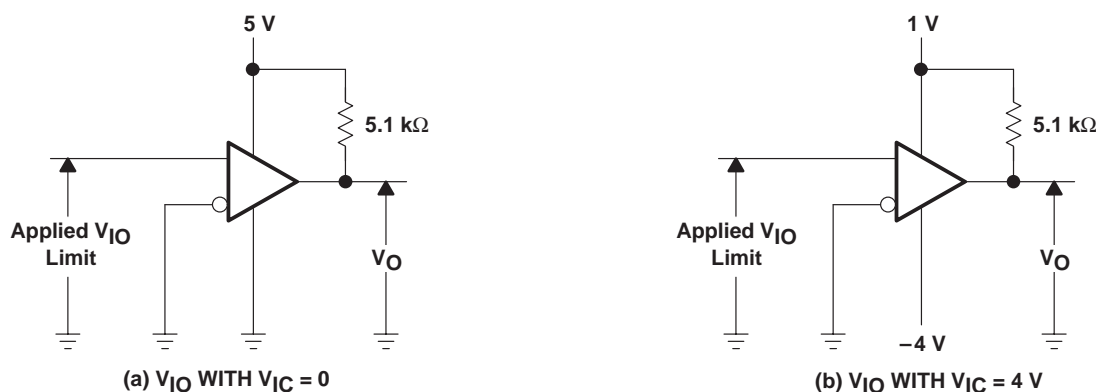
## PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the  $V_{ICR}$  test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.



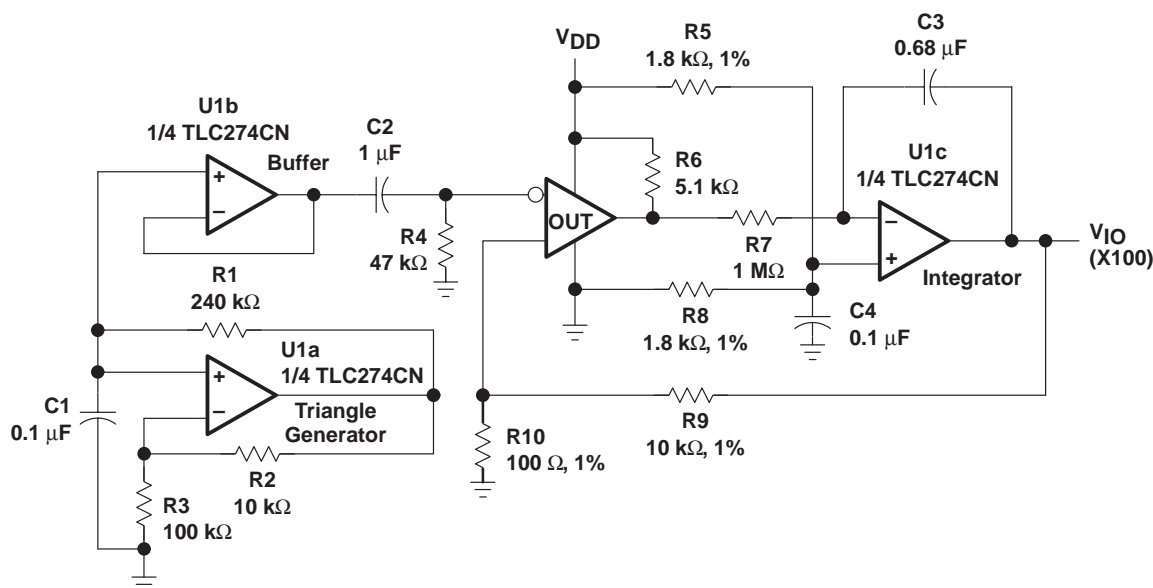
**Figure 1. Method for Verifying That Input Offset Voltage is Within Specified Limits**

## PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practice circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

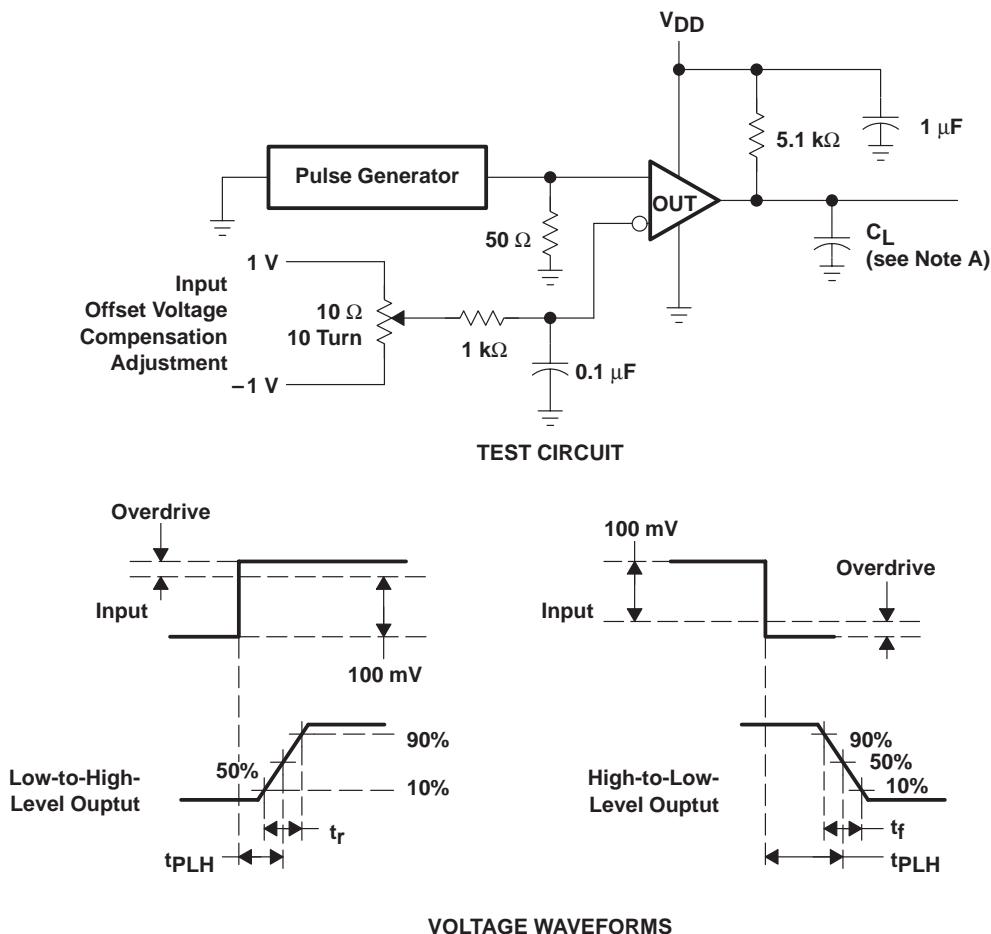


**Figure 2. Test Circuit for Input Offset Voltage Measurement**



## PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105-mV or 5-mV overdrive, causes the output to change.



NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 3. Response, Rise, and Fall Times Test Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC354CD</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC354C
TLC354CD.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC354C
<a href="#">TLC354CN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC354CN
TLC354CN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC354CN
<a href="#">TLC354CPW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P354
TLC354CPW.A	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P354
<a href="#">TLC354CPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P354
TLC354CPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P354
<a href="#">TLC354ID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC354I
TLC354ID.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC354I

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC354CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC354CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

## TUBE

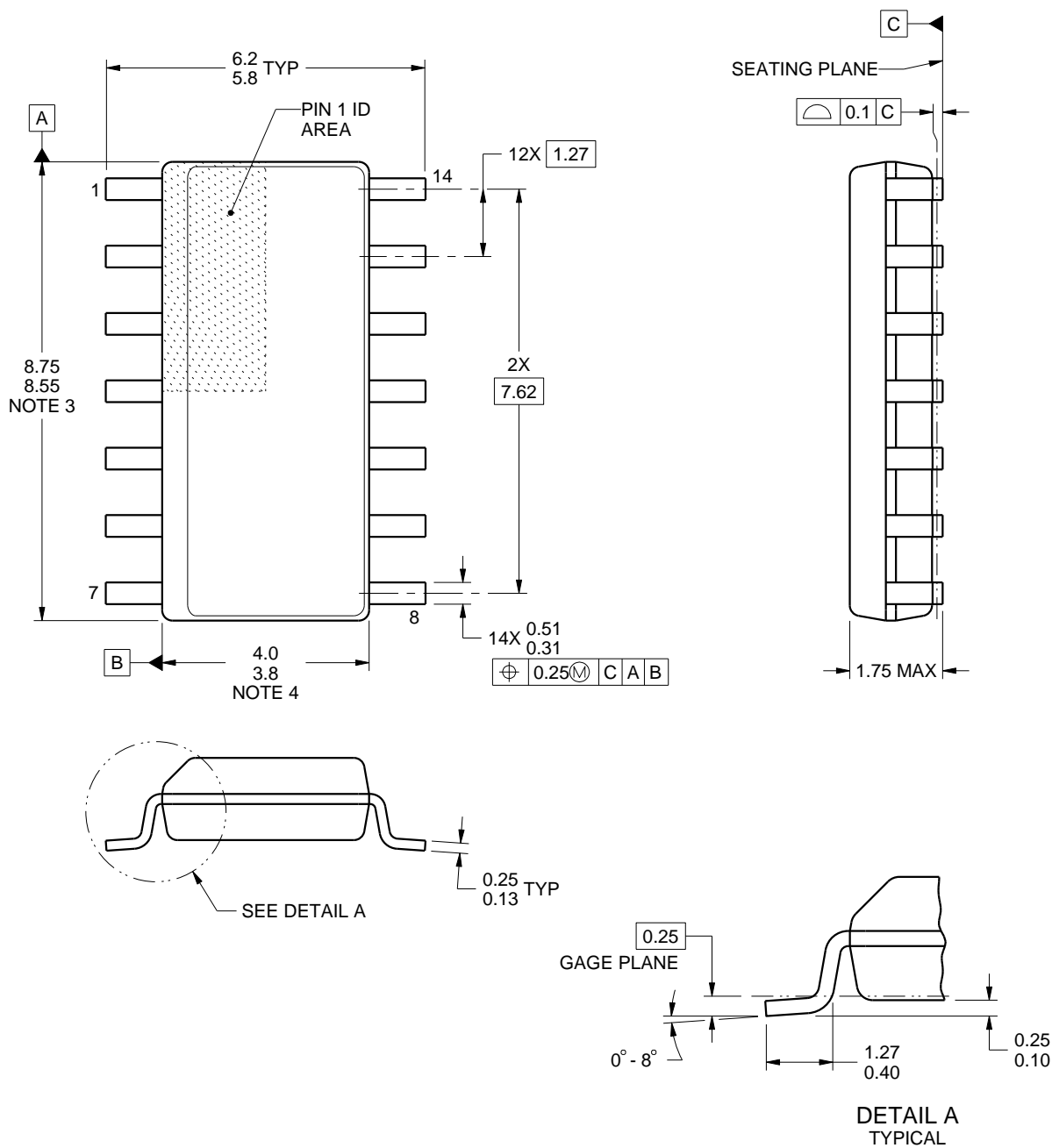


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC354CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC354CD.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC354CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC354CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC354CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC354CPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC354ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC354ID.A	D	SOIC	14	50	505.46	6.76	3810	4

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



**PW0014A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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