TLC352 Dual Differential Comparator

1 Features

- Single or dual supply operation
- Wide range of supply voltages: 2.7V to 18V
- Very low supply current drain:
  - 150µA typical at 5V
- Built-in ESD protection
- High input impedance: $10^{12}\Omega$ typical
- Extremely low input bias current 5pA typical
- Ultra-stable low input offset voltage
- Common-mode input voltage range includes ground
- Outputs compatible with TTL, MOS, and CMOS
- Pin-compatible with LM393

2 Description

This device is fabricated using CMOS technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2.7V to 18V. Each device features extremely high input impedance (typically greater than $10^{12}\Omega$), which allows direct interface to high-impedance sources. The output are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from 2.7V supply makes this device an excellent for low-voltage battery applications.

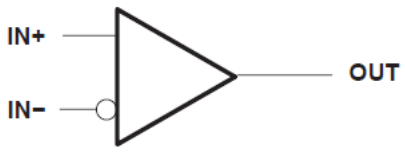
The TLC352 has internal electrostatic discharge (ESD) protection circuits and is classified with a 2000V ESD rating. However, care must be exercised in handling this device as exposure to ESD can result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0°C to 70°C. The TLC352I is characterized for operation over the industrial temperature range of −40°C to 85°C.

Device Information

T_A	V_{IO} max at 25°C	PACKAGE(1)
		SMALL-OUTLINE (D)
0°C to 70°C	5mV	TLC352CD
−40°C to 85°C	5mV	TLC352ID

(1) The D packages are available taped and reeled. Add R suffix to device type (like TLC352CDR).



Symbol (Each Comparator)

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3 Pin Configuration and Functions

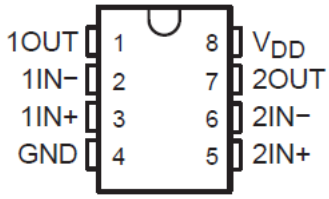


Figure 3-1. TLC352C, TLC352I D or P Package (Top View)

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			18	V
V_{ID}	Differential input voltage(3)			$\pm V_{DD}$	V
V_I	Input voltage range		–0.3	V_{DD}	V
V_O	Output voltage			18	V
I_I	Input current			±5	mA
I_O	Output current			20	mA
	Duration of output short circuit to ground(4)		Unlimited		
T_A	Operating free-air temperature range	TLC352C	0	70	°C
		TLC352I	–40	85	
	Storage temperature range		– 65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D package		260	°C
		P package			

(1) Stresses beyond those listed under “absolute maximum ratings” can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values except differential voltages are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN −.
(4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

4.2 Recommended Operating Conditions

			TLC352C		TLC352I		UNIT
			MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage		2.7	16	2.7	16	V
V_{IC}	Common-mode input voltage	V_{DD} = 5V	0	3.5	0	3.5	V
		V_{DD} = 10V	0	8.5	0	8.5	
T_A	Operating free-air temperature		0	70	−40	85	°C

4.3 Electrical Characteristics

at specified free-air temperature, V_{DD} = 2.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC352C			TLC352I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min		25°C		2	5		2	5	mV
				Full range			6.5			7	
I_{IO}	Input offset current			25°C		1			1		pA
				MAX			0.3			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				MAX			0.6			2	nA
V_{ICR}	Common-mode input voltage range			Full range	0 to 1.2			0 to 1.2			V
V_{OL}	Low-level output voltage			25°C		100	200		100	200	mV
				Full range			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5V	V_{OL} = 0.3V	25°C	1	1.6		1	1.6		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 0.5V	No load	25°C		65	150		65	150	µA
				Full range			200			200	

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, −40°C to 85°C for TLC352I.

4.4 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC352C			TLC352I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min		25°C		1	5		1	5	mV
				Full range			6.5			7	
I_{IO}	Input offset current			25°C		1			1		pA
				MAX			0.3			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				MAX			0.6			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1			0 to V_{DD} − 1			V
				Full range	0 to V_{DD} − 1.5			0 to V_{DD} − 1.5			
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1			0.1		nA
			V_{OH}= 15V	Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = 1V	I_{OL} = 4mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = − 1V	V_{OL} = 1.5V	25°C	6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1V	No load	25°C		0.15	0.3		0.15	0.3	mA
				Full range			0.4			0.4	

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, −40°C to 85°C for TLC352I.

4.5 Switching Characteristics

V_{DD} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC352C, TLC352I			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5V through 5.1kΩ C_L = 15pF(1) (2)	100mV input step with 10mV overdrive		200		ns
		100mV overdrive		100		

(1) C_L includes probe and jig capacitance
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

5 Typical Characteristics

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

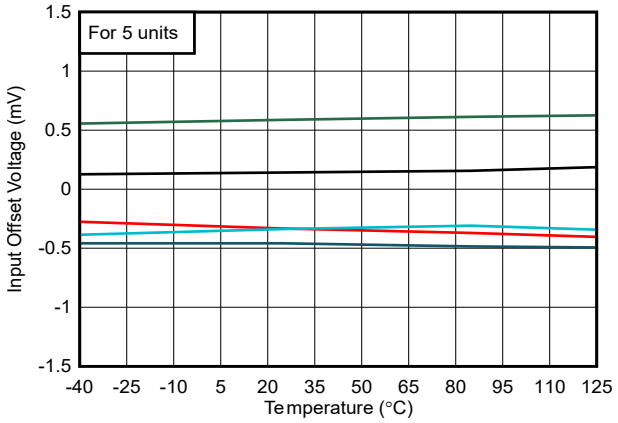


Figure 5-1. Offset vs. Temperature

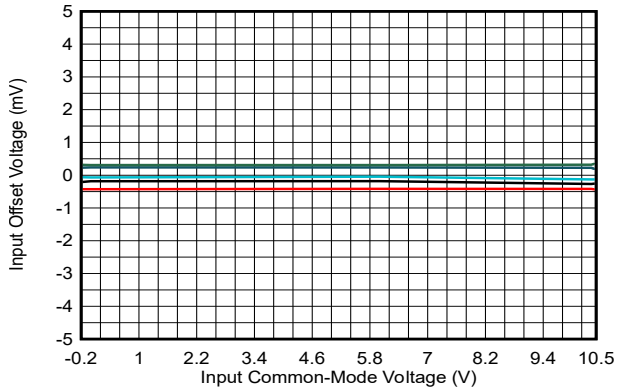


Figure 5-2. Offset Voltage vs. Common-Mode, 12V

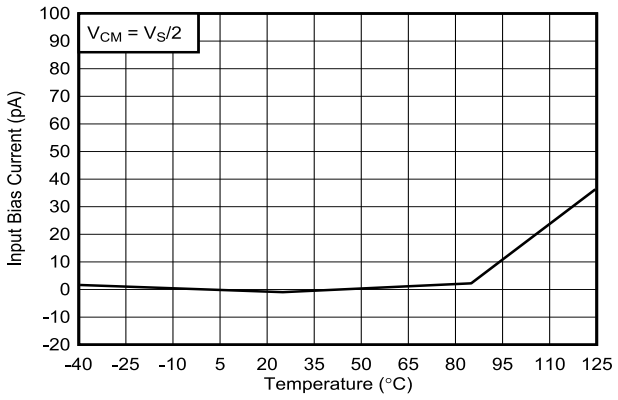


Figure 5-3. Bias Current vs. Temperature

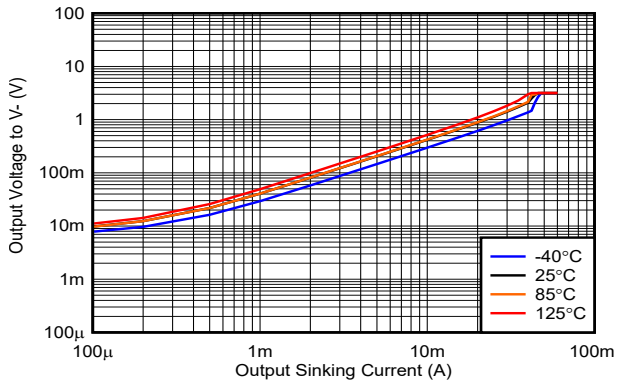


Figure 5-4. Output Voltage vs. Sinking Current, 3.3V

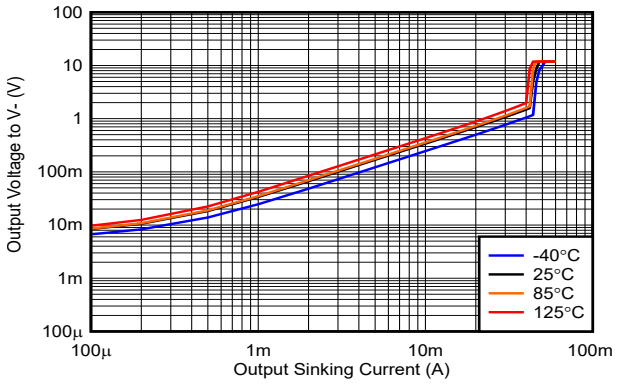


Figure 5-5. Output Voltage vs. Sinking Current, 12V

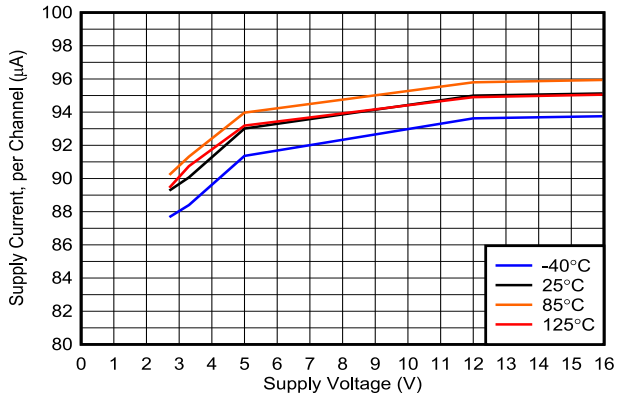


Figure 5-6. Supply Current vs. Supply Voltage, Output LOW, No Load

5 Typical Characteristics (continued)

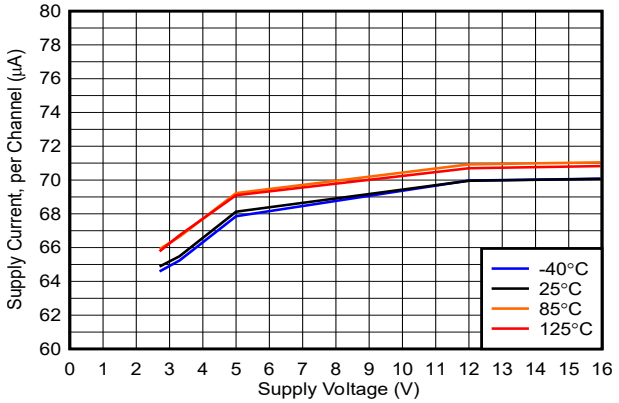


Figure 5-7. Supply Current vs. Supply Voltage, Output HIGH, No Load

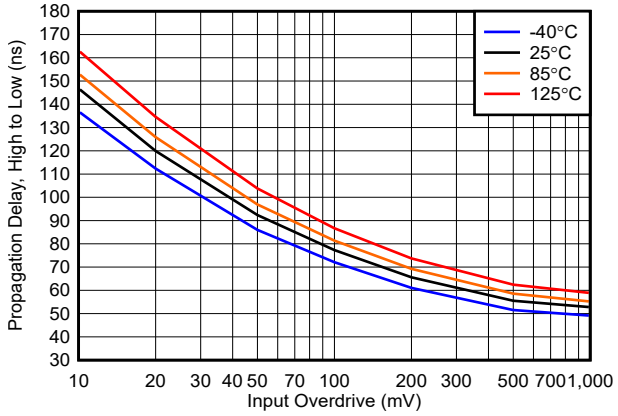


Figure 5-8. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

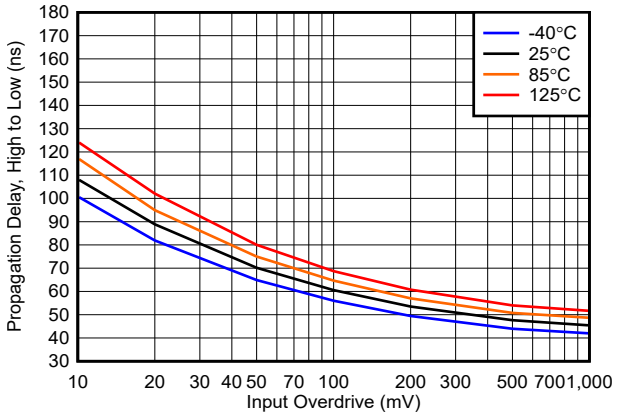


Figure 5-9. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

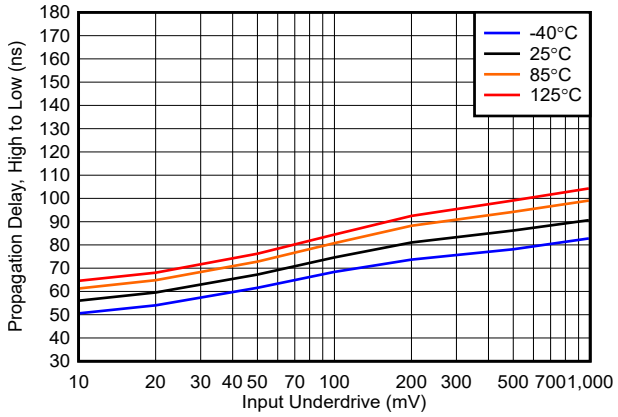


Figure 5-10. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V

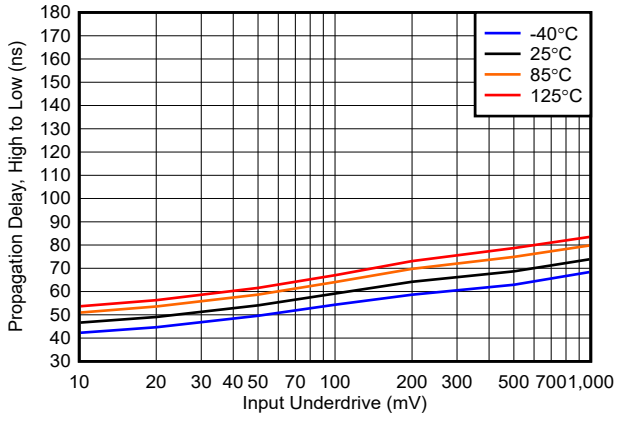


Figure 5-11. Propagation Delay, (High to Low) vs. Input Underdrive, 12V

6 Detailed Description

6.1 Overview

The TLC352 device is a micro-power comparator with open-drain output. Operating down to 3V while only consuming only 75µA per channel, the TLC372 is excellent for power conscious applications.

6.2 Functional Block Diagrams

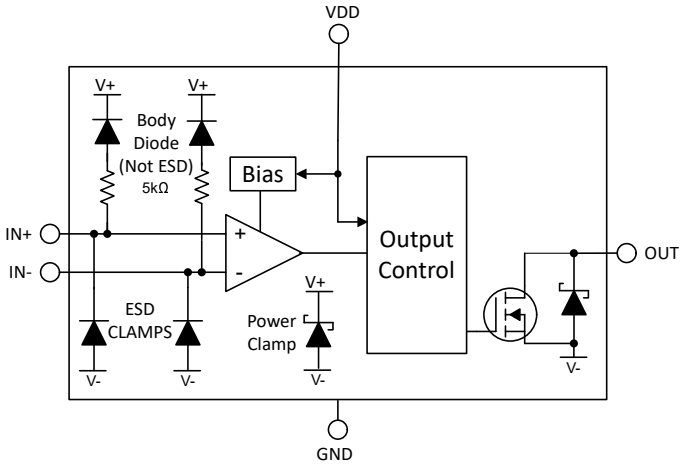


Figure 6-1. Block Diagram

6.3 Feature Description

The TLC372 comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of an open-drain output stage capable of sinking current with a negative differntial input voltage.

6.4 Device Functional Modes

6.4.1 Input

The TLC3x2 input voltage range extends from V- to 1.5V below V+ over the full temperature range. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

6.4.2 ESD Protection

The TLC3x2 input and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 300mV. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limitng the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

6.4.4 Open-Drain Output

The TLC3x2 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 16V, independent of the comparator supply voltage (VDD). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing VOL and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to VDD can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the GND pin if floating pins are not desired.

6.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 6-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

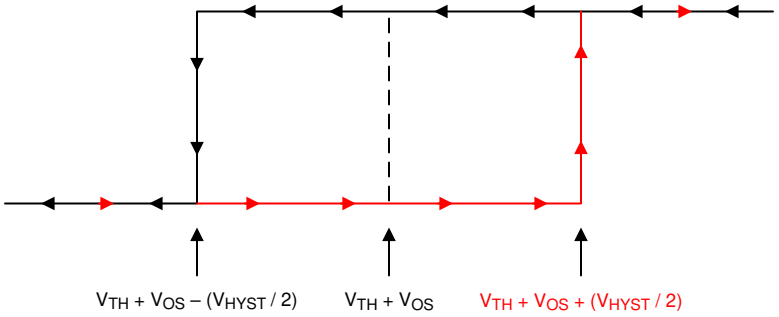


Figure 6-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

6.4.5.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

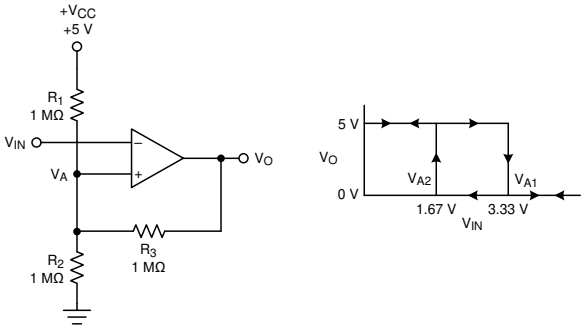


Figure 6-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

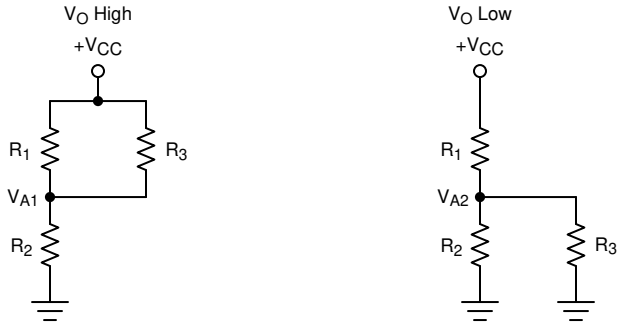


Figure 6-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown above on the right.

Use the equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

6.4.5.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 6-5.

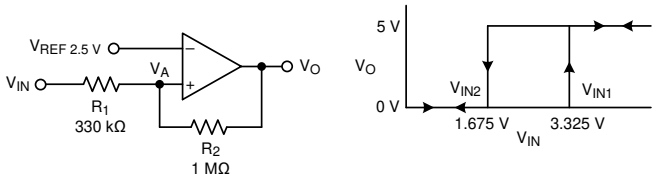


Figure 6-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 6-6.

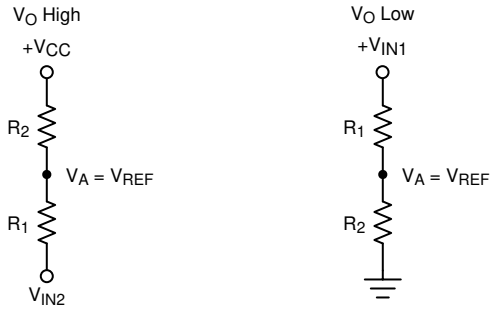


Figure 6-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2002) to Revision B (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updates throughout data sheet to reflect performance of new die	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC352CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	352C
TLC352CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	352C
TLC352CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	352C
TLC352CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC352CP
TLC352CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC352CP
TLC352ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	352I
TLC352IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	352I
TLC352IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	352I
TLC352IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC352IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC352IP
TLC352IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC352IP
TLC352IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	P352I
TLC352IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	P352I
TLC352IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P352I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

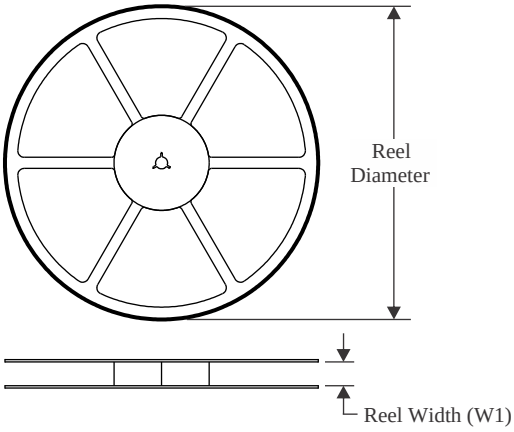
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

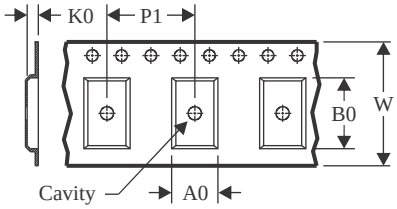
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

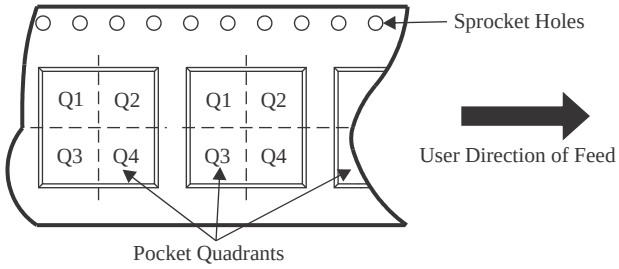


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

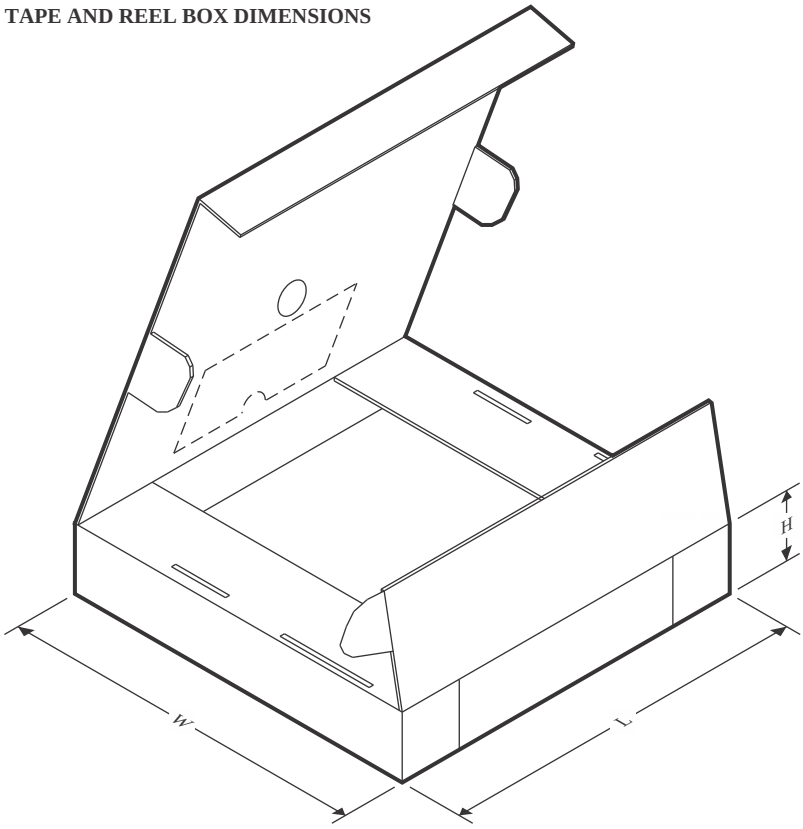
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC352CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

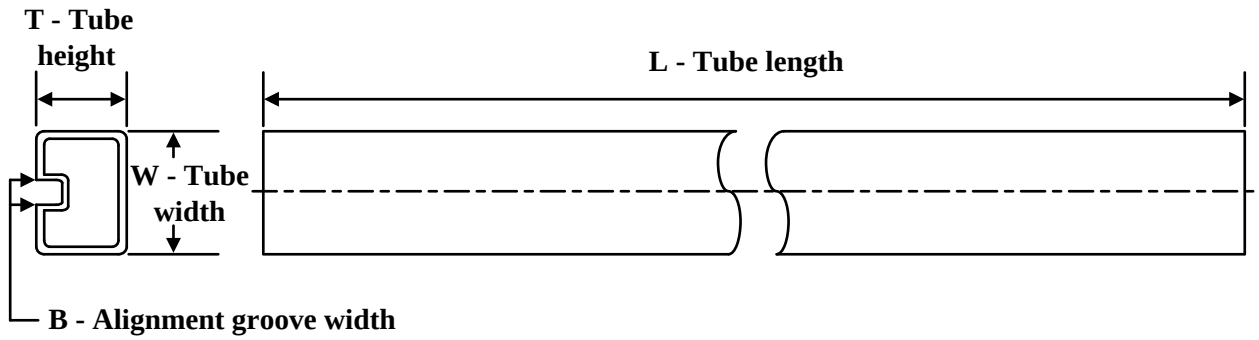
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

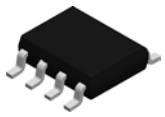
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC352CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC352IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC352IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC352CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC352CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC352IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC352IP.A	P	PDIP	8	50	506	13.97	11230	4.32

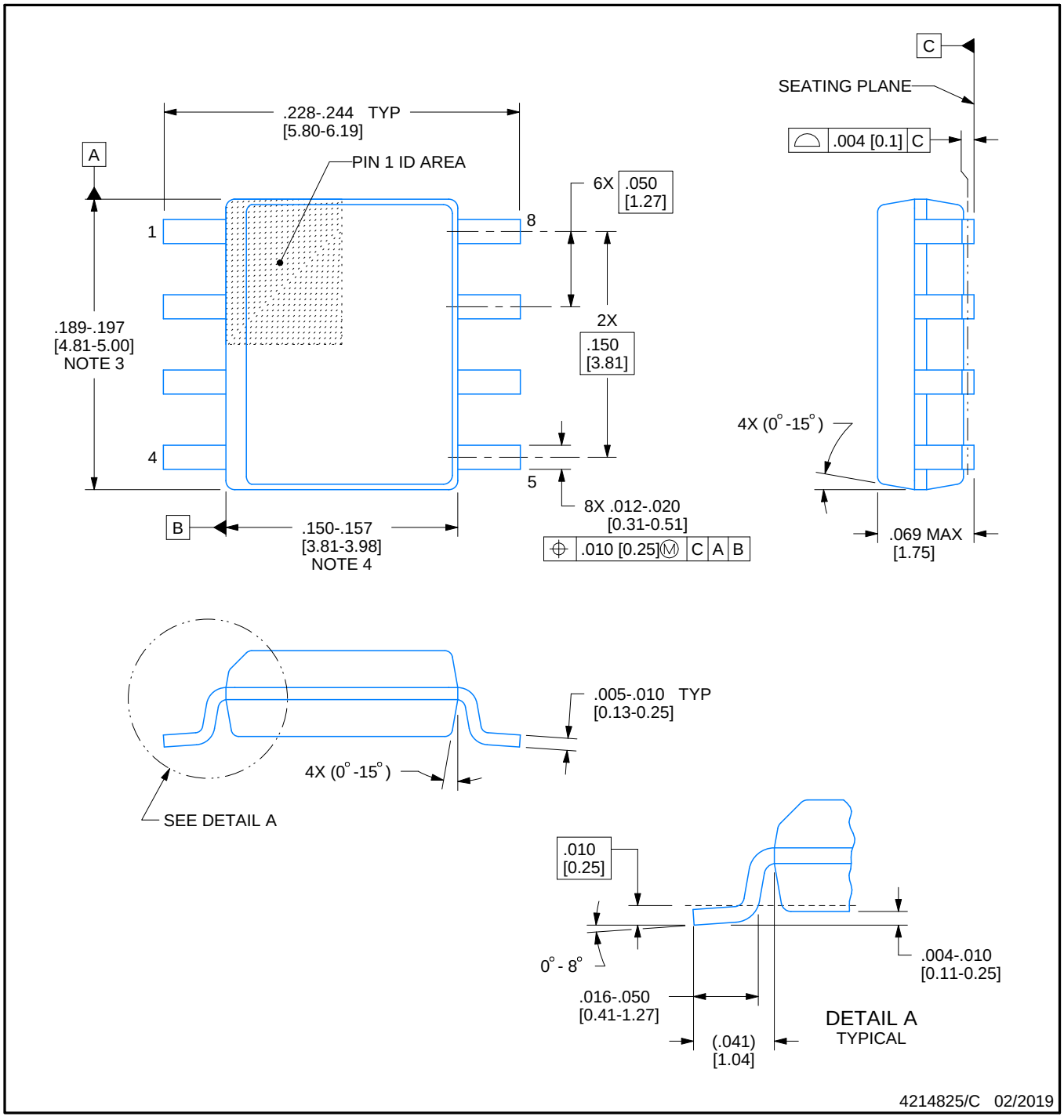


PACKAGE OUTLINE

D0008A

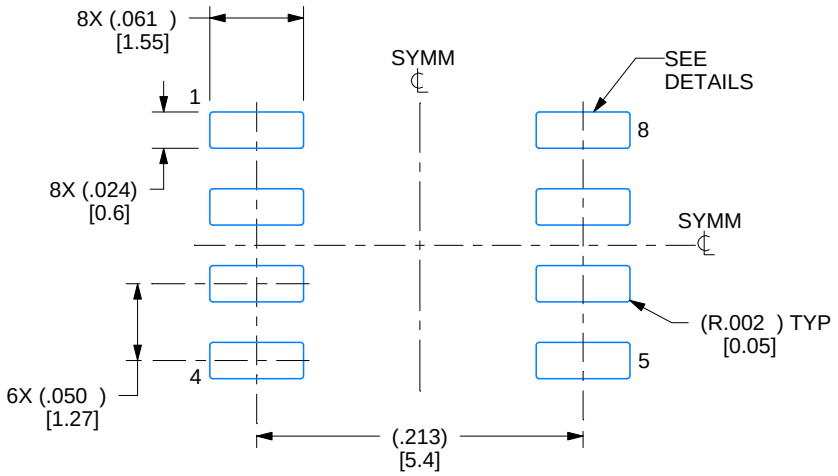
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

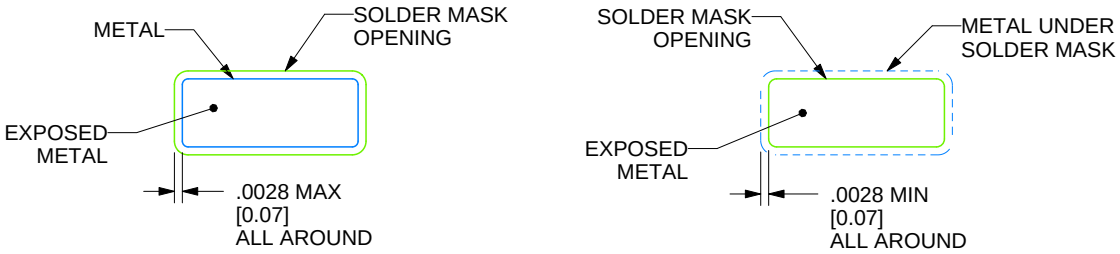


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

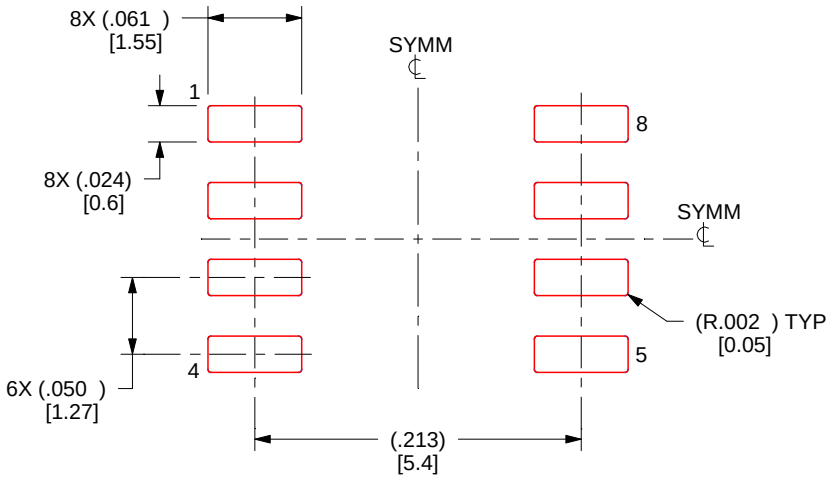
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



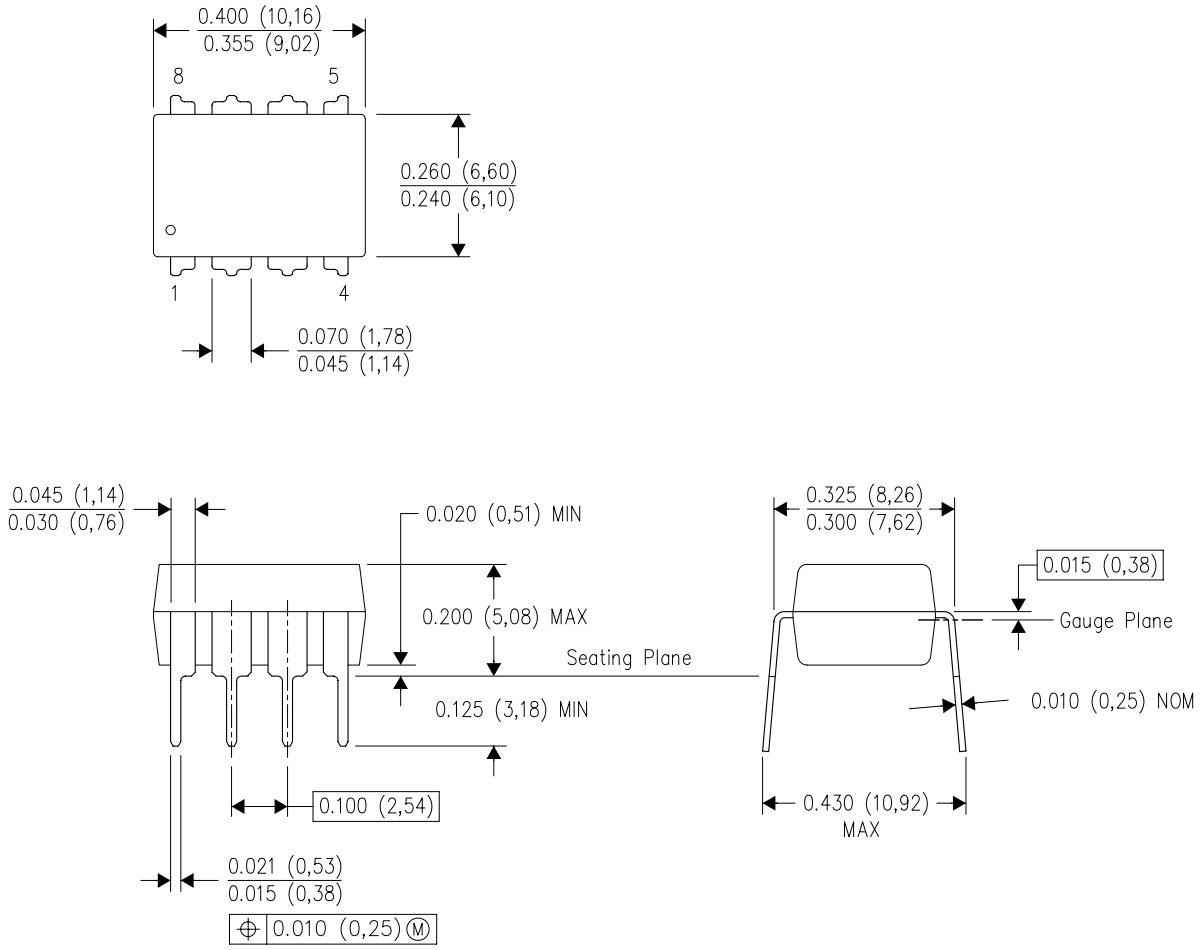
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



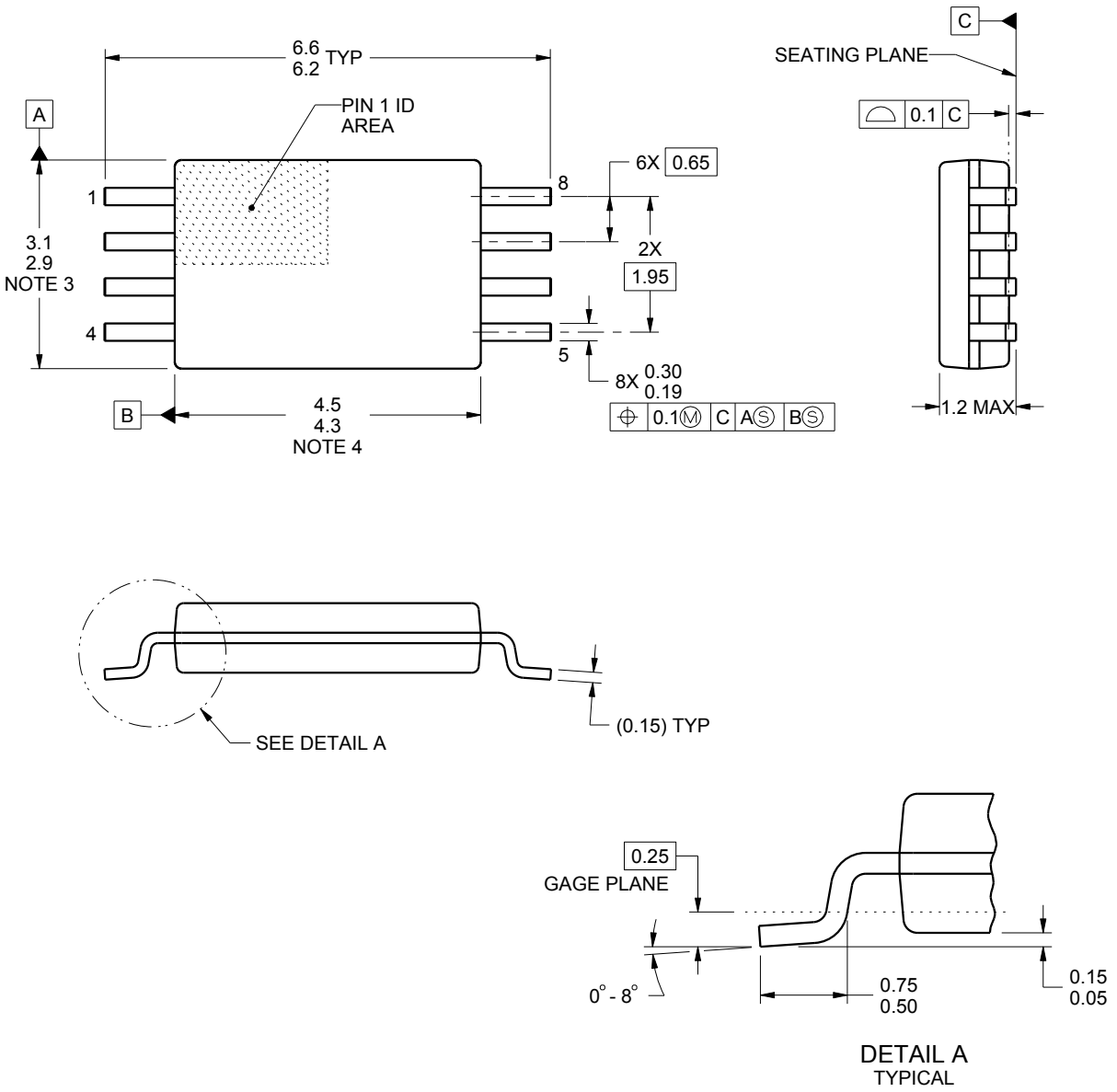
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

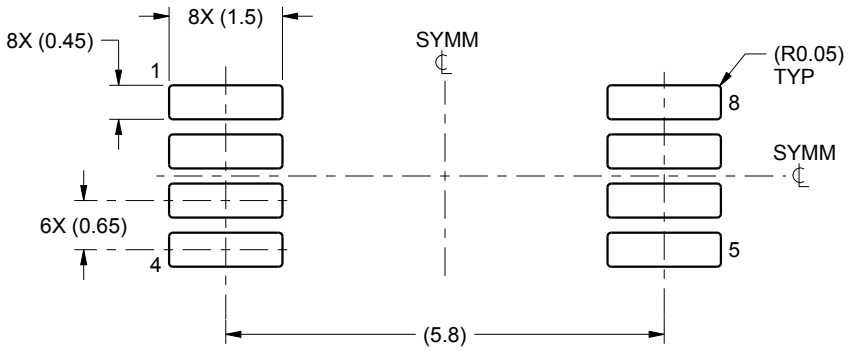
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

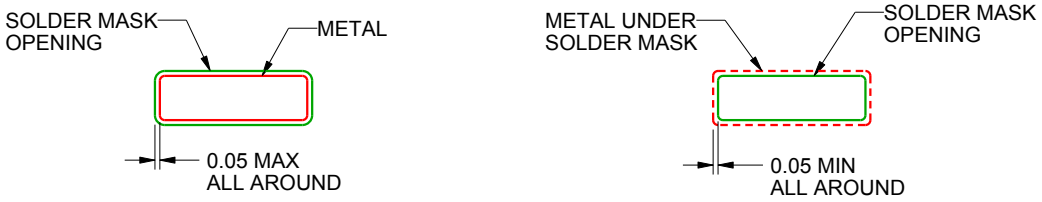


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

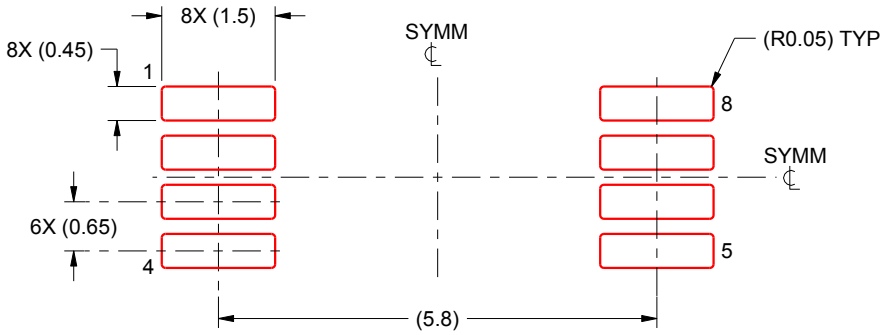


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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