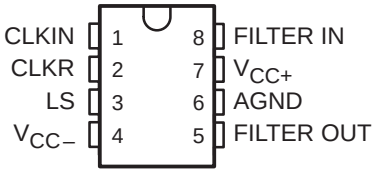
- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04/MF4A-50 . . . ±0.8%
  TLC14/MF4A-100 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range From 0.1 Hz to 30 kHz, $V_{CC\pm}$ = ±2.5 V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply-Voltage Sensitivity**
- **Designed to be Interchangeable With National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0. 8% error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) terminal.

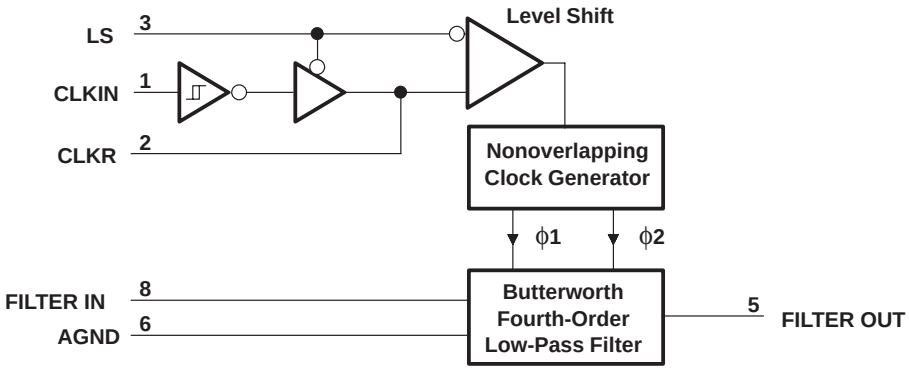
The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C. The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from –40°C to 85°C. The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1 100:1	TLC04CD/MF4A-50CD TLC14CD/MF4A-100CD	TLC04CP/MF4A-50CP TLC14CP/MF4A-100CP
–40°C to 85°C	50:1 100:1	TLC04ID/MF4A-50ID TLC14ID/MF4A-100ID	TLC04IP/MF4A-50IP TLC14IP/MF4A-100IP
–55°C to 125°C	50:1 100:1		TLC04MP/MF4A-50MP TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6	I	Analog ground. The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock in. CLKIN is the clock input terminal for CMOS-compatible clock or self-clocking options. For either option, LS is at V_{CC-}. For self-clocking, a resistor is connected between CLKIN and CLKR and a capacitor is connected from CLKIN to ground.
CLKR	2	I	Clock R. CLKR is the clock input for a TTL-compatible clock. For a TTL clock, LS is connected to midsupply and CLKIN can be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter input
FILTER OUT	5	O	Butterworth fourth-order low-pass filter output
LS	3	I	Level shift. LS accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, LS is at V_{CC-} and for TTL-compatible clocks, LS is at midsupply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range, T_A: TLC04C/MF4A-50C, TLC14C/MF4A-100C . . . . . 0°C to 70°C
TLC04I/MF4A-50I, TLC14I/MF4A-100I . . . . . –40°C to 85°C
TLC04M/MF4A-50M, TLC14M/MF4A-100M . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

		TLC04/MF4A-50		TLC14/MF4A-100		UNIT
		MIN	MAX	MIN	MAX	
Positive supply voltage, V_{CC+}		2.25	6	2.25	6	V
Negative supply voltage, V_{CC-}		–2.25	–6	–2.25	–6	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
Clock frequency, f_{clock} (see Note 2)	$V_{CC\pm}$ = ±2.5 V	5	1.5×10^6	5	1.5×10^6	Hz
	$V_{CC\pm}$ = ±5 V	5	2×10^6	5	2×10^6	
Cutoff frequency, f_{co} (see Note 3)		0.1	40×10^3	0.05	20×10^3	Hz
Operating free-air temperature, T_A	TLC04C/MF4A-50C, TLC14C/MF4A-100C	0	70	0	70	°C
	TLC04I/MF4A-50I, TLC14I/MF4A-100I	–40	85	–40	85	
	TLC04M/MF4A-50M, TLC14M/MF4A-100M	–55	125	–55	125	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = –2.5 V, $f_{clock} \le$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OO}	Output offset voltage				25			50		mV
V_{OM}	Peak output voltage	V_{OM+}	R_L = 10 kΩ	1.8	2		1.8	2		V
		V_{OM-}		–1.25	–1.7		–1.25	–1.7		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		–0.5			–0.5		mA
		Sink			4			4		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.2	2.25		1.2	2.25	mA

‡ All typical values are at T_A = 25°C.

NOTE 4: $I_{OS(source)}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal $I_{OS(sink)}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, $f_{clock} \leq$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50 MIN	TLC04/MF4A-50 TYP†	TLC04/MF4A-50 MAX	TLC14/MF4A-100 MIN	TLC14/MF4A-100 TYP†	TLC14/MF4A-100 MAX	UNIT
V_{OO}	Output offset voltage				150			200		mV
V_{OM}	Peak output voltage	V_{OM+}	R_L = 10 kΩ	3.75	4.3		3.75	4.5		V
		V_{OM-}		−3.75	−4.1		−3.75	−4.1		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−2			−2		mA
		Sink			5			5		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.8	3		1.8	3	mA
k_{SVS}	Supply voltage sensitivity (see Figures 1 and 2)				−30			−30		dB

† All typical values are at T_A = 25°C.

NOTE 4: $I_{OS(source)}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal. $I_{OS(sink)}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.

clocking section

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		6.1	7	8.9	V
			V_{CC+} = 5 V, V_{CC-} = 0		3.1	3.5	4.4	
V_{IT-}	Negative-going input threshold voltage		V_{CC+} = 10 V, V_{CC-} = 0		1.3	3	3.8	V
			V_{CC+} = 5 V, V_{CC-} = 0		0.6	1.5	1.9	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		V_{CC+} = 10 V, V_{CC-} = 0		2.3	4	7.6	V
			V_{CC+} = 5 V, V_{CC-} = 0		1.2	2	3.8	
V_{OH}	High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
			V_{CC} = 5 V		4.5			
V_{OL}	Low-level output voltage		V_{CC} = 10 V	I_O = 10 μA			1	V
			V_{CC} = 5 V				0.5	
	Input leakage current		V_{CC} = 10 V	LS at midsupply, T_A = 25°C			2	μA
			V_{CC} = 5 V				2	
I_O	Output current		V_{CC} = 10 V	CLKR and CLKIN shortened to V_{CC-}	−3	−7		mA
			V_{CC} = 5 V		−0.75	−2		
			V_{CC} = 10 V	CLKR and CLKIN shortened to V_{CC+}	3	7		mA
			V_{CC} = 5 V		0.75	2		

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		1.5	3		1.5	3		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \le 250$ kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	Hz/Hz
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \le 250$ kHz			±25			±25		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.46	−1.3				
	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \le 250$ kHz		24	25		24	25		dB
Voltage amplification, dc	$f_{clock} \le 250$ kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			5			5		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
5. The frequency responses at f are referenced to a dc gain of 0 dB.
6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 μV rms for the TLC04/MF4A-50 and 135 μV rms for the TLC14/MF4A-100.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		2	4		2	4		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \le 250$ kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	Hz/Hz
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \le 250$ kHz			±15			±15		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.44	−1.3				
	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 6)	T_A = 25°C			86			84		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \le 250$ kHz		24	25		24	25		dB
Voltage amplification, dc	$f_{clock} \le 250$ kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			7			7		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
5. The frequency responses at f are referenced to a dc gain of 0 dB.
6. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 μV rms for the TLC04/MF4A-50 and 178 μV rms for the TLC14/MF4A-100.

TYPICAL CHARACTERISTICS

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC+} RIPPLE FREQUENCY

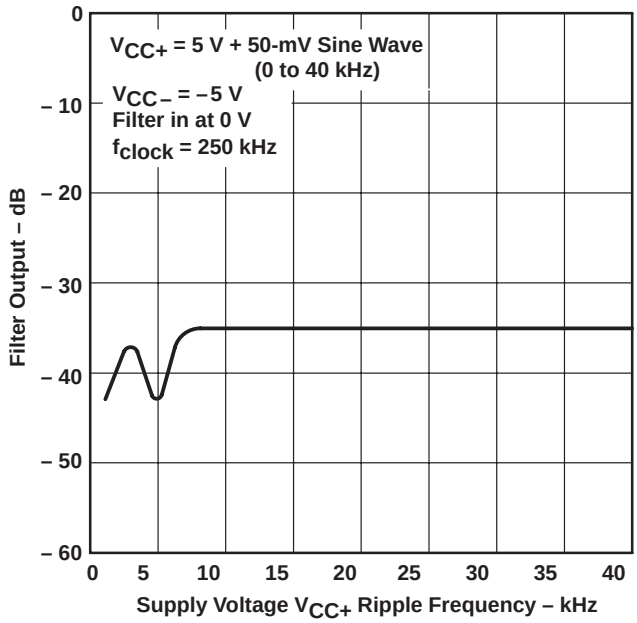


Figure 1

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC-} RIPPLE FREQUENCY

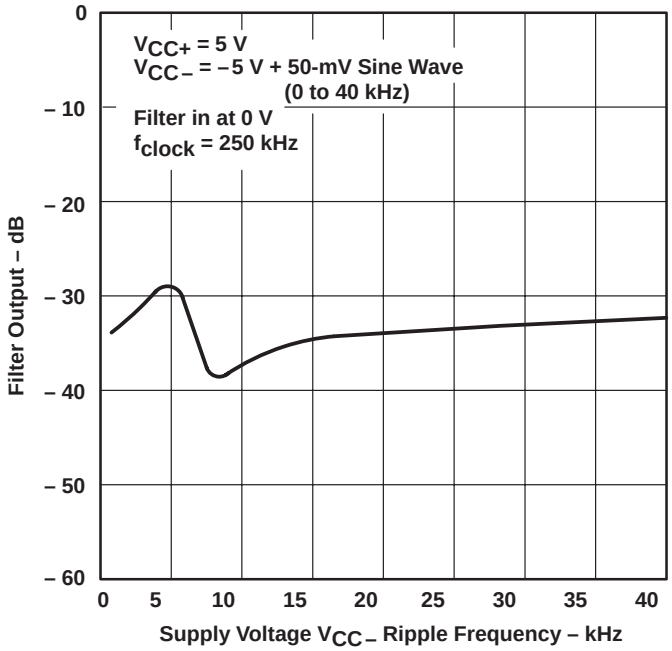


Figure 2

APPLICATION INFORMATION

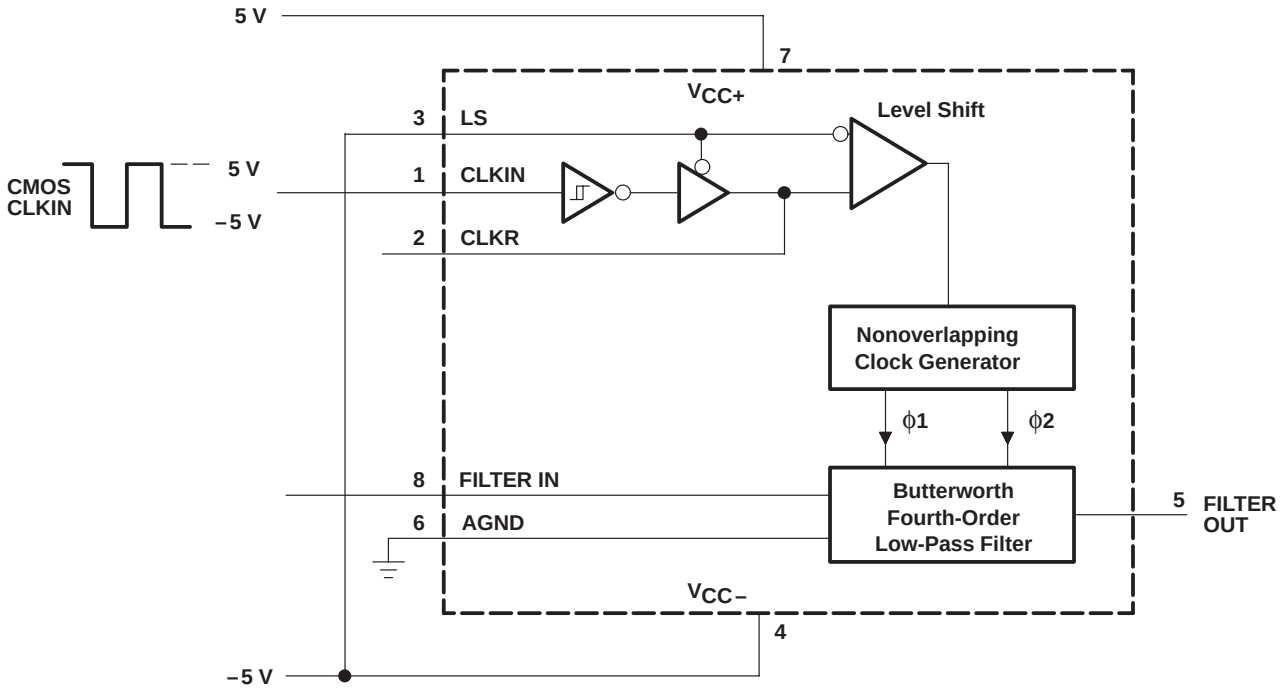


Figure 3. CMOS-Clock-Driven Dual-Supply Operation

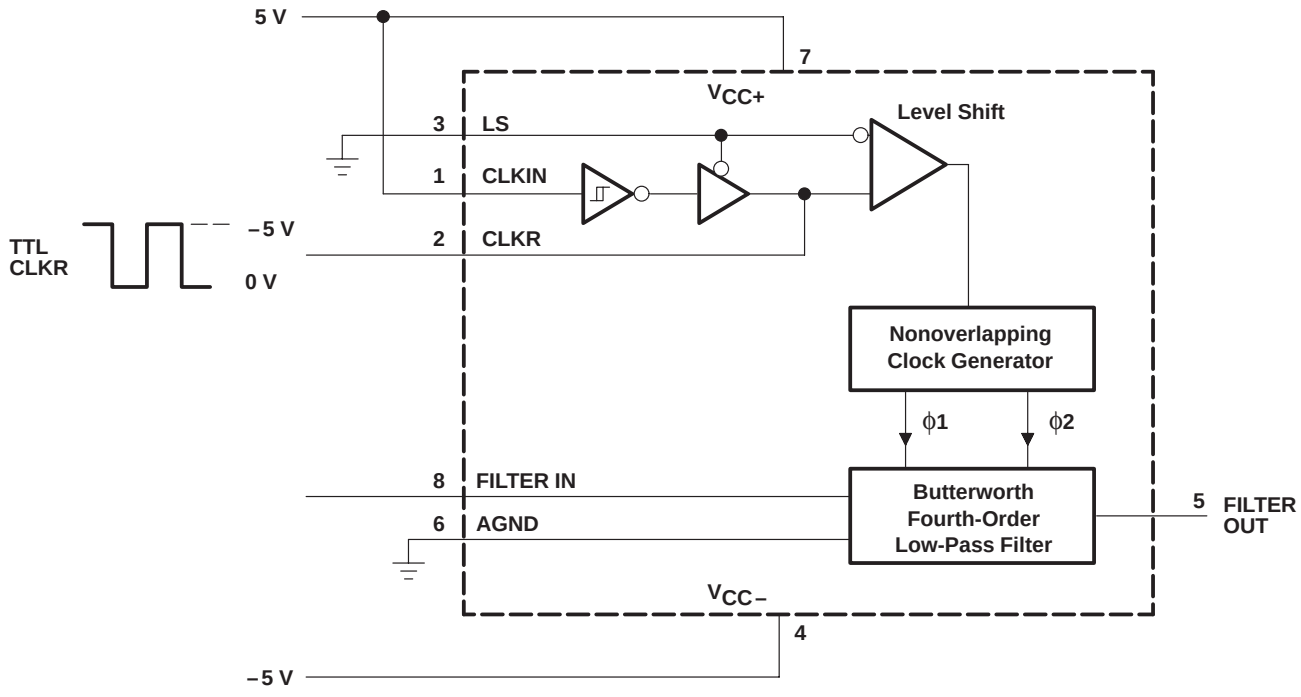
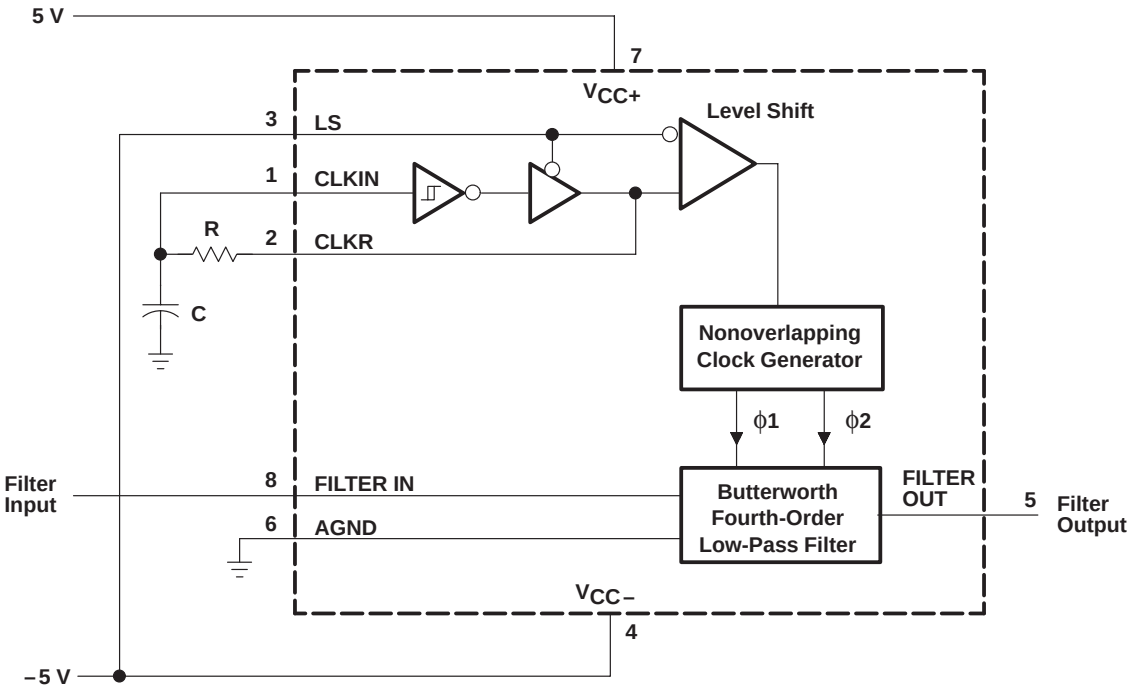


Figure 4. TTL-Clock-Driven Dual-Supply Operation

APPLICATION INFORMATION



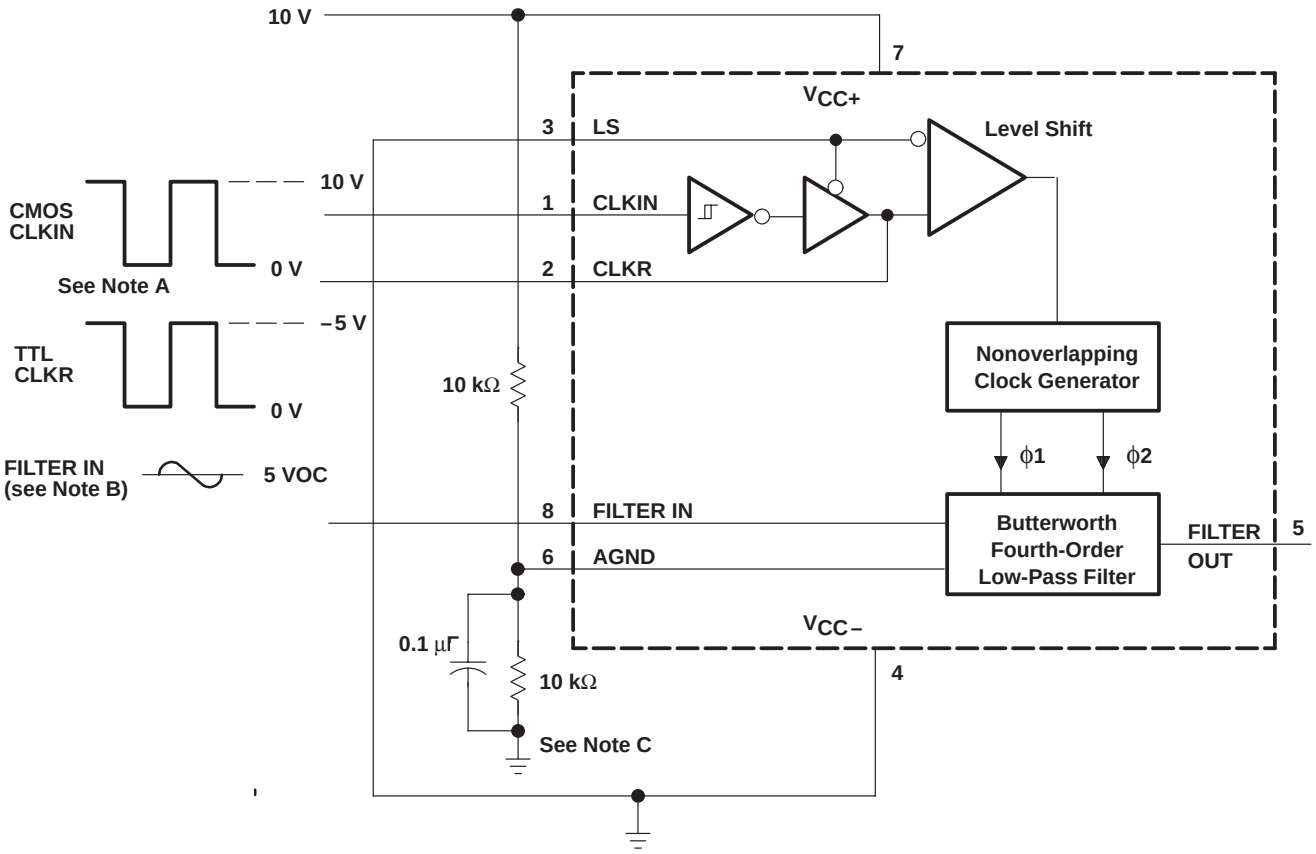
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC}-V_{IT-}}{V_{CC}-V_{IT+}}\right)\left(\frac{V_{IT+}}{V_{IT-}}\right)\right]}$$

For V_{CC} = 10 V

$$f_{clock} = \frac{1}{1.69\ RC}$$

Figure 5. Self-Clocking Through Schmitt-Trigger Oscillator Dual-Supply Operation

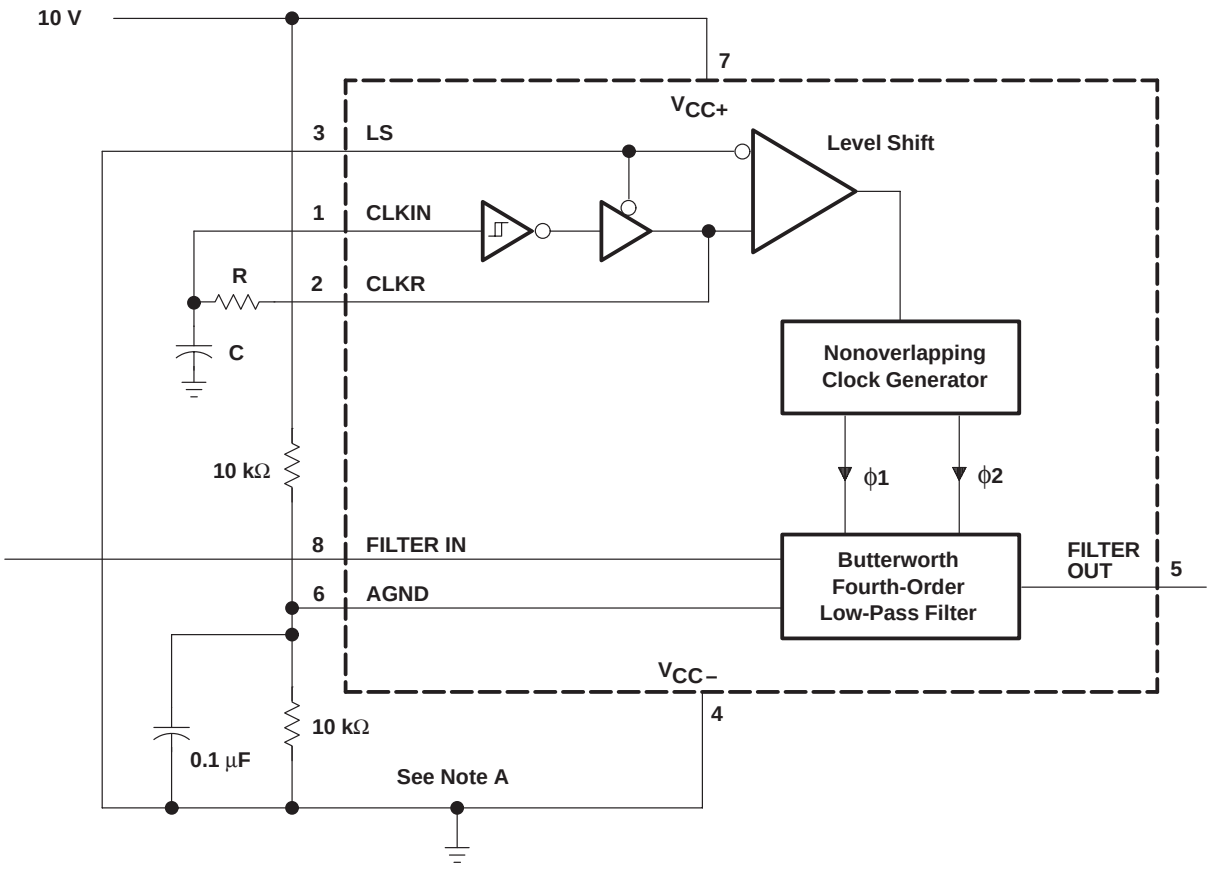
APPLICATION INFORMATION



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The filter input signal should be dc-biased to midsupply or ac-coupled to the terminal.
C. AGND must be biased to midsupply.

Figure 6. External-Clock-Driven Single-Supply Operation

APPLICATION INFORMATION



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC}-V_{IT-}}{V_{CC}-V_{IT+}}\right)\left(\frac{V_{IT+}}{V_{IT-}}\right)\right]}$$

For V_{CC} = 10 V

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: AGND must be biased to midsupply.

Figure 7. Self Clocking Through Schmitt-Trigger Oscillator Single-Supply Operation

APPLICATION INFORMATION

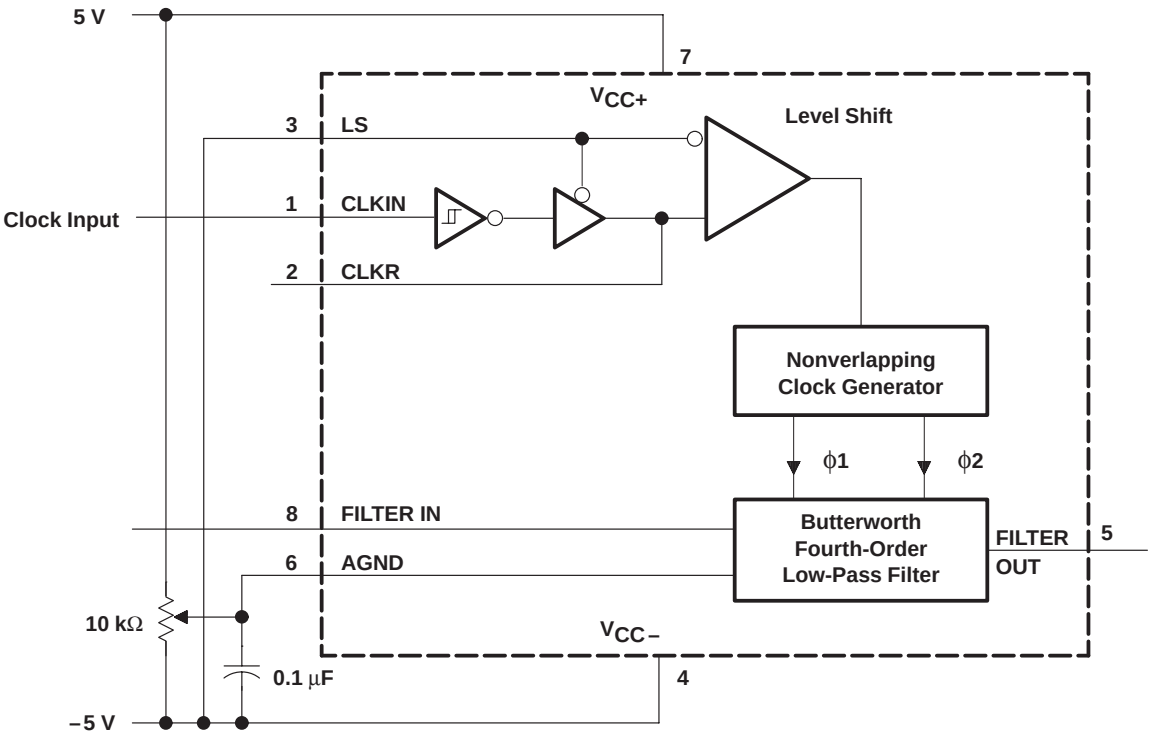


Figure 8. DC Offset Adjustment

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC04CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC04C
TLC04CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC04C
TLC04ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC04I
TLC04ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC04I
TLC04IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC04I
TLC04IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC04I
TLC14CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC14C
TLC14CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC14C
TLC14ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC14I
TLC14ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC14I
TLC14IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC14I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

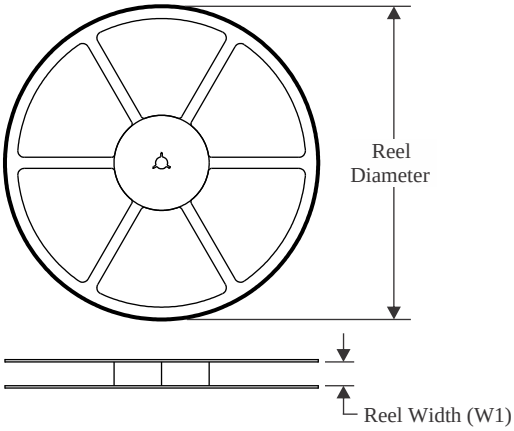
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

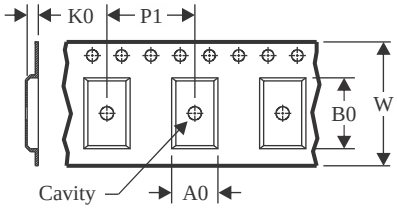
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

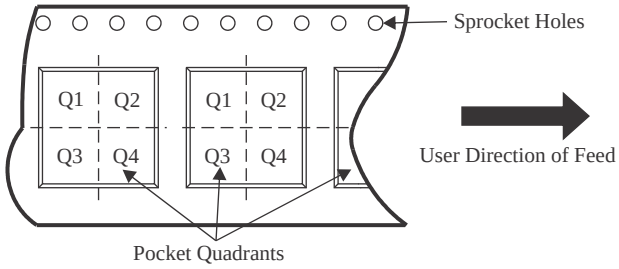


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

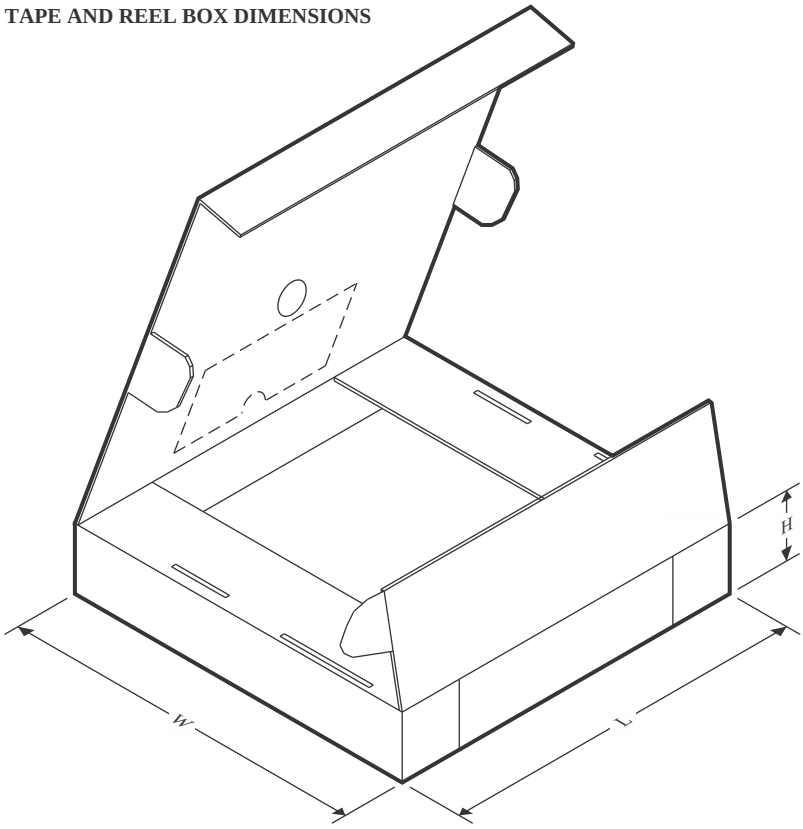
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC04IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

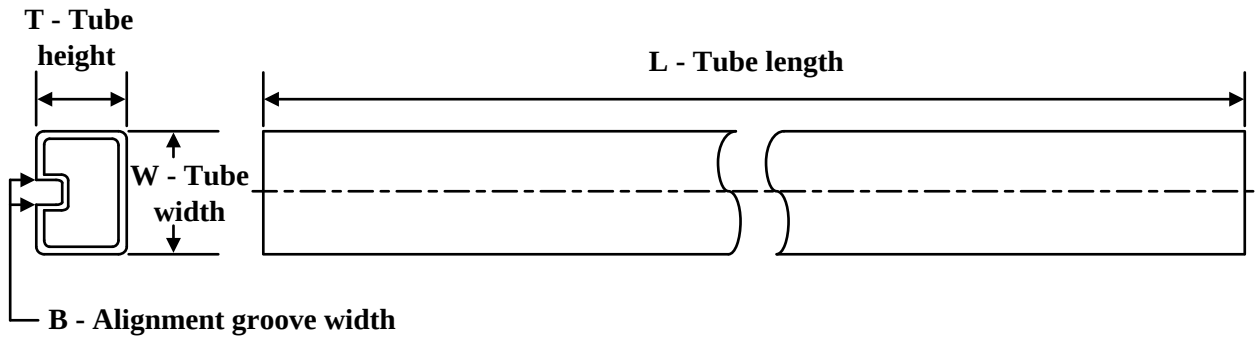
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

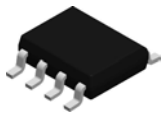
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC04IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC04CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC04CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC04ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC04ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC14CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC14CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC14ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC14ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC14IDG4	D	SOIC	8	75	505.46	6.76	3810	4

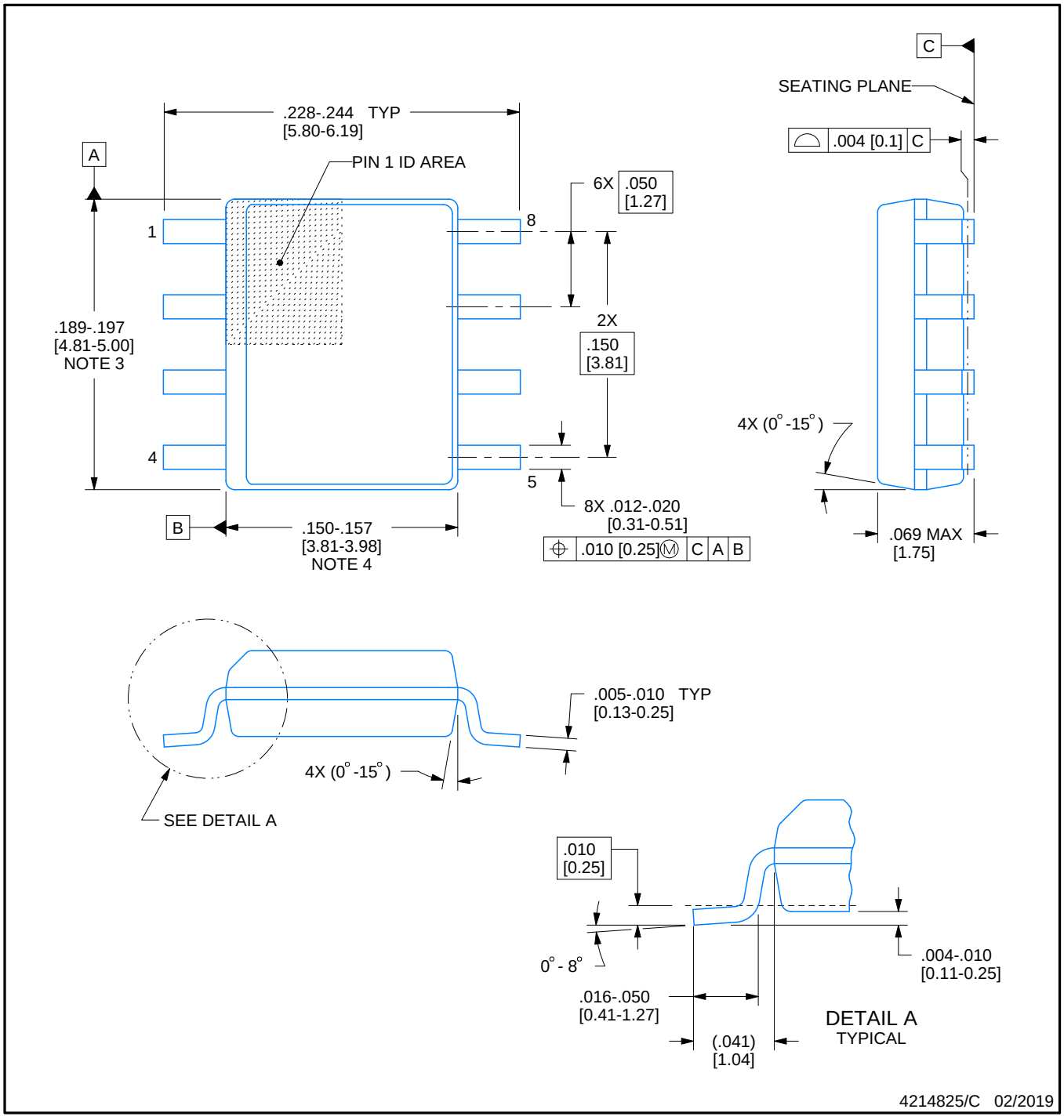


PACKAGE OUTLINE

D0008A

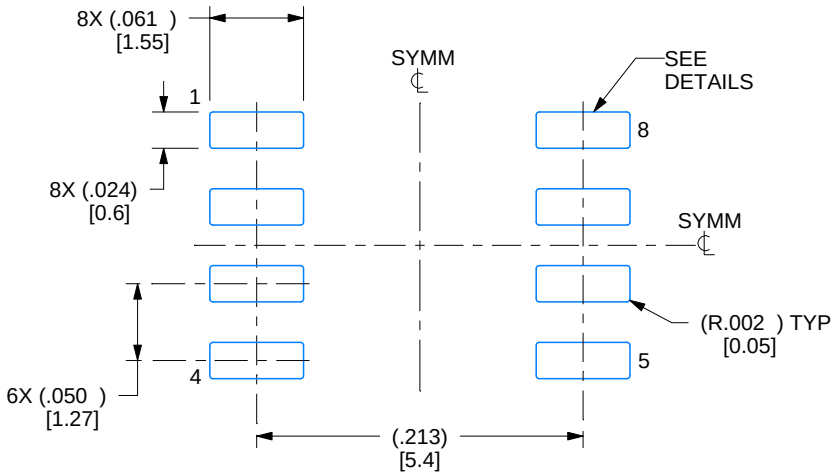
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

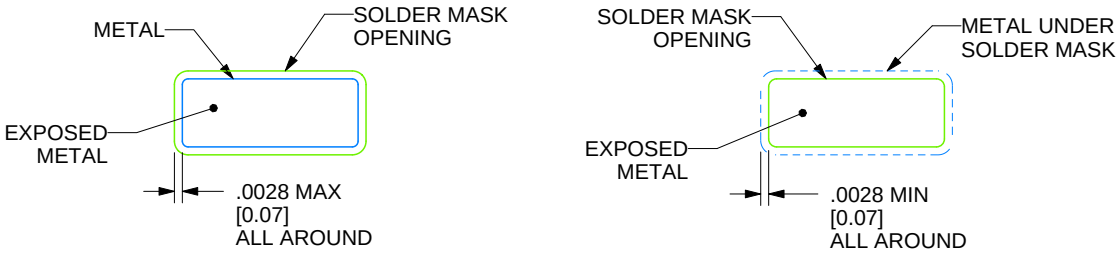


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

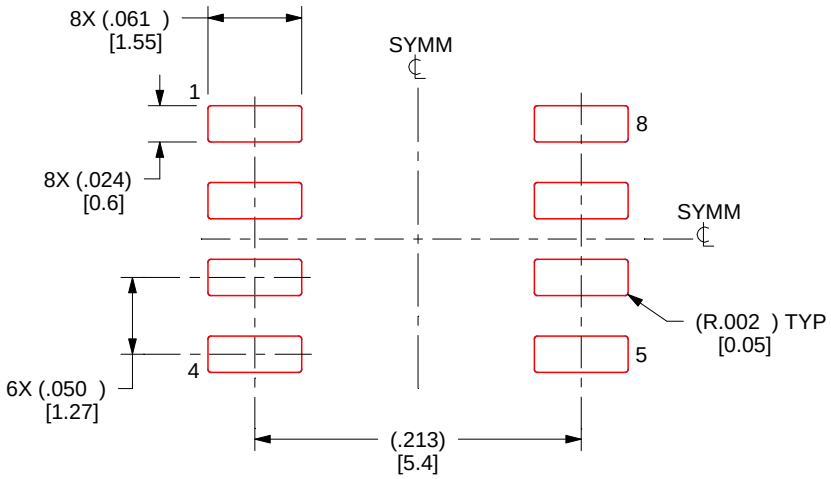
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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