TL7700-SEP 采用增强型航天塑料的耐辐射电源电压监控器

1 特性

- VID V62/19602
- 耐辐射
  - 单粒子锁定 (SEL) 在 125°C 下的抗扰度可达 43MeV-cm^2/mg
  - 每个晶圆批次的 RLAT 总电离剂量 (TID) 高达 20krad(Si)
- 增强型航天塑料
  - 受控基线
  - 金线
  - NiPdAu 铅涂层
  - 一个组装和测试基地
  - 一个制造基地
  - 支持军用（ –55°C 至 125°C ）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
  - 采用增强型模塑化合物实现低释气
- 可通过两个外部电阻器来调节检测电压
- 1% 检测电压容差 (25°C)
- 可调节检测电压的迟滞
- 宽工作电源电压范围：1.8V 至 40V
- 低功耗：I_{CC} = 0.6mA（典型值），V_{CC} = 40V

2 应用

- 近地轨道 (LEO) 航天应用
- 适用于卫星的电源监控器
- 监控 DPS、MCU、FPGA 和 ASIC

3 说明

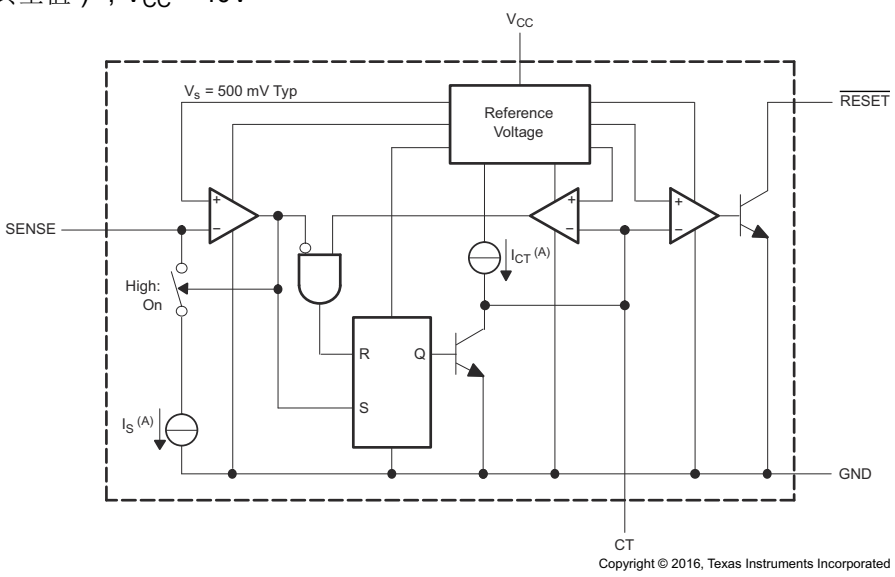
TL7700-SEP 是一款专为用作微型计算机和微处理器系统中的复位控制器而设计的双极集成电路。使用两个外部电阻器可将检测电压设置为大于 0.5V 的任何值。

电路功能非常稳定，电源电压范围为 1.8V 至 40V。由于具有超小的电源电流，该器件可用于交流线路供电型应用和便携式电池供电型应用。TL7700-SEP 器件的设计工作温度范围是 –55°C 至 125°C。

器件信息

器件型号(1)	封装	尺寸和质量（标称值）(2)
V62/19602	TSSOP (8)	3.00mm × 4.40mm 质量 = 39.47 mg

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 质量误差在 ±10% 以内。



功能方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 2019) to Revision A (August 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向“器件信息”表添加了封装质量并从 *说明* 部分删除了汽车应用	1
• Removed MIN and MAX values for SENSE input current [25°C] in the *Electrical Characteristics* section	5
• Changed MIN value for SENSE input current [– 55°C to 125°C], From 1.5 µA : To 1 µA, in the *Electrical Characteristics* section	5
• Changed MIN value for Timing-capacitor charge current [25°C], From 11 µA : To 8 µA, in the *Electrical Characteristics* section	5
• Added more variables to the t_{po} equation in the *Output Pulse-Duration Setting* section	12
• Added equations to demonstrate an example calculation in the *Detailed Design Procedure* section	13

5 Pin Configuration and Functions

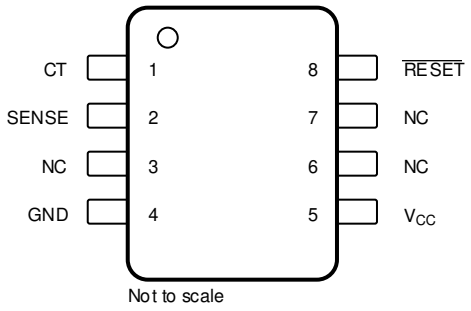


图 5-1. PW Package
8-Pin TSSOP
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	1	I/O	Timing capacitor connection This terminal sets the RESET output pulse duration (t_{po}). It is connected internally to a 15-µA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 µs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active, and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or tri-state buffer (in the low-level or high-impedance state).
GND	4	—	Ground Keep this terminal as low impedance as possible to reduce circuit noise.
NC	3, 6, 7	—	No internal connection.
$\overline{\text{RESET}}$	8	O	Reset output This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.
SENSE	2	I	Voltage sense This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
V_{CC}	5	—	Power supply This terminal is used in an operating-voltage range of 1.8 V to 40 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		41	V
V_s	SENSE input voltage	–0.3	41	V
V_{OH}	Output voltage (off state)		41	V
I_{OL}	Output current (on state)		5	mA
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.8	40	V
I_{OL}	Low-level output current		3	mA
T_A	Operating free-air temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL7700-SEP PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_s	SENSE input voltage		–55°C to 125°C	490		520	mV
I_s	SENSE input current	V_s = 0.4 V	25°C		2.5		µA
			–55°C to 125°C	1		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_s = 0.6 V, no load	25°C		0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA	25°C			0.4	V
		I_{OL} = 3 mA	25°C			0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_s = 0.6 V	–55°C to 125°C			1	µA
I_{CT}	Timing-capacitor charge current	V_s = 0.6 V	25°C	8	15	19	µA

6.6 Switching Characteristics

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF (see 图 7-5)	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF (see 图 7-5)	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (see 图 7-5)			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (see 图 7-5)			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF (see 图 7-5)			10	µs

6.7 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating conditions.

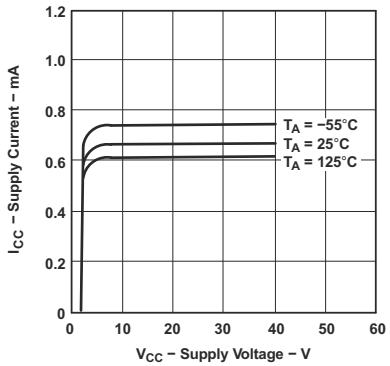


图 6-1. Supply Current vs Supply Voltage

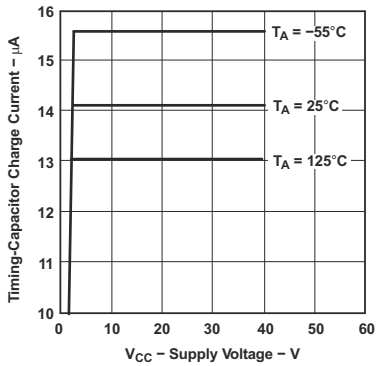


图 6-2. Timing Capacitor Charge Current vs Supply Voltage

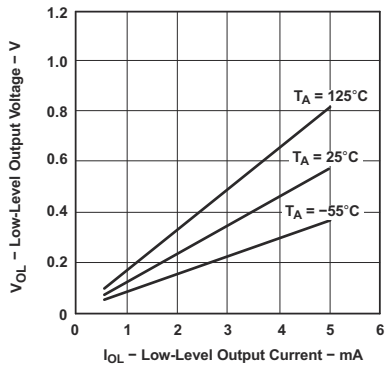


图 6-3. V_{OL} vs I_{OL}

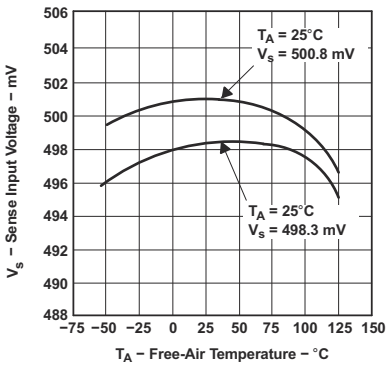


图 6-4. Sense Input Voltage vs Temperature

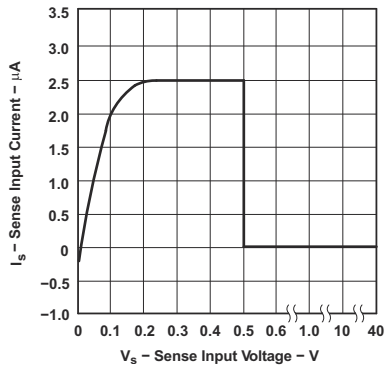


图 6-5. Sense Input Current vs Sense Input Voltage

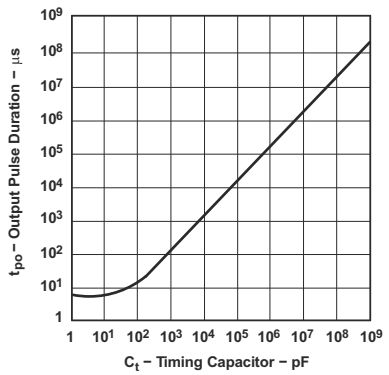


图 6-6. Output Pulse Duration vs Timing Capacitor

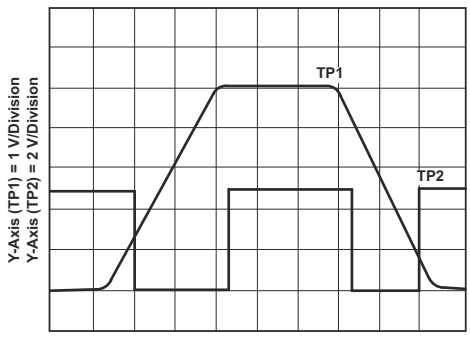


图 6-7. V_{CC} vs Output Waveform 1 - See 图 6-8

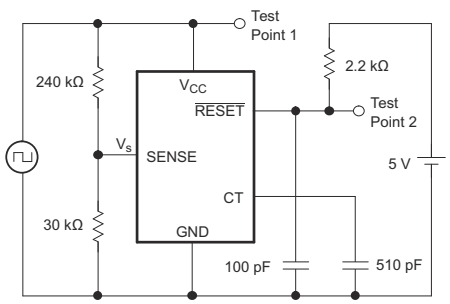


图 6-8. V_{CC} vs Output Test Circuit 1

6.7 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating conditions.

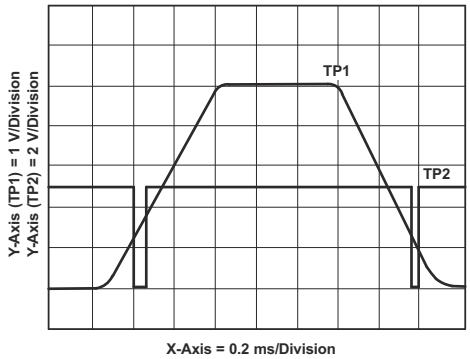


图 6-9. V_{CC} vs Output Waveform 2 - See 图 6-10

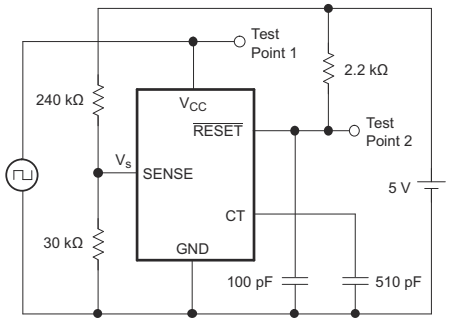


图 6-10. V_{CC} vs Output Test Circuit 2

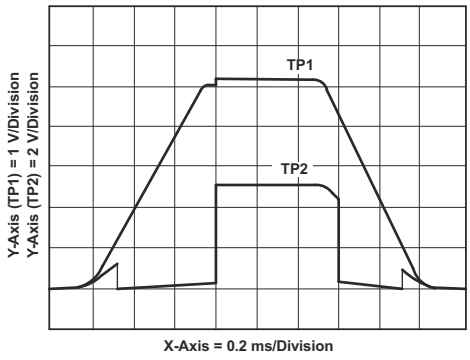


图 6-11. V_{CC} vs Output Waveform 3 - See 图 6-12

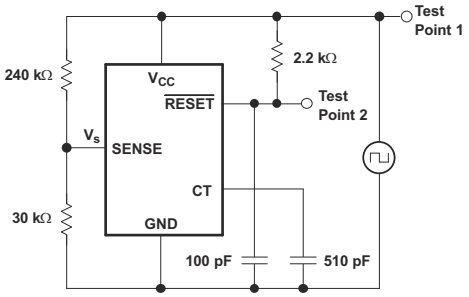


图 6-12. V_{CC} vs Output Test Circuit 3

7 Parameter Measurement Information

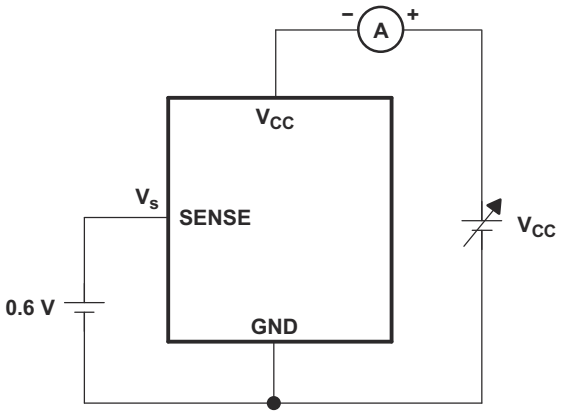


图 7-1. V_{CC} vs I_{CC} Measurement Circuit

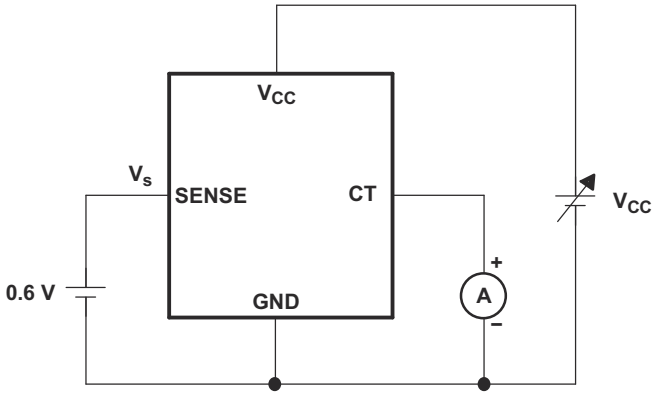


图 7-2. V_{CC} vs I_{CT} Measurement Circuit

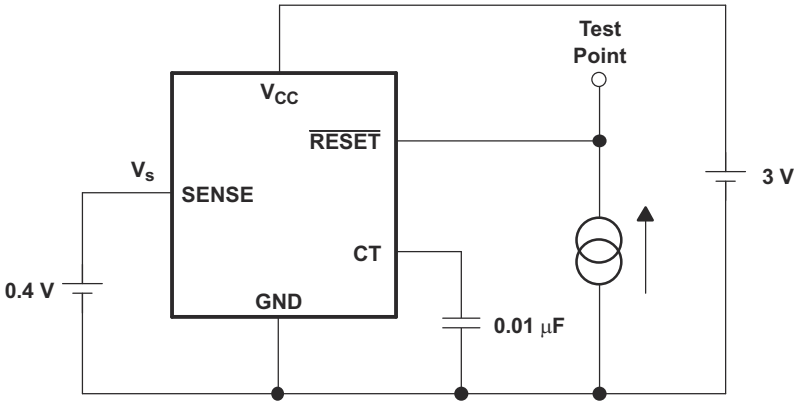


图 7-3. I_{OL} vs V_{OL} Measurement Circuit

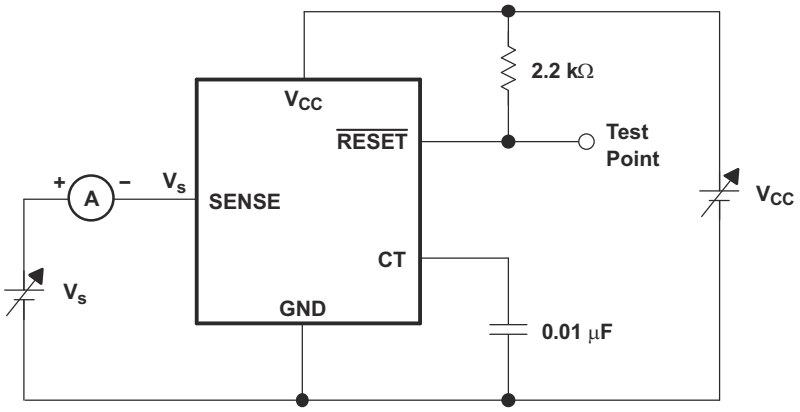


图 7-4. V_s and I_s Characteristics Measurement Circuit

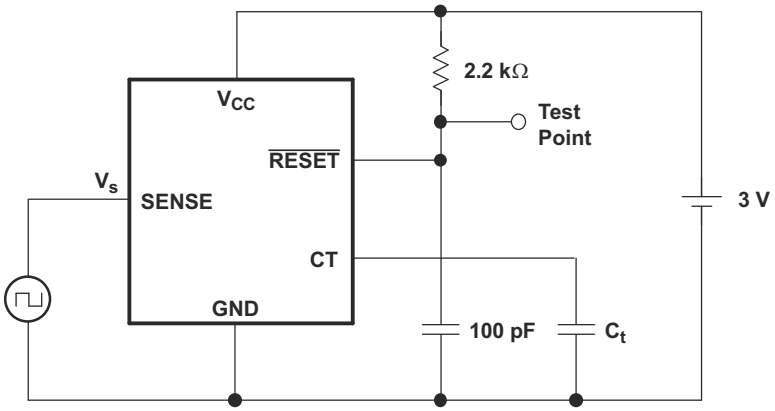


图 7-5. Switching Characteristics Measurement Circuit

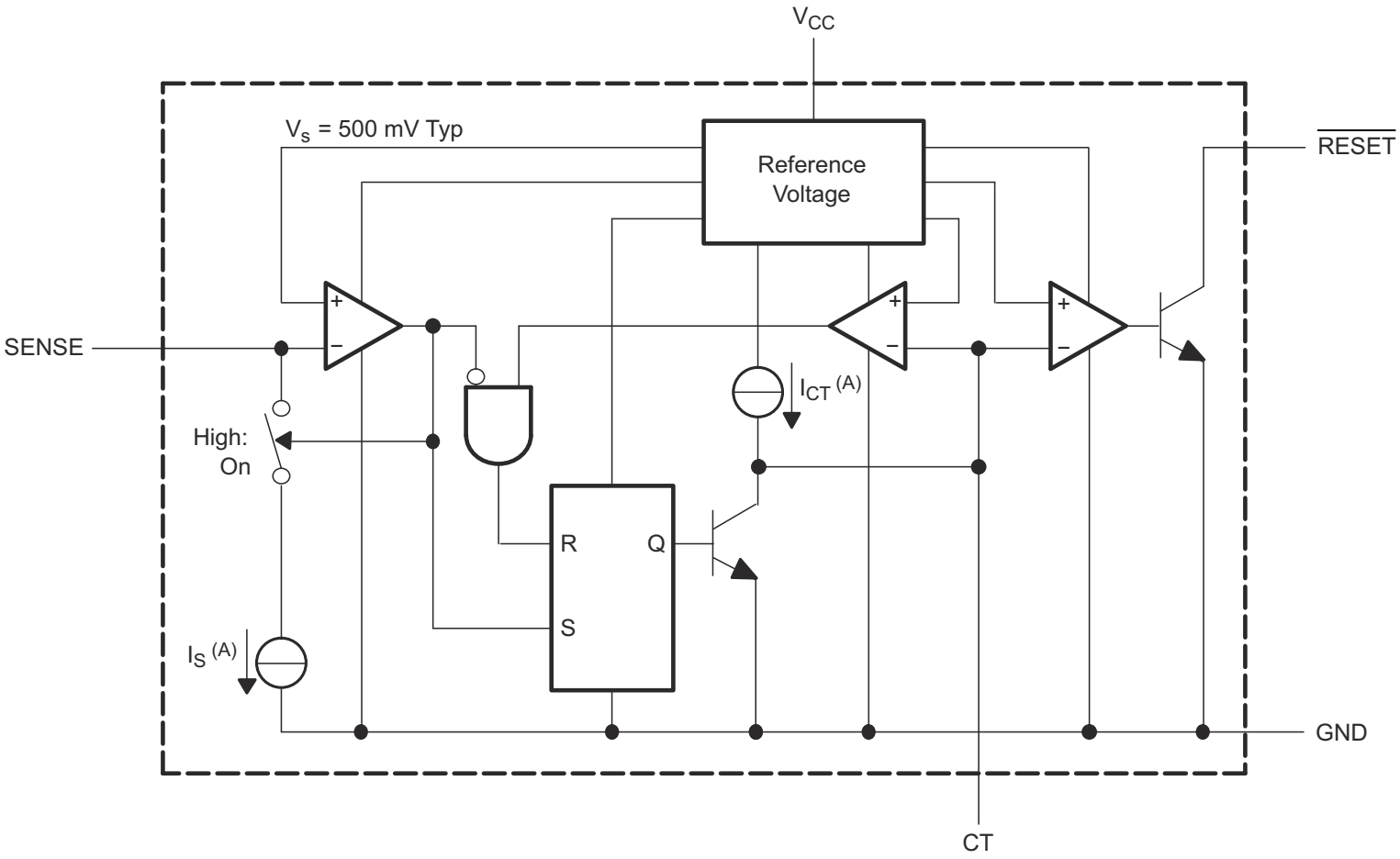
8 Detailed Description

8.1 Overview

The TL7700-SEP is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

The TL7700-SEP has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with AC line operation and portable battery operation.

8.2 Functional Block Diagram



I_{CT} = 15 µA (Typ), I_s = 2.5 µA (Typ)

8.3 Feature Description

8.3.1 Sense-Voltage Setting

The typical SENSE terminal input voltage (V_S) of the TL7700-SEP is 500 mV. By using two external resistors, the circuit designer can set the desired sense voltage to any value above 500 mV. Based on the schematic shown in 图 8-1, the desired sense voltage ($V_{S'}$) is calculated as:

$$V_{S'} = V_S \times \frac{(R1 + R2)}{R2} \quad (1)$$

where:

- V_S = 490 mV to 520 mV over temperature range

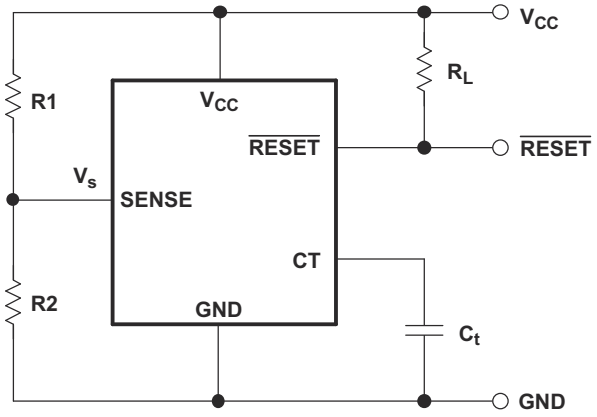


图 8-1. Setting the Sense Voltage

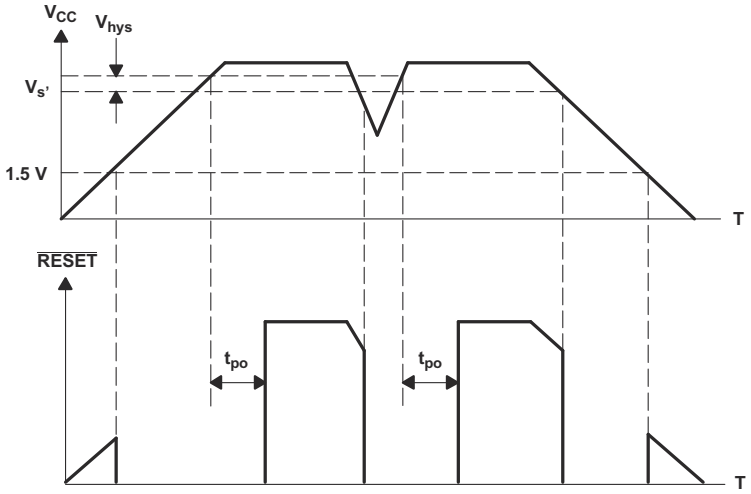
8.3.2 Sense-Voltage Hysteresis Setting

If the desired sense voltage ($V_{s'}$) does not have hysteresis in it and the voltage on the sensing line contains ripples, the resetting of TL7700-SEP will be unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in 图 8-2, the hysteresis (V_{hys}) is added and the value is determined as:

$$V_{hys} = I_s \times R1 \quad (2)$$

where

- I_s = 1 μA to 3.5 μA over temperature range



The desired sense voltage ($V_{s'}$) is different from the SENSE input voltage (V_s). V_s is typically 500 mV for triggering.

图 8-2. V_{CC}-RESET Response

8.3.3 Output Pulse-Duration Setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700-SEP sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{\text{RESET}}$ changes from a low to a high level. The output pulse duration is the time between the point when the SENSE-pin voltage exceeds the threshold level and the point when the $\overline{\text{RESET}}$ output changes from a low level to a high level. When the TL7700-SEP is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} in seconds is:

$$t_{po} = C_T \frac{\Delta V_{CT}}{I_{CT}} \quad (3)$$

where:

- C_T is the timing capacitor in farads
- ΔV_{CT} is the change in voltage at the CT pin (1.5-V reference voltage)
- I_{CT} is the timing capacitor charge current (typically 15 μA)

There is a limit on the device response speed. Even if C_t = 0, t_{po} is not 0, but approximately 5 μs to 10 μs. Therefore, when the TL7700-SEP is used as a comparator with hysteresis without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, and so forth) must be considered.

8.4 Device Functional Modes

图 8-2 shows how the $\overline{\text{RESET}}$ output pin responds to a change in the voltage at the SENSE pin. When the SENSE pin drops below 500 mV, the $\overline{\text{RESET}}$ pin is pulled low.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TL7700-SEP supply-voltage supervisor allows for any voltage greater than 500 mV to be monitored. This flexibility allows it to be used in many applications from FPGAs and microcontrollers to supply monitoring.

9.2 Typical Application

图 9-1 shows an application where the TL7700-SEP device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the sense voltage drops below 4.5 V, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.

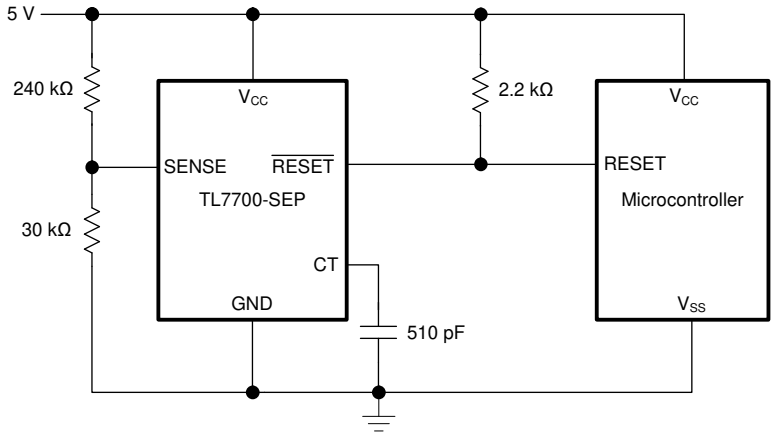


图 9-1. 5-V Supply Voltage Supervision

9.2.1 Design Requirements

- When the TL7700-SEP is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time.
- The RESET output is an open-collector output, so a pullup resistor is required.

9.2.2 Detailed Design Procedure

The SENSE terminal input voltage, V_s, for TL7700-SEP is typically 500 mV. By using two external resistors, any sense voltage over 500 mV can be sensed.

Resistor R1 should be selected first to set the desired hysteresis. 节 8.3.2 provides detailed information on how to set the hysteresis. For this application, a 240-kΩ resistor is selected.

$$V_{hys} = I_s \times R1 \tag{4}$$

$$V_{hys} = 2.5\ \mu A \times 240\ k\Omega = 0.6\ V \tag{5}$$

Resistor R2 should then be selected based on the R1 value and the desired sense voltage ($V_{s'}$). 节 8.3.1 describes how to set $V_{s'}$ and provides and equation. In this example, $V_{s'}$ is set to 4.5 V by using the value of R1 selected earlier and using a 30-kΩ resistor for R2.

$$V_{s'} = V_s \times \frac{(R1 + R2)}{R2} \tag{6}$$

$$V_{s'} = 0.5\ V \times \frac{(240\ k\Omega + 30\ k\Omega)}{30\ k\Omega} = 4.5\ V \quad (7)$$

Finally, the output pulse duration (t_{PO}) is set using the equation found in 节 8.3.3.

$$t_{po} = C_T \frac{\Delta V_{CT}}{I_{CT}} \quad (8)$$

$$t_{po} = 510\ pF \frac{1.5\ V}{15\ \mu A} = 51\ \mu s \quad (9)$$

9.2.3 Application Curve

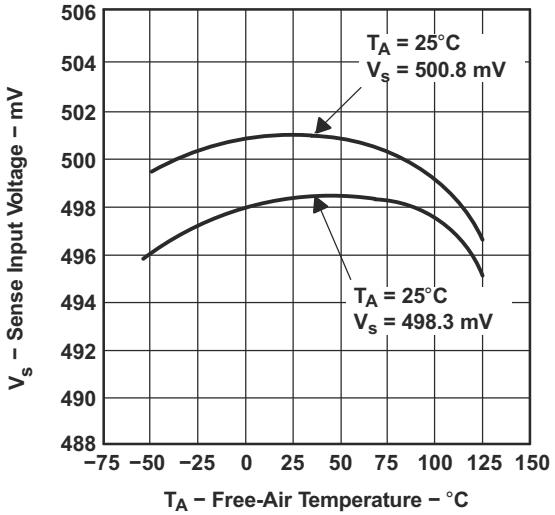


图 9-2. SENSE Input Voltage vs Temperature

10 Power Supply Recommendations

The TL7700-SEP device will operate within the supply range specified in 节 6.3. The device risks permanent damage over the voltage specified in 节 6.1.

11 Layout

11.1 Layout Guidelines

As the $\overline{\text{RESET}}$ pin is an open collector output, a pullup resistor is required to ensure the output is high when the output transistor is off. The SENSE resistors should be placed as close to the SENSE pin as possible to avoid introducing noise to the pin.

11.2 Layout Example

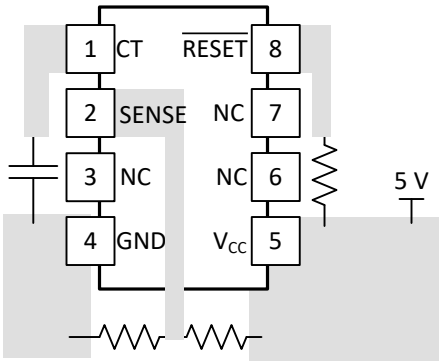


图 11-1. TL7700-SEP Layout

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL7700CMPWPSEP	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP
TL7700CMPWPSEP.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP
TL7700CMPWTPSEP	Active	Production	TSSOP (PW) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP
TL7700CMPWTPSEP.A	Active	Production	TSSOP (PW) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP
V62/19602-01XE	Active	Production	TSSOP (PW) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP
V62/19602-01XE-T	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

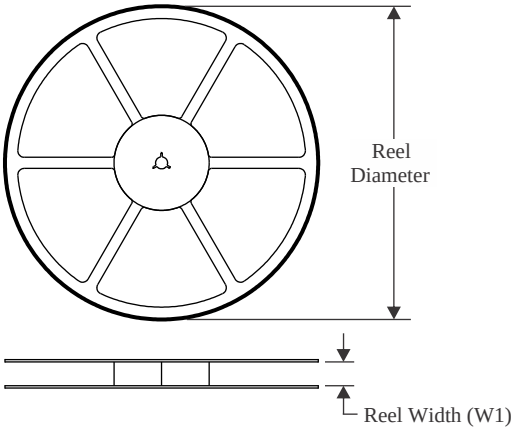
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

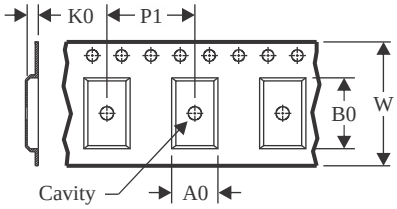
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

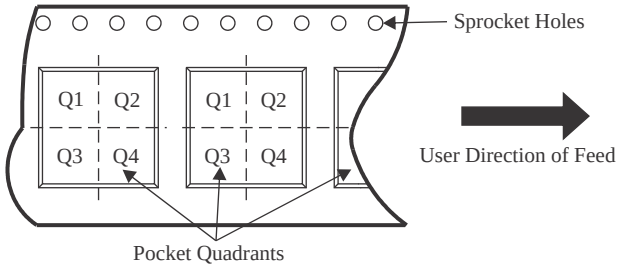


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

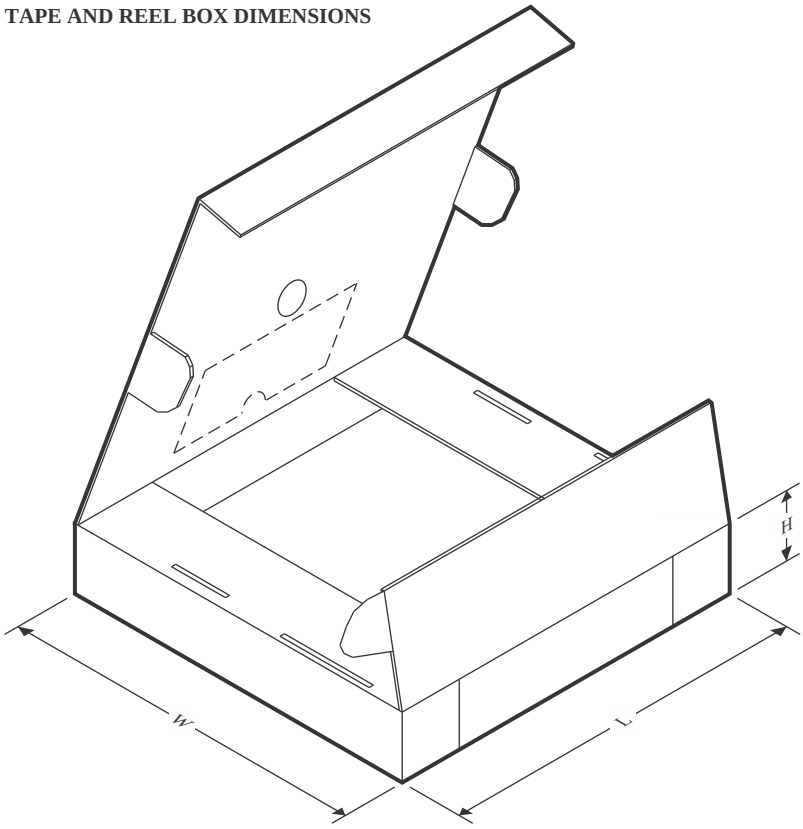
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7700CMPWTPSEP	TSSOP	PW	8	250	180.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

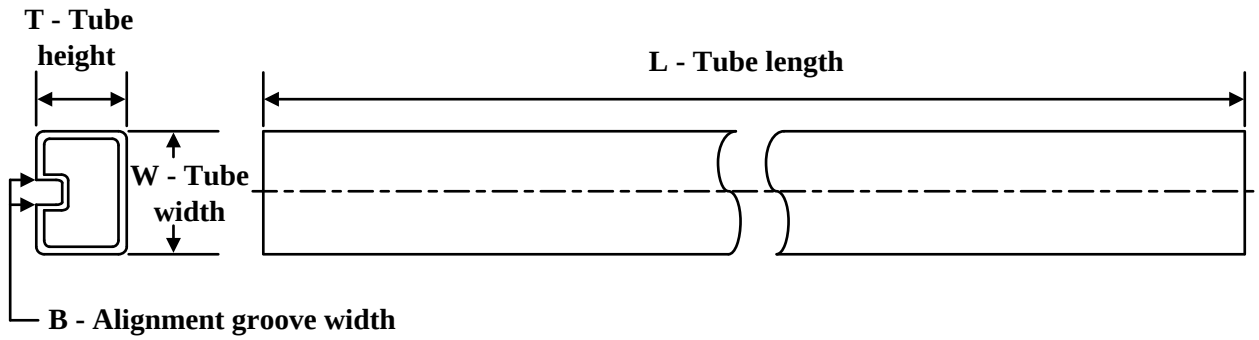
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7700CMPWTPSEP	TSSOP	PW	8	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

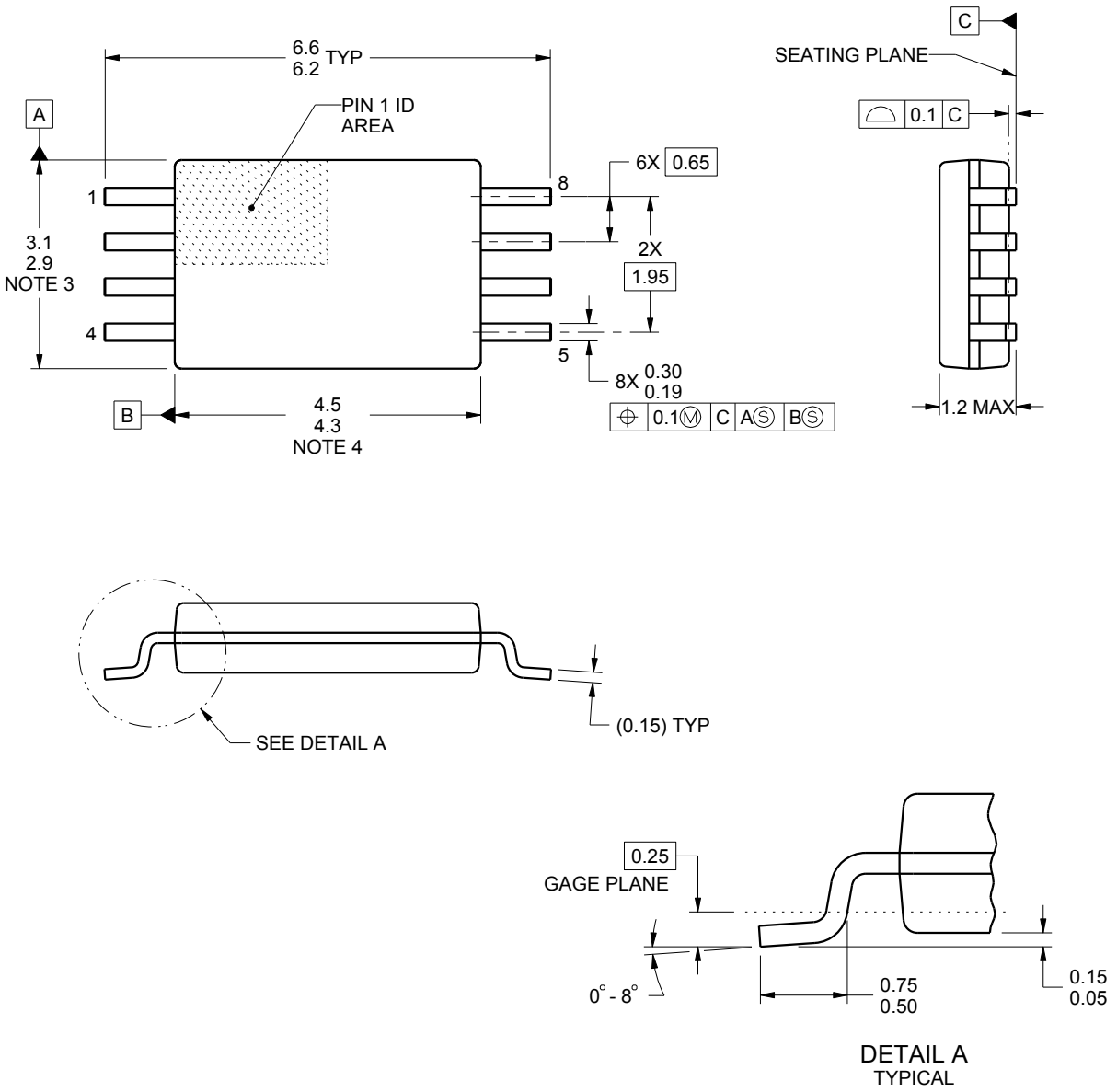
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7700CMPWPSEP	PW	TSSOP	8	150	530	10.2	3600	3.5
TL7700CMPWPSEP.A	PW	TSSOP	8	150	530	10.2	3600	3.5
V62/19602-01XE-T	PW	TSSOP	8	150	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0008A

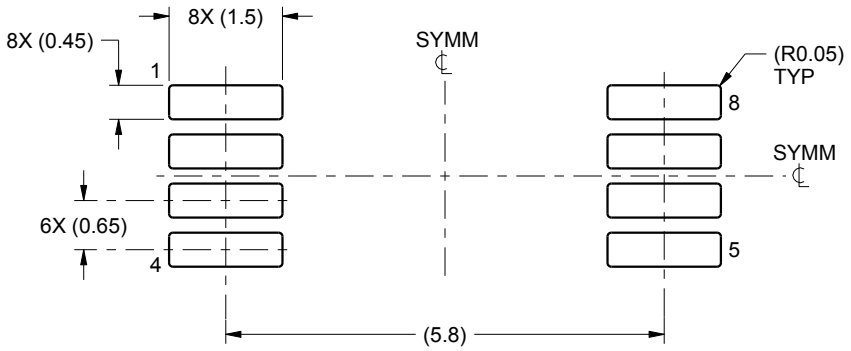
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

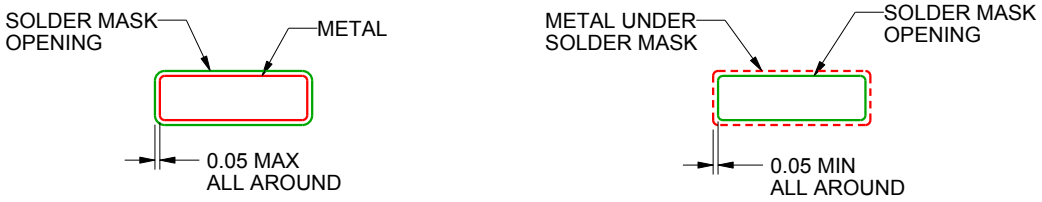


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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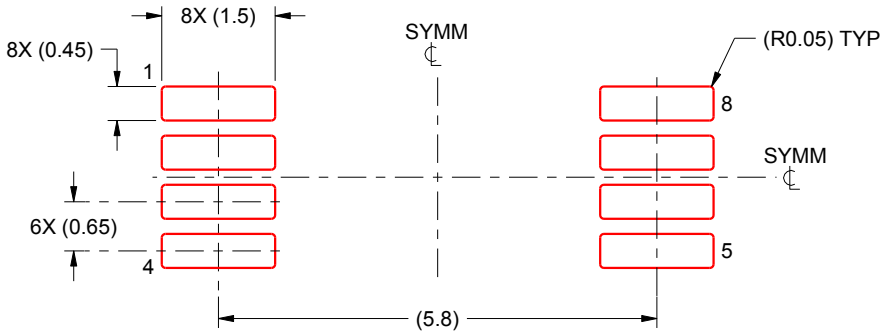
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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