THS452x Very Low Power, Negative Rail Input, Rail-To-Rail Output, Fully Differential Amplifier

1 Features

- Fully Differential Architecture
- Bandwidth: 145 MHz (A_V = 1 V/V)
- Slew Rate: 490 V/µs
- HD_2: –133 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)
- HD_3: –141 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)
- Input Voltage Noise: 4.6 nV/$\sqrt{Hz}$ (f = 100 kHz)
- THD+N: –112dBc (0.00025%) at 1 kHz (22-kHz BW, G = 1, 5 V_{PP})
- Open-Loop Gain: 119 dB (DC)
- NRI—Negative Rail Input
- RRO—Rail-to-Rail Output
- Output Common-Mode Control (with Low Offset)
- Power Supply:
  - Voltage: +2.5 V (±1.25 V) to +5.5 V (±2.75 V)
  - Current: 1.14 mA/ch
- Power-Down Capability: 20 µA (typical)

2 Applications

- Low-Power SAR and ΔΣ ADC Drivers
- Low-Power Differential Drivers
- Low-Power Differential Signal Conditioning
- Low-Power, High-Performance Differential Audio Amplifiers

3 Description

The THS4521, THS4522, and THS4524 family of devices are very low-power, fully differential amplifiers with rail-to-rail output and an input common-mode range that includes the negative rail. These amplifiers are designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter, and provide exceptional performance in audio applications.

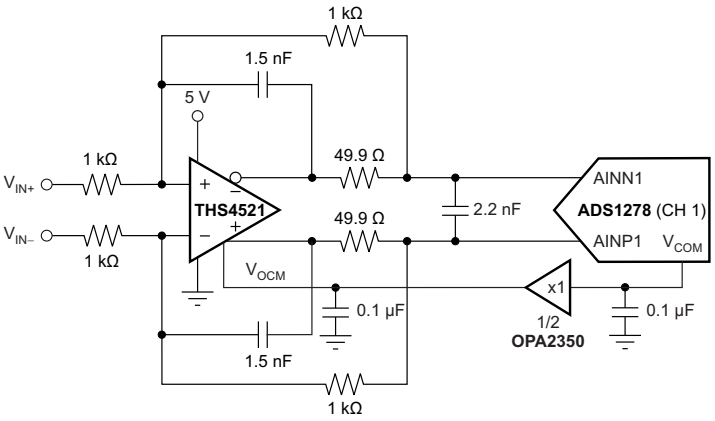
The family includes single FDA (THS4521), dual FDA (THS4522), and quad FDA (THS4524) versions.

Device Information(1)

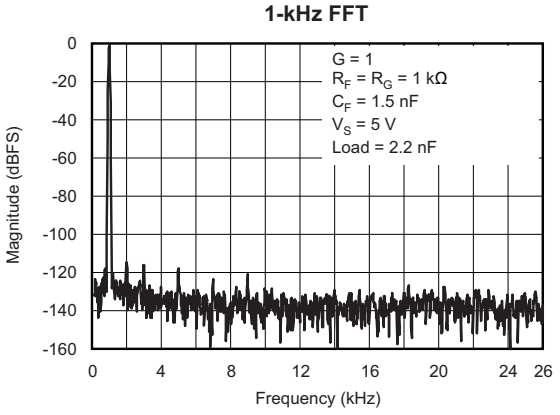
PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4521	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
THS4522	TSSOP (16)	5.00 mm × 4.40 mm
THS4524	TSSOP (38)	9.70 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

THS4521 and ADS1278 Combined Performance



1-kHz FFT



Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
1 k	–0.50	109.1	–107.9	105.5	113.7

For more information on this circuit, view SBAU197.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (December 2014) to Revision H — **Page**

- Changed capacitor units in front page diagram from mF to µF (typo) ... 1
- Changed RF and RG unit in front page FFT plot from kW to kΩ (typo) ... 1
- Changed Absolute Maximum Ratings minimum storage temperature value from 65 to –65 (typo) ... 7
- Added *Community Resources* section ... 53

Changes from Revision F (September 2011) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (December 2010) to Revision F — **Page**

- Changed Input Offset Current values in 3.3 V Electrical Characteristics ... 8
- Changed Input Offset Current Drift values in 3.3 V Electrical Characteristics ... 8
- Changed Input Offset Current values in 5 V Electrical Characteristics ... 11
- Changed Input Offset Current Drift values in 5 V Electrical Characteristics ... 11
- Changed R41 and R42 in Figure 79 ... 42

Changes from Revision D (August 2010) to Revision E — **Page**

- Changed test level indication for 5-V input offset voltage drift from B to C ... 10

5 Device Comparison Table

These fully differential amplifiers feature accurate output common-mode control that allows for dc-coupling when driving analog-to-digital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, these devices are ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single +2.5V to +5V and ground power supply.

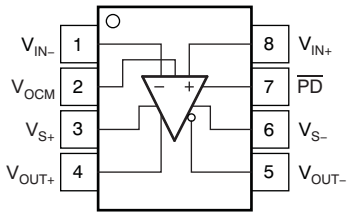
The THS4521, THS4522, and THS4524 family of fully differential amplifiers is characterized for operation over the full industrial temperature range from –40°C to +85°C. Table 1 shows a comparison of the THS4521 device to similar TI devices.

Table 1. THS4521 Device Comparison

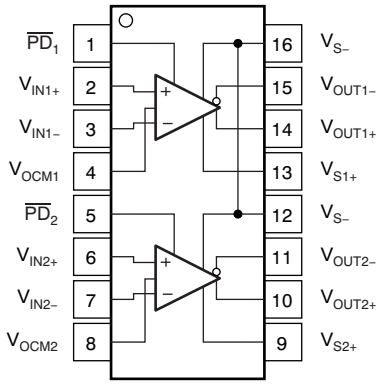
DEVICE	BW (MHz)	I_Q (mA)	THD (dBc) AT 100 kHz	V_N (nV/√Hz)	RAIL-TO-RAIL	DUAL PART NUMBERS
THS4531	36	0.25	–104	10.0	Neg In, Out	—
THS4521	145	0.95	–102	4.6	Neg In, Out	THS4522
THS4520	620	14.2	–107	2.0	Out	—
THS4541	850	10.1	–137	2.2	Neg In, Out	—

6 Pin Configuration and Functions

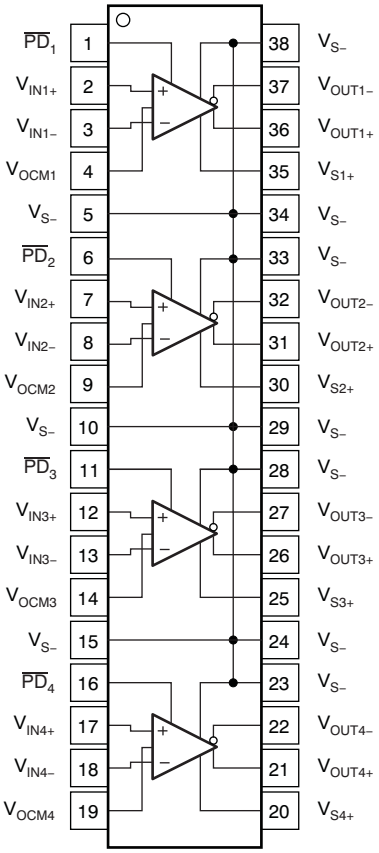
THS4521 D and DGK Package
8-Pin SOIC and VSSOP
Top View



THS4522 PW Package
16-Pin TSSOP
Top View



THS4524 DBT Package
38-Pin TSSOP
Top View



Pin Functions: THS4521

PIN		DESCRIPTION
NAME	NO.	
$V_{IN–}$	1	Inverting amplifier input
V_{OCM}	2	Common-mode voltage input
V_{S+}	3	Amplifier positive power-supply input
V_{OUT+}	4	Noninverting amplifier output
$V_{OUT–}$	5	Inverting amplifier output
$V_{S–}$	6	Amplifier negative power-supply input. Note that $V_{S–}$ is tied together on multi-channel devices.
$\overline{PD}$	7	Power down. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN+}	8	Noninverting amplifier input

Pin Functions: THS4522

PIN		DESCRIPTION
NAME	NO.	
$\overline{PD}_1$	1	Power down 1. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN1+}	2	Noninverting amplifier 1 input
V_{IN1-}	3	Inverting amplifier 1 input
V_{OCM1}	4	Common-mode voltage input 1
$\overline{PD}_2$	5	Power down 2. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN2+}	6	Noninverting amplifier 2 input
V_{IN2-}	7	Inverting amplifier 2 input
V_{OCM2}	8	Common-mode voltage input 2
V_{S+2}	9	Amplifier 2 positive power-supply input
V_{OUT2+}	10	Noninverting amplifier 2 output
V_{OUT2-}	11	Inverting amplifier 2 output
V_{S-}	12	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S+1}	13	Amplifier 1 positive power-supply input
V_{OUT1+}	14	Noninverting amplifier 1 output
V_{OUT1-}	15	Inverting amplifier 1 output
V_{S-}	16	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.

Pin Functions: THS4524

PIN		DESCRIPTION
NAME	NO.	
$\overline{PD}_1$	1	Power down 1. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN1+}	2	Noninverting amplifier 1 input
V_{IN1-}	3	Inverting amplifier 1 input
V_{OCM1}	4	Common-mode voltage input 1
V_{S-}	5	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
$\overline{PD}_2$	6	Power down 2. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN2+}	7	Noninverting amplifier 2 input
V_{IN2-}	8	Inverting amplifier 2 input
V_{OCM2}	9	Common-mode voltage input 2
V_{S-}	10	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
$\overline{PD}_3$	11	Power down 3. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN3+}	12	Noninverting amplifier 3 input
V_{IN3-}	13	Inverting amplifier 3 input
V_{OCM3}	14	Common-mode voltage input 3
V_{S-}	15	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
$\overline{PD}_4$	16	Power down 4. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
V_{IN4+}	17	Noninverting amplifier 4 input
V_{IN4-}	18	Inverting amplifier 4 input
V_{OCM4}	19	Common-mode voltage input 4
V_{S4+}	20	Amplifier 4 positive power-supply input
V_{OUT4+}	21	Noninverting amplifier 4 output
V_{OUT4-}	22	Inverting amplifier 4 output
V_{S-}	23	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S-}	24	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S3+}	25	Amplifier 3 positive power-supply input
V_{OUT3+}	26	Noninverting amplifier3 output
V_{OUT3-}	27	Inverting amplifier3 output
V_{S-}	28	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S-}	29	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S2+}	30	Amplifier 2 positive power-supply input
V_{OUT2+}	31	Noninverting amplifier 2 output
V_{OUT2-}	32	Inverting amplifier 2 output
V_{S-}	33	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S-}	34	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
V_{S1+}	35	Amplifier 1 positive power-supply input
V_{OUT1+}	36	Noninverting amplifier 1 output
V_{OUT1-}	37	Inverting amplifier 1 output
V_{S-}	38	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

	MIN	MAX	UNIT
Supply voltage, $V_{S–}$ to V_{S+}		5.5	V
Input/output voltage, V_I ($V_{IN±}$, $V_{OUT±}$, V_{OCM} pins)	($V_{S–}$) – 0.7	(V_{S+}) + 0.7	V
Differential input voltage, V_{ID}		1	V
Output current, I_O		100	mA
Input current, I_I ($V_{IN±}$, V_{OCM} pins)		10	mA
Continuous power dissipation	See *Thermal Information* table		
Maximum junction temperature, T_J		150	°C
Maximum junction temperature, T_J (continuous operation, long-term reliability)		125	°C
Operating free-air temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1300	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model (MM)	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{S+} single-supply voltage	2.7	5.0	5.4	V
T_A Ambient temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS4521		THS4522	THS4524	UNIT
		D	DGK	PW	DBT	
		8 PINS	8 PINS	16 PINS	38 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	127.8	193.8	124.2	106.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	81.8	84.1	62.8	60.9	
$R_{θJB}$	Junction-to-board thermal resistance	68.3	115.3	68.5	65.5	
$ψ_{JT}$	Junction-to-top characterization parameter	32.2	17.9	15.8	18.5	
$ψ_{JB}$	Junction-to-board characterization parameter	67.8	113.6	68	65.1	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = 3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1	C		135		MHz
	V_{OUT} = 100 mV_{PP}, G = 2	C		49		MHz
	V_{OUT} = 100 mV_{PP}, G = 5	C		18.6		MHz
	V_{OUT} = 100 mV_{PP}, G = 10	C		9.3		MHz
Gain bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10	C		93		MHz
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1	C		95		MHz
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 1	C		20		MHz
Rising slew rate (differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		420		V/µs
Falling slew rate (differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		460		V/µs
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		1.2%		
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		2.1%		
Rise time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		4		ns
Fall time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		3.5		ns
Settling time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω	C		13		ns
HARMONIC DISTORTION						
2nd harmonic	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1	C		–85		dBc
	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input	C		–133		dBc
3rd harmonic	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1	C		–90		dBc
	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input	C		–141		dBc
Second-order intermodulation distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope	C		–83		dBc
Third-order intermodulation distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope	C		–90		dBc
Input voltage noise	f > 10 kHz	C		4.6		nV/√Hz
Input current noise	f > 100 kHz	C		0.6		pA/√Hz
Overdrive recovery time	Overdrive = ±0.5 V	C		80		ns
Output balance error	V_{OUT} = 100 mV, f ≤ 2 MHz (differential input)	C		–57		dB
Closed-loop output impedance	f = 1 MHz (differential)	C		0.3		Ω
Channel-to-channel crosstalk (THS4522, THS4524)	f = 10 kHz, measured differentially	C		–125		dB
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		A	100	116		dB
Input-referred offset voltage	T_A = +25°C	A		±0.2	±2	mV
	T_A = –40°C to +85°C	B		±0.5	±3.5	mV
Input offset voltage drift(3)	T_A = –40°C to +85°C	C		±2		µV/°C
Input bias current(4)	T_A = +25°C	B		0.65	0.85	µA
	T_A = –40°C to +85°C	B		0.75	0.95	µA
Input bias current drift(3)	T_A = –40°C to +85°C	B		±1.75	±2	nA/°C
Input offset current	T_A = +25°C	B		±30	±180	nA
	T_A = –40°C to +85°C	B		±30	±215	nA
Input offset current drift(3)	T_A = –40°C to +85°C	B		±100	±600	pA/°C

(1) Test levels: **(A)** 100% tested at 25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Not directly measurable; calculated using noise gain of 101 as described in the Applications section, *Audio Performance*.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and V_{OCM} drift are average values calculated by taking data at the maximum-range ambient-temperature end points, computing the difference, and dividing by the temperature range. Maximum drift is set by the distribution of a large sampling of devices. Drift is not specified by a test or a quality assurance (QA) sample test.
(4) Input bias current is positive out of the device.

Electrical Characteristics: $V_{S+} - V_{S-} = 3.3$ V (continued)

At $V_{S+} = 3.3$ V, $V_{S-} = 0$ V, V_{OCM} = open, $V_{OUT} = 2\ V_{PP}$ (differential), $R_L = 1$ kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL(1)	MIN	TYP	MAX	UNIT
INPUT						
Common-mode input voltage low	T_A = +25°C	A		–0.2	–0.1	V
	T_A = –40°C to +85°C	B		–0.1	0	V
Common-mode input voltage high	T_A = +25°C	A	1.9	2		V
	T_A = –40°C to +85°C	B	1.8	1.9		V
Common-mode rejection ratio (CMRR)		A	80	100		dB
Input impedance		C		0.7 pF		kΩ‖pF
OUTPUT						
Output voltage low	T_A = +25°C	A		0.08	0.15	V
	T_A = –40°C to +85°C	B		0.09	0.2	V
Output voltage high	T_A = +25°C	A	3.0	3.1		V
	T_A = –40°C to +85°C	B	2.95	3.05		V
Output current drive (for linear operation)	R_L = 50 Ω	C		±35		mA
POWER SUPPLY						
Specified operating voltage		B	2.5	3.3	5.5	V
Quiescent operating current, per channel	T_A = +25°C	A	0.9	1.0	1.2	mA
	T_A = –40°C to +85°C	B	0.85	1.0	1.25	mA
Power-supply rejection ratio (±PSRR)		A	80	100		dB
POWER DOWN						
Enable voltage threshold	Assured *on* above 2.1 V	A		1.6	2.1	V
Disable voltage threshold	Assured *off* below 0.7 V	A	0.7	1.6		V
Disable pin bias current		C		1		µA
Power-down quiescent current		C		10		µA
Turn-on time delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω	B		108		ns
Turn-off time delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω	B		88		ns
V_{OCM} VOLTAGE CONTROL						
Small-signal bandwidth		C		23		MHz
Slew rate		C		55		V/µs
Gain		A	0.98	0.99	1.02	V/V
Common-mode offset voltage from V_{OCM} input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 1.65 V ±0.5 V	B		±2.5	±4	mV
Input bias current	V_{OCM} = 1.65 V ±0.5 V	B		±5	±8	µA
V_{OCM} voltage range		A	1	0.8 to 2.5	2.3	V
Input impedance		C		72‖1.5		kΩ‖pF
Default output common-mode voltage offset from (V_{S+}– V_{S-}) / 2	Measured at V_{OUT} with V_{OCM} input open	A		±1.5	±5	mV

7.6 Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V

At $V_{S+} = 5$ V, $V_{S-} = 0$ V, V_{OCM} = open, $V_{OUT} = 2\ V_{PP}$ (differential), $R_F = 1$ kΩ, $R_L = 1$ kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth	$V_{OUT} = 100\ mV_{PP}$, G = 1	C		145		MHz
	$V_{OUT} = 100\ mV_{PP}$, G = 2	C		50		MHz
	$V_{OUT} = 100\ mV_{PP}$, G = 5	C		20		MHz
	$V_{OUT} = 100\ mV_{PP}$, G = 10	C		9.5		MHz
Gain bandwidth product	$V_{OUT} = 100\ mV_{PP}$, G = 10	C		95		MHz
Large-signal bandwidth	$V_{OUT} = 2\ V_{PP}$, G = 1	C		145		MHz
Bandwidth for 0.1-dB flatness	$V_{OUT} = 2\ V_{PP}$, G = 1	C		30		MHz
Rising slew rate (differential)	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		490		V/µs
Falling slew rate (differential)	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		600		V/µs
Overshoot	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		1%		
Undershoot	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		2.6%		
Rise time	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		3.4		ns
Fall time	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		3		ns
Settling time to 1%	V_{OUT} = 2-V Step, G = 1, $R_L = 200\ \Omega$	C		10		ns
HARMONIC DISTORTION						
2nd harmonic	f = 1 MHz, $V_{OUT} = 2\ V_{PP}$, G = 1	C		–85		dBc
	f = 1 kHz, $V_{OUT} = 1\ V_{RMS}$, G = 1(2), differential input	C		–133		dBc
3rd harmonic	f = 1 MHz, $V_{OUT} = 2\ V_{PP}$, G = 1	C		–91		dBc
	f = 1 kHz, $V_{OUT} = 1\ V_{RMS}$, G = 1(2), differential input	C		–141		dBc
Second-order intermodulation distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope	C		–86		dBc
Third-order intermodulation distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope	C		–93		dBc
Input voltage noise	f > 10 kHz	C		4.6		nV/√Hz
Input current noise	f > 100 kHz	C		0.6		pA/√Hz
SNR	$V_{OUT} = 5\ V_{PP}$, 20 Hz to 22 kHz BW, differential input	C		123		dBc
THD+N	f = 1 kHz , $V_{OUT} = 5\ V_{PP}$, 20 Hz to 22 kHz BW, differential input	C		112		dBc
Overdrive recovery time	Overdrive = ±0.5 V	C		75		ns
Output balance error	V_{OUT} = 100 mV, f < 2 MHz, V_{IN} differential	C		–57		dB
Closed-loop output impedance	f = 1 MHz (differential)	C		0.3		Ω
Channel-to-channel crosstalk (THS4522. THS4524)	f = 10 kHz, measured differentially	C		–125		dB
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		A	100	119		dB
Input-referred offset voltage	T_A = +25°C	A		±0.24	±2	mV
	T_A = –40°C to +85°C	B		±0.5	±3.5	mV
Input offset voltage drift(3)	T_A = –40°C to +85°C	C		±2		µV/°C
Input bias current(4)	T_A = +25°C	B		0.7	0.9	µA
	T_A = –40°C to +85°C	B		0.9	1.1	µA
Input bias current drift(3)	T_A = –40°C to +85°C	B		±1.8	±2.2	nA/°C

(1) Test levels: **(A)** 100% tested at 25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Not directly measurable; calculated using noise gain of 101 as described in the Applications section, *Audio Performance*.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and V_{OCM} drift are average values calculated by taking data at the maximum-range ambient-temperature end points, computing the difference, and dividing by the temperature range. Maximum drift is set by the distribution of a large sampling of devices. Drift is not specified by a test or a quality assurance (QA) sample test.
(4) Input bias current is positive out of the device.

Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

At $V_{S+} = 5$ V, $V_{S-} = 0$ V, V_{OCM} = open, $V_{OUT} = 2\ V_{PP}$ (differential), $R_F = 1$ kΩ, $R_L = 1$ kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Input offset current	T_A = +25°C	B		±30	±180	nA
	T_A = –40°C to +85°C	B		±30	±215	nA
Input offset current drift(3)	T_A = –40°C to +85°C	B		±100	±600	pA/°C
INPUT						
Common-mode input voltage low	T_A = +25°C	A		–0.2	–0.1	V
	T_A = –40°C to +85°C	B		–0.1	0	V
Common-mode input voltage high	T_A = +25°C	A	3.6	3.7		V
	T_A = –40°C to +85°C	B	3.5	3.6		V
Common-mode rejection ratio (CMRR)		A	80	102		dB
Input impedance		C		100‖0.7		kΩ‖pF
OUTPUT						
Output voltage low	T_A = +25°C	A		0.10	0.15	V
	T_A = –40°C to +85°C	B		0.115	0.2	V
Output voltage high	T_A = +25°C	A	4.7	4.75		V
	T_A = –40°C to +85°C	B	4.65	4.7		V
Output current drive (for linear operation)	R_L = 50 Ω	C		±55		mA
POWER SUPPLY						
Specified operating voltage		B	2.5	5.0	5.5	V
Quiescent operating current, per channel	T_A = +25°C	A	0.95	1.14	1.25	mA
	T_A = –40°C to +85°C	B	0.9	1.15	1.3	mA
Power-supply rejection ratio (±PSRR)		A	80	100		dB
POWER DOWN						
Enable voltage threshold	Ensured *on* above 2.1 V	A		1.6	2.1	V
Disable voltage threshold	Ensured *off* below 0.7 V	A	0.7	1.6		V
Disable pin bias current		C		1		µA
Power-down quiescent current		C		20		µA
Turn-on time delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω	B		70		ns
Turn-off time delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω	B		60		ns
V_{OCM} VOLTAGE CONTROL						
Small-signal bandwidth		C		23		MHz
Slew rate		C		55		V/µs
Gain		A	0.98	0.99	1.02	V/V
Common-mode offset voltage from V_{OCM} input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 2.5 V ±1 V	B		±5	±9	mV
Input bias current	V_{OCM} = 2.5V ±1 V	B		±20	±25	µA
V_{OCM} voltage range		A	1	0.8 to 4.2	4	V
Input impedance		C		46‖1.5		kΩ‖pF
Default output common-mode voltage offset from $(V_{S+} – V_{S-}) / 2$	Measured at V_{OUT} with V_{OCM} input open	A		±1	±5	mV

7.7 Typical Characteristics

Table 2. Table of Graphs: $V_{S+} - V_{S-} = 3.3$ V

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Large- and Small-Signal Pulse Response	Figure 3
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10-kHz Output Spectrum on AP Analyzer	Figure 6
Harmonic Distortion vs Frequency	Figure 7
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 8
Harmonic Distortion vs Gain at 1 MHz	Figure 9
Harmonic Distortion vs Load at 1 MHz	Figure 10
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Output Balance Error vs Frequency	Figure 23
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Table 3. Table of Graphs: $V_{S+} - V_{S-} = 5$ V

	FIGURE
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Harmonic Distortion vs Output Voltage at 1 MHz	Figure 35
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Frequency Response vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 42
R_O vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 43
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Output Balance Error vs Frequency	Figure 50
V_{OCM} Small-Signal Frequency Response	Figure 51
V_{OCM} Large-Signal Frequency Response	Figure 52
V_{OCM} Input Impedance vs Frequency	Figure 53

7.8 Typical Characteristics: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

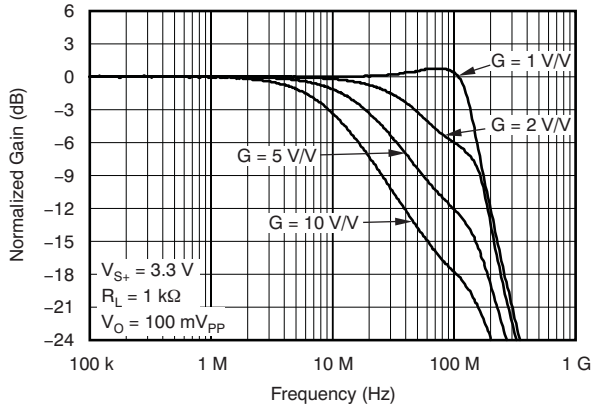


Figure 1. Small-Signal Frequency Response

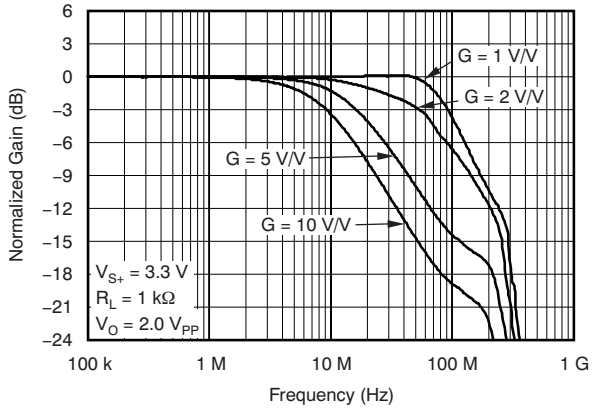


Figure 2. Large-Signal Frequency Response

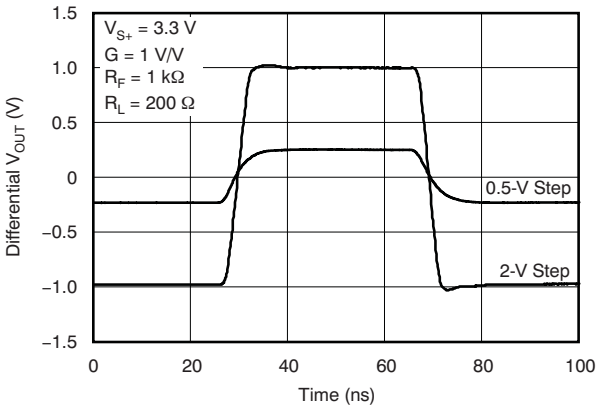


Figure 3. Large- and Small-Signal Pulse Response

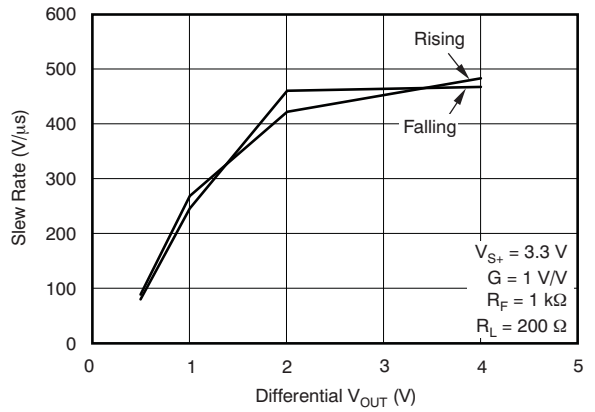


Figure 4. Slew Rate vs V_{OUT}

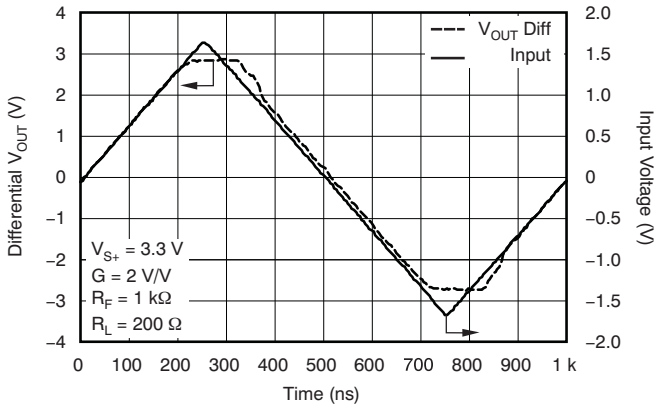


Figure 5. Overdrive Recovery

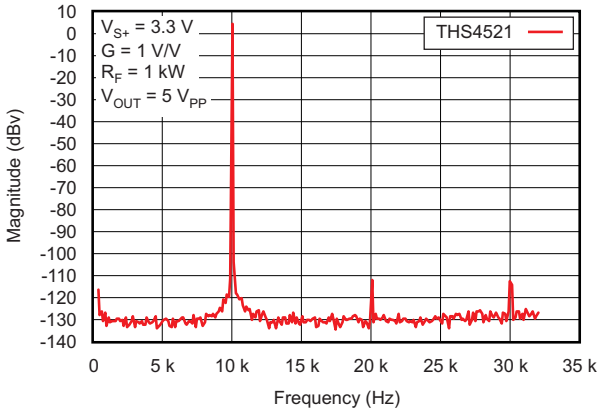


Figure 6. 10-kHz Output Spectrum On AP Analyzer

Typical Characteristics: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

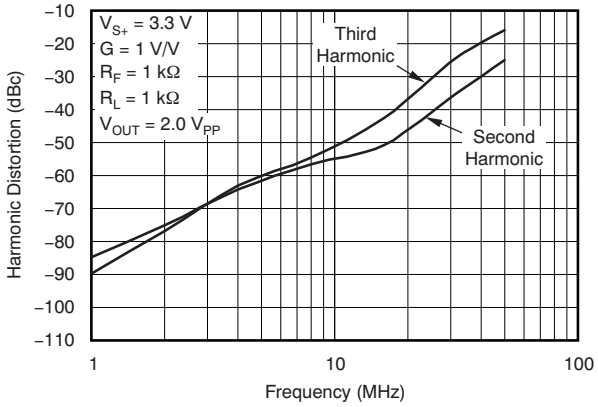


Figure 7. Harmonic Distortion vs Frequency

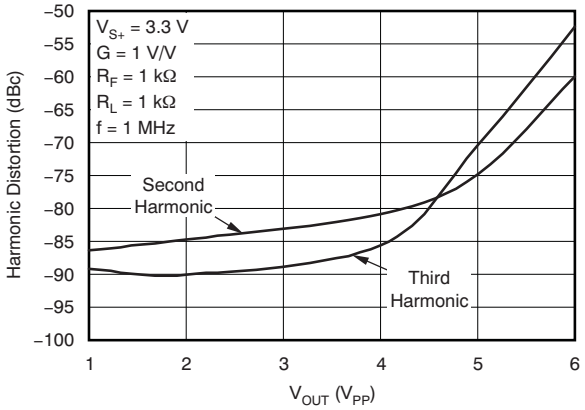


Figure 8. Harmonic Distortion vs V_{OUT} at 1 MHz

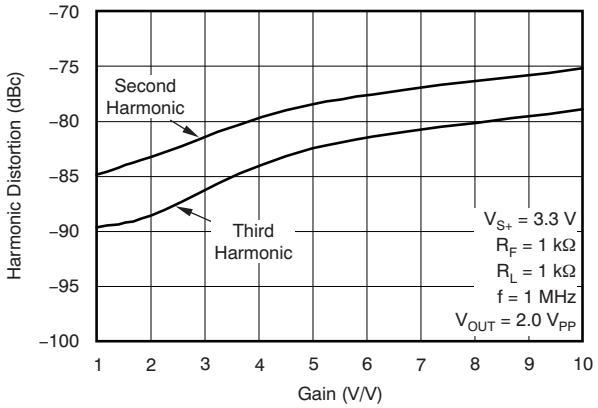


Figure 9. Harmonic Distortion vs Gain at 1 MHz

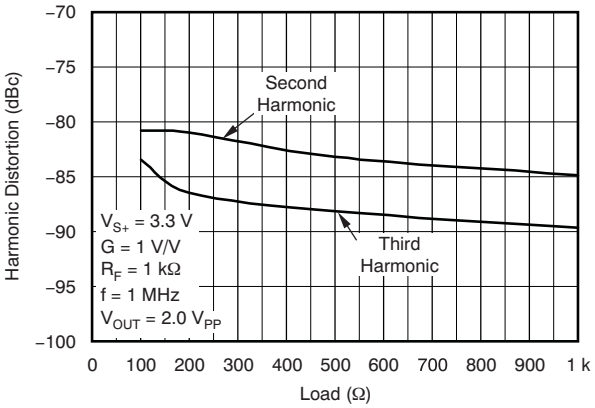


Figure 10. Harmonic Distortion vs Load at 1 MHz

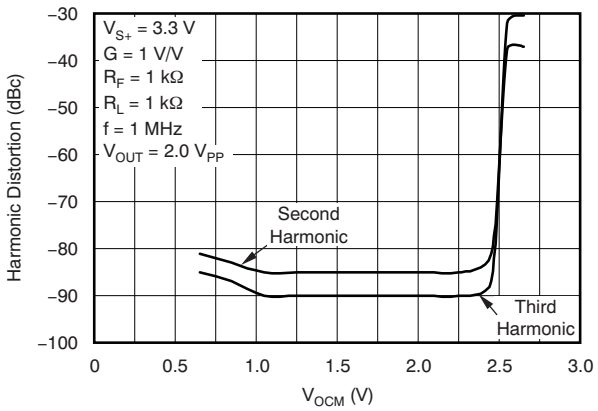


Figure 11. Harmonic Distortion vs V_{OCM} at 1 MHz

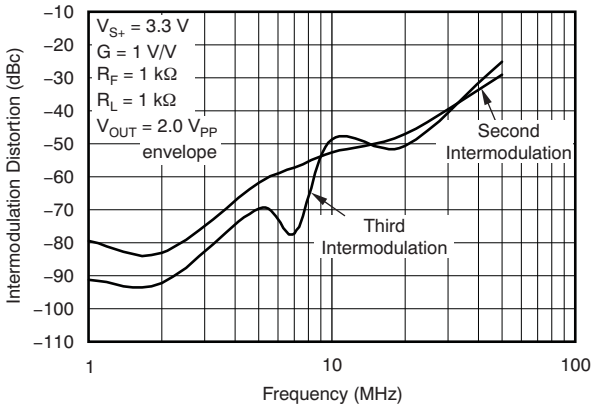


Figure 12. Two-Tone Intermodulation Distortion vs Frequency

Typical Characteristics: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

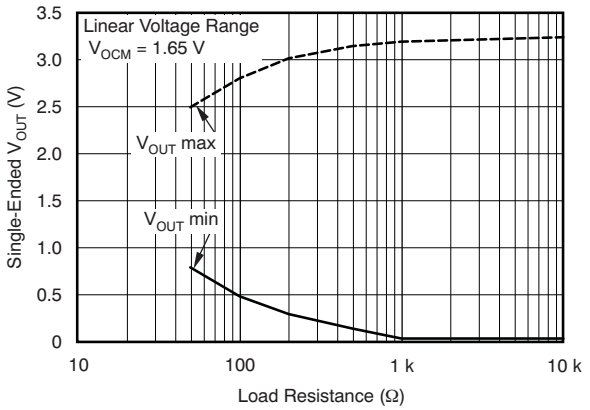


Figure 13. Single-Ended Output Voltage Swing vs Load Resistance

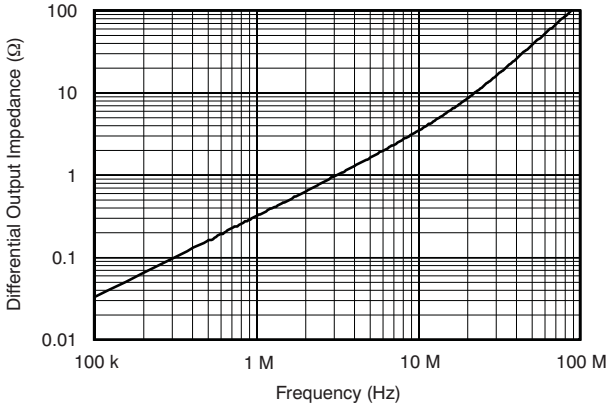


Figure 14. Main Amplifier Differential Output Impedance vs Frequency

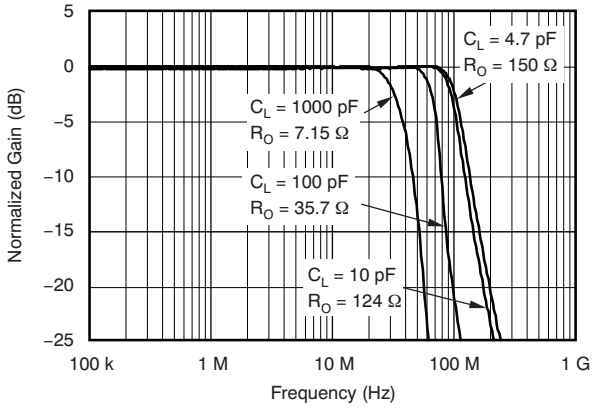


Figure 15. Frequency Response vs C_{LOAD} R_{LOAD} = 1 kΩ

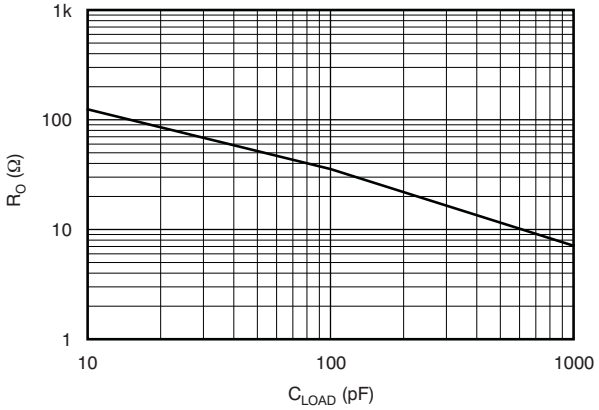


Figure 16. R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

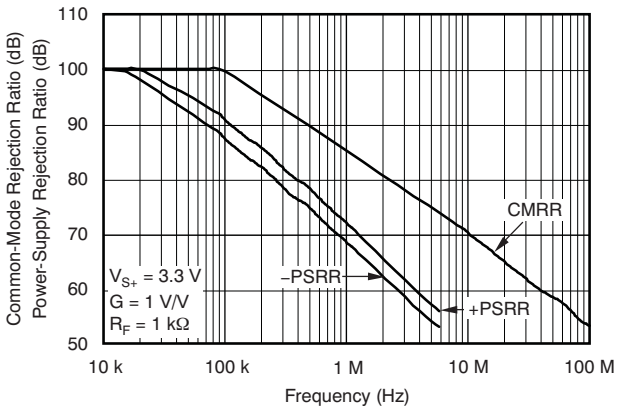


Figure 17. Rejection Ratio vs Frequency

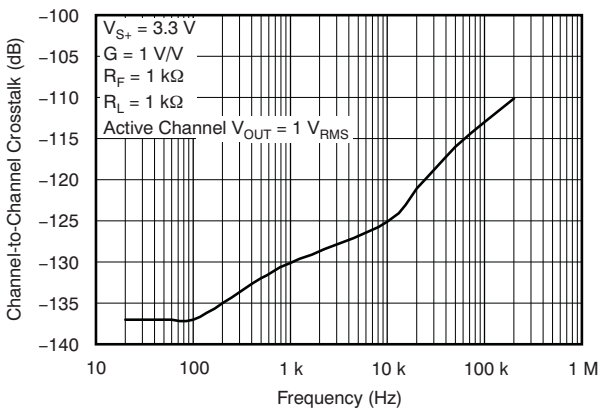


Figure 18. THS4522, THS4524 Crosstalk (Differential Measurement)

Typical Characteristics: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

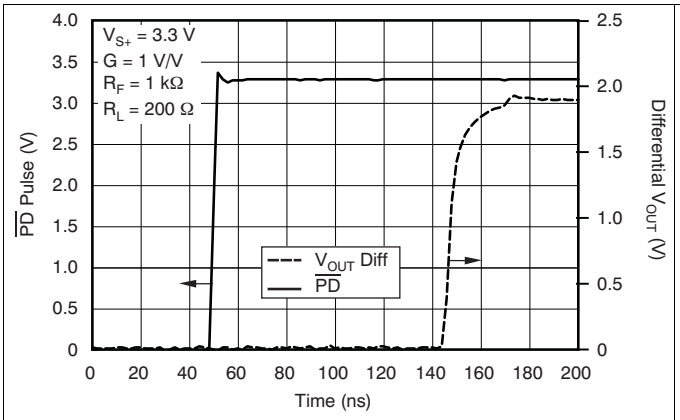


Figure 19. Turn-On Time

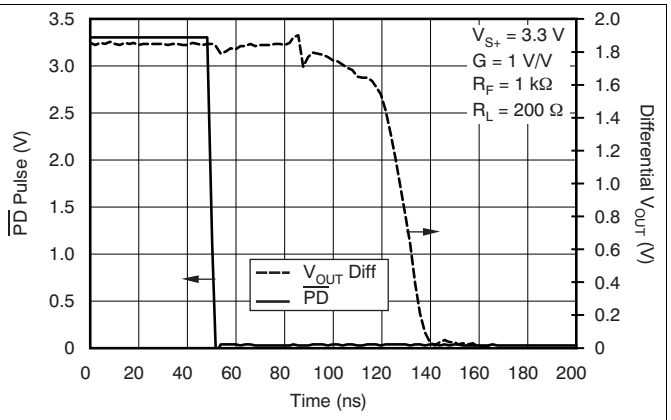


Figure 20. Turn-Off Time

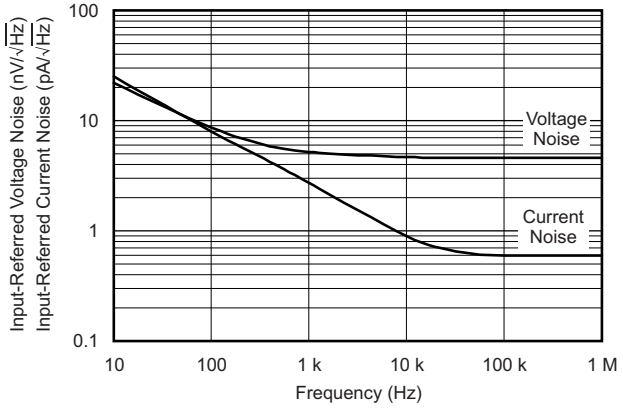


Figure 21. Input-Referred Voltage and Current Noise Spectral Density

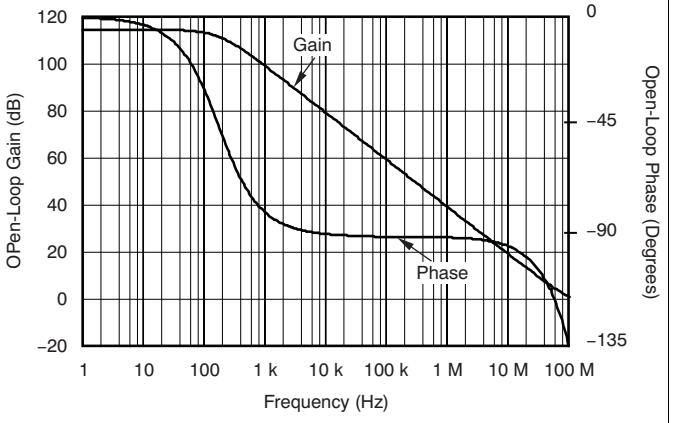


Figure 22. Main Amplifier Differential Open-Loop Gain and Phase

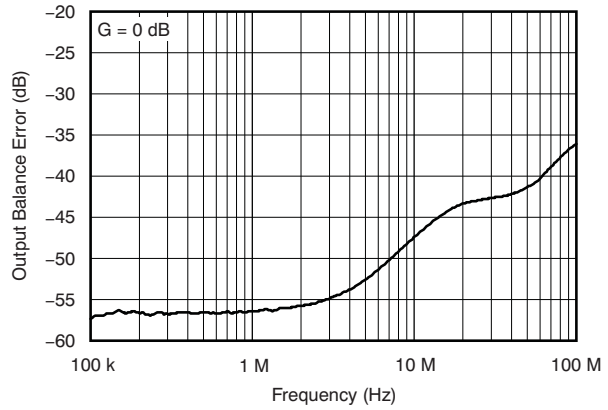


Figure 23. Output Balance Error vs Frequency

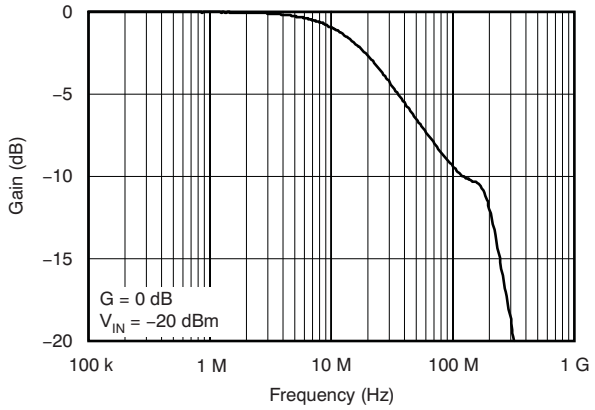


Figure 24. V_{OCM} Small-Signal Frequency Response

Typical Characteristics: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

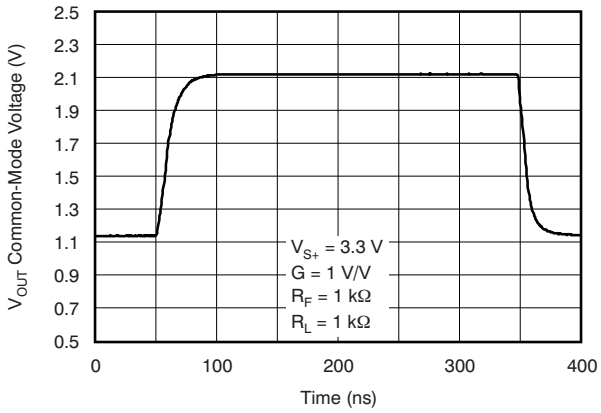


Figure 25. V_{OCM} Large-Signal Pulse Response

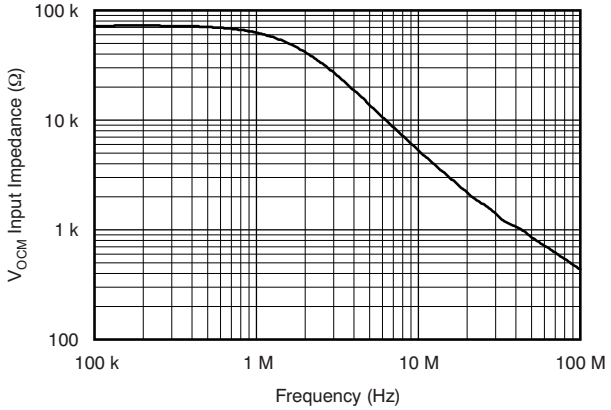


Figure 26. V_{OCM} Input Impedance vs Frequency

7.9 Typical Characteristics: 5 V

At V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

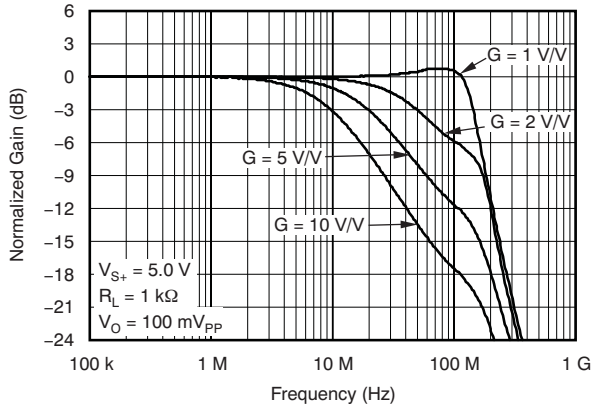


Figure 27. Small-Signal Frequency Response

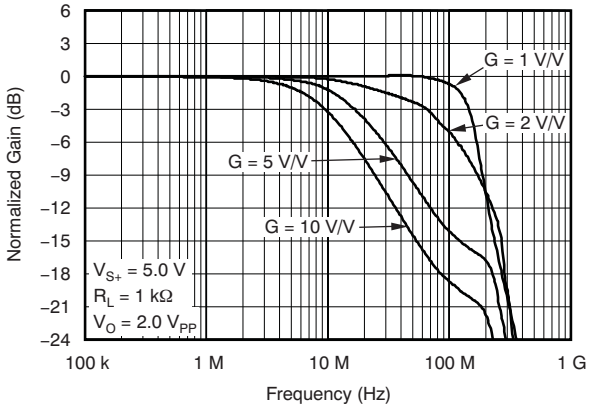


Figure 28. Large-Signal Frequency Response

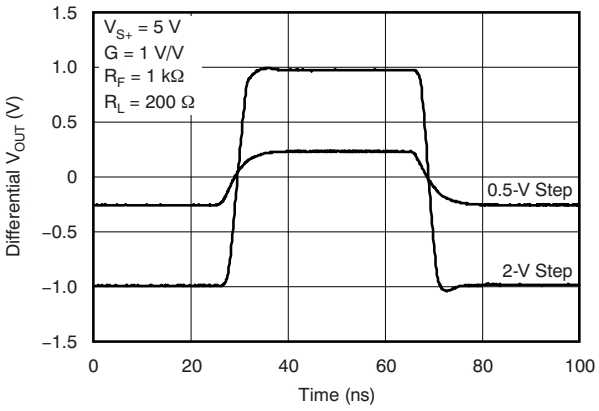


Figure 29. Large- and Small-Signal Pulse Response

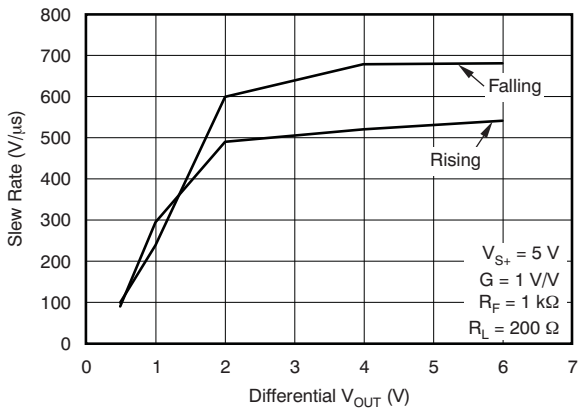


Figure 30. Slew Rate vs V_{OUT}

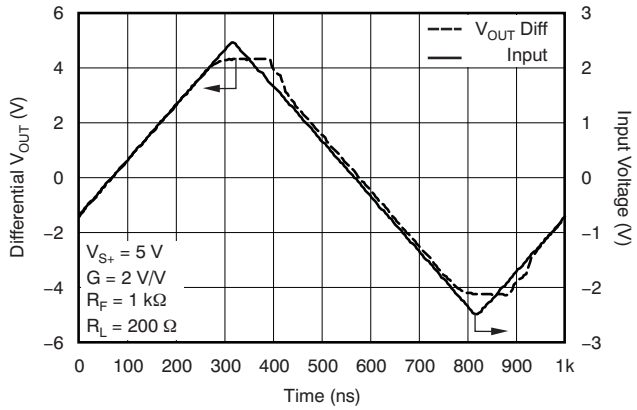


Figure 31. Overdrive Recovery

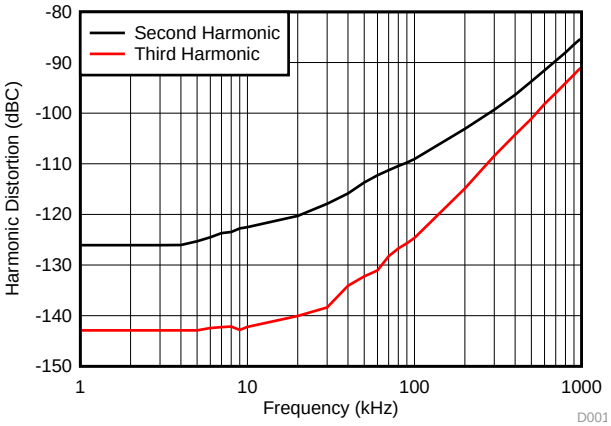


Figure 32. Harmonic Distortion vs Frequency Below 1 MHz

Typical Characteristics: 5 V (continued)

At V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

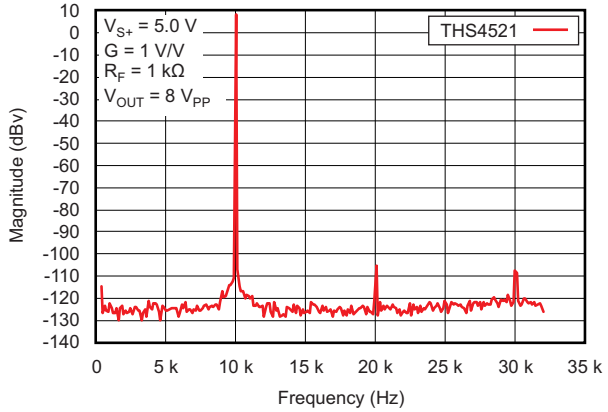


Figure 33. 10-kHz Output Spectrum On AP Analyzer at V_{OUT} = 8 V_{PP}

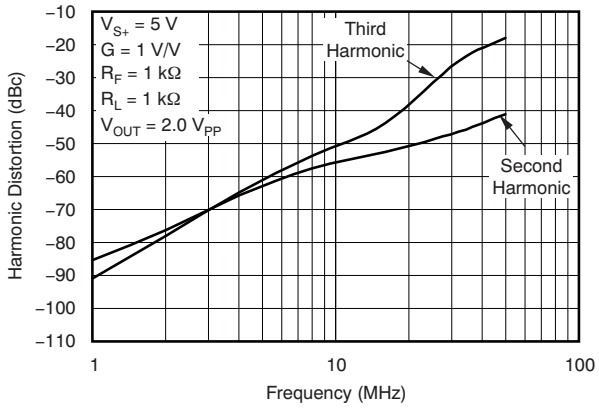


Figure 34. Harmonic Distortion vs Frequency

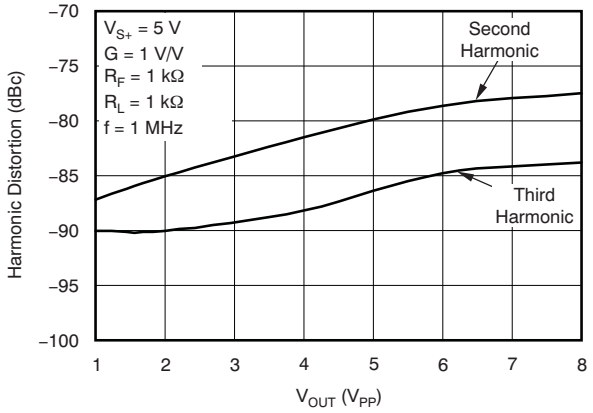


Figure 35. Harmonic Distortion vs V_{OUT} at 1 MHz

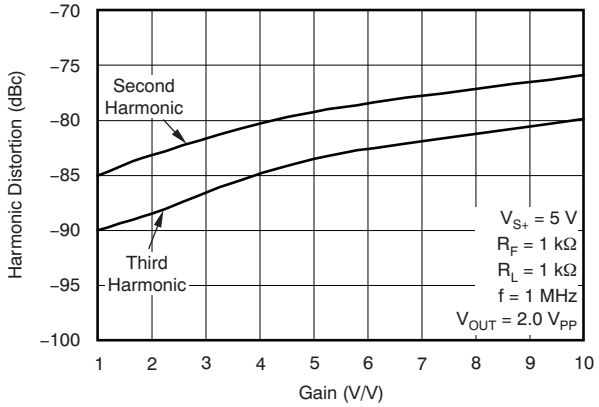


Figure 36. Harmonic Distortion vs Gain at 1 MHz

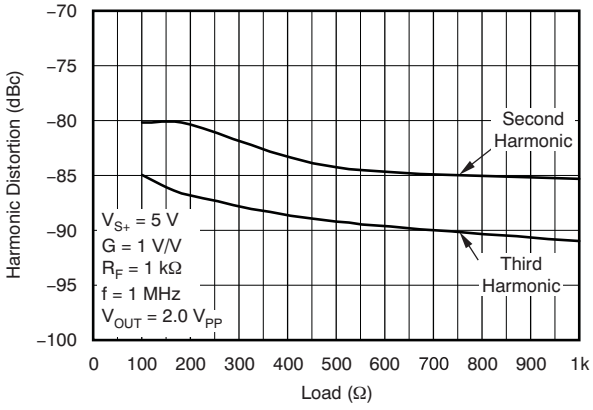


Figure 37. Harmonic Distortion vs Load at 1 MHz

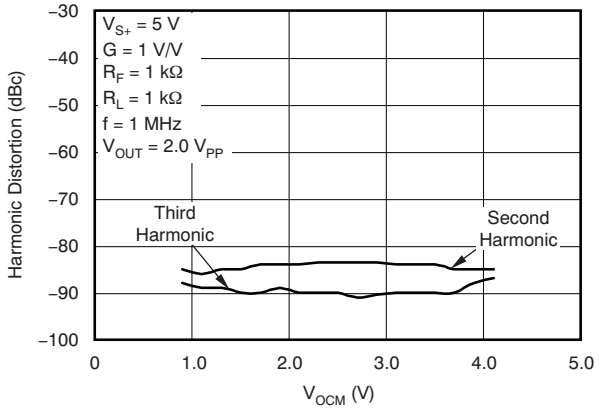


Figure 38. Harmonic Distortion vs V_{OCM} at 1 MHz

Typical Characteristics: 5 V (continued)

At V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

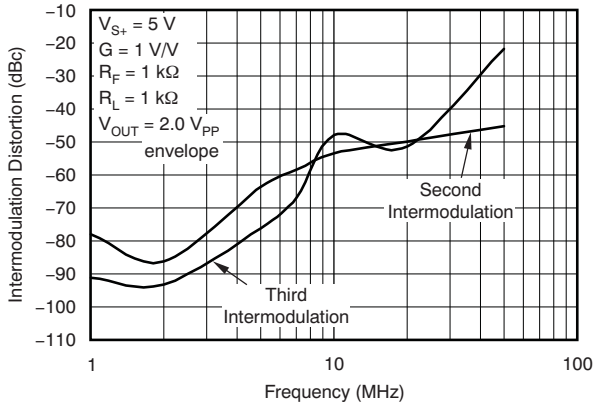


Figure 39. Two-Tone Intermodulation Distortion vs Frequency

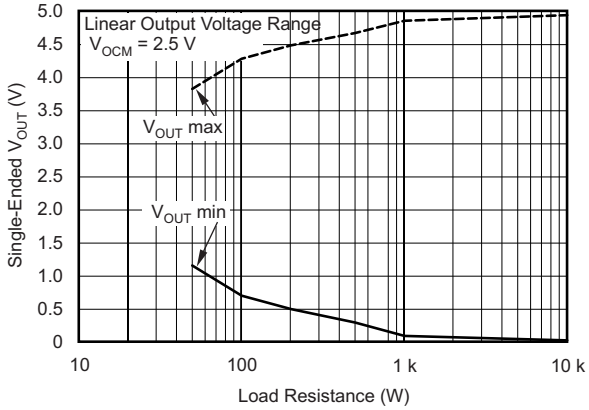


Figure 40. Single-Ended Output Voltage Swing vs Differential Load Resistance

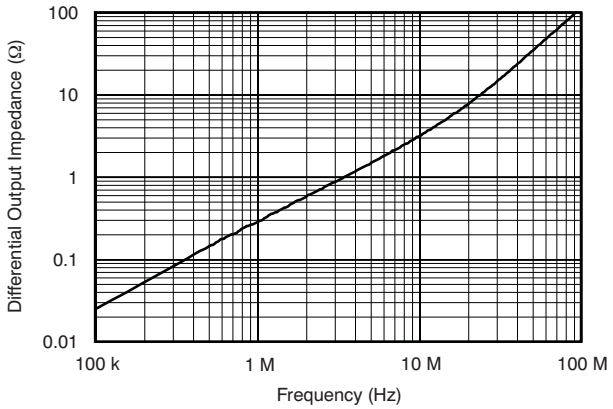


Figure 41. Main Amplifier Differential Output Impedance vs Frequency

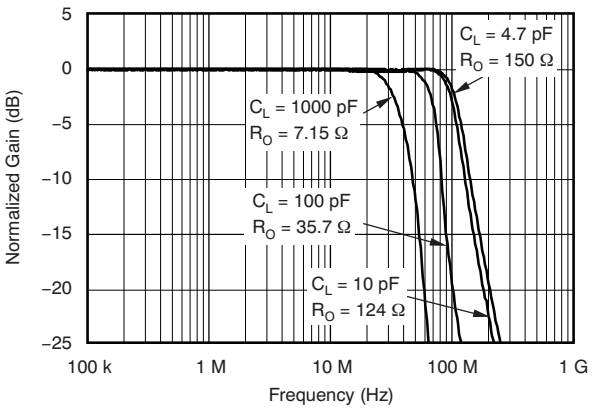


Figure 42. Frequency Response vs C_{LOAD} R_{LOAD} = 1 kΩ

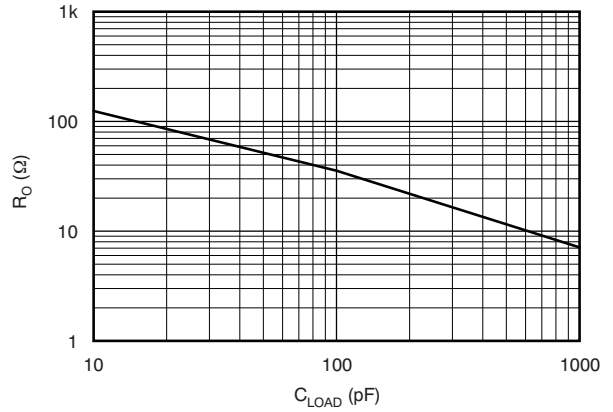


Figure 43. R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

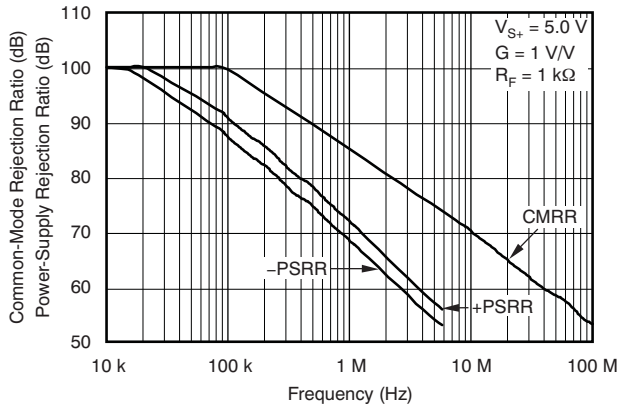


Figure 44. Rejection Ratio vs Frequency

Typical Characteristics: 5 V (continued)

At V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

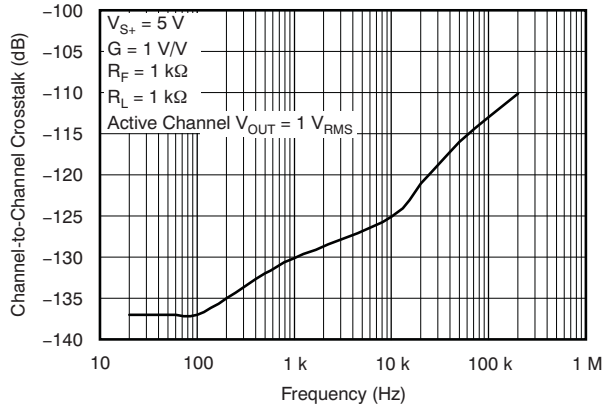


Figure 45. THS4522, THS4524 Crosstalk (Measured Differentially)

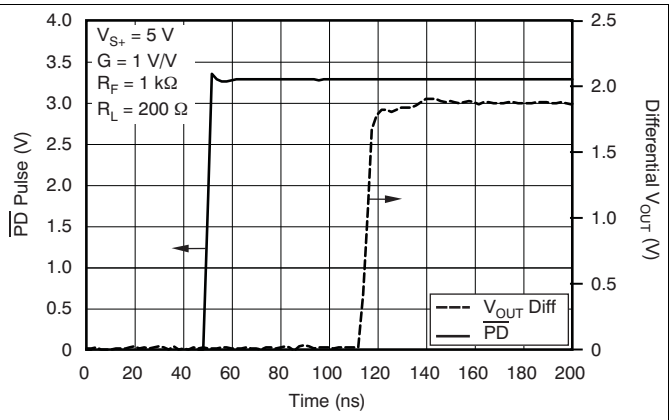


Figure 46. Turn-On Time

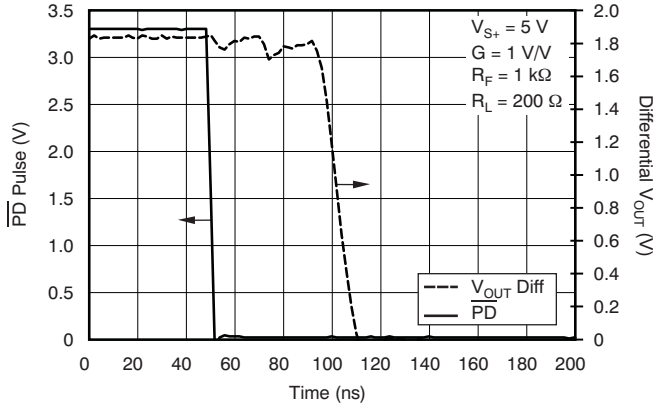


Figure 47. Turn-Off Time

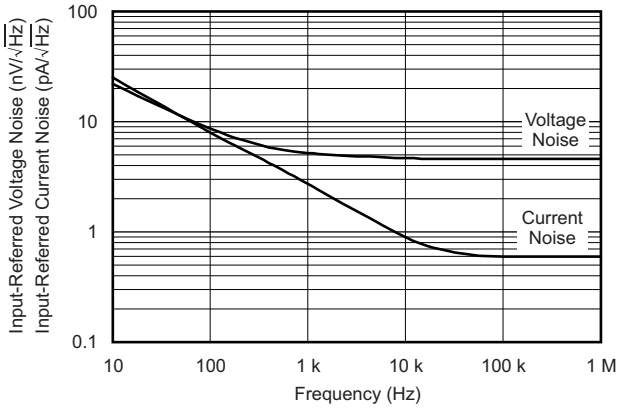


Figure 48. Input-Referred Voltage and Current Noise Spectral Density

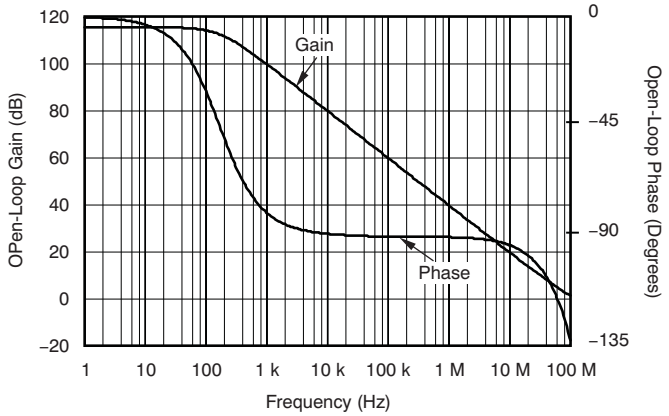


Figure 49. Main Amplifier Differential Open-Loop Gain and Phase

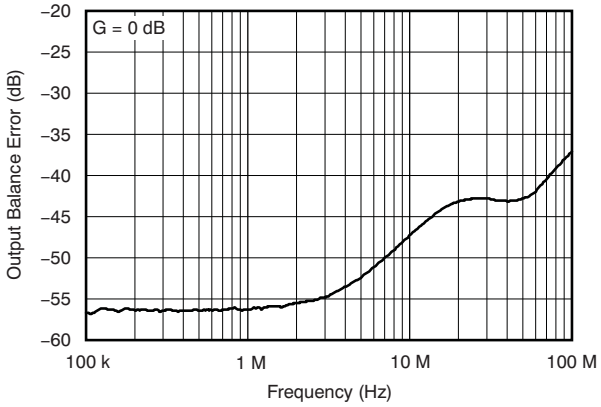


Figure 50. Output Balance Error vs Frequency

Typical Characteristics: 5 V (continued)

At V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

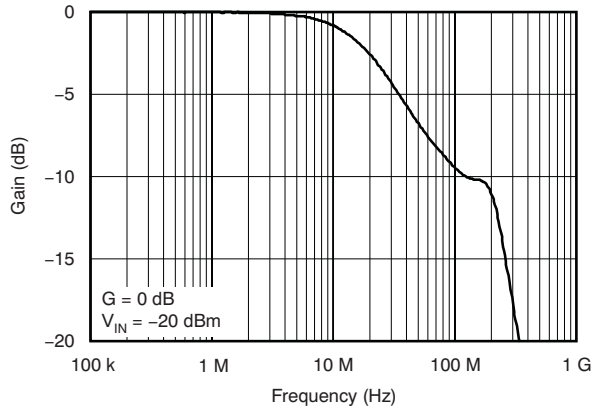


Figure 51. V_{OCM} Small-Signal Frequency Response

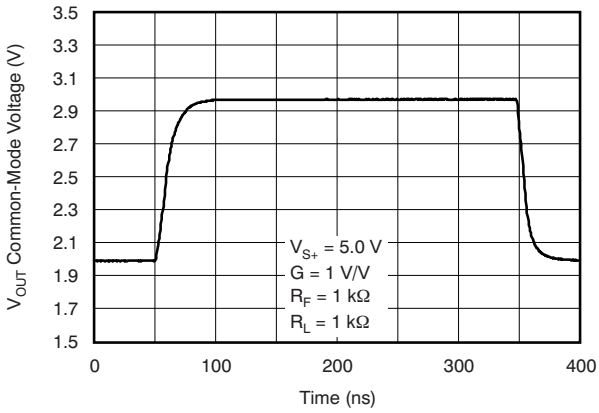


Figure 52. V_{OCM} Large-Signal Pulse Response

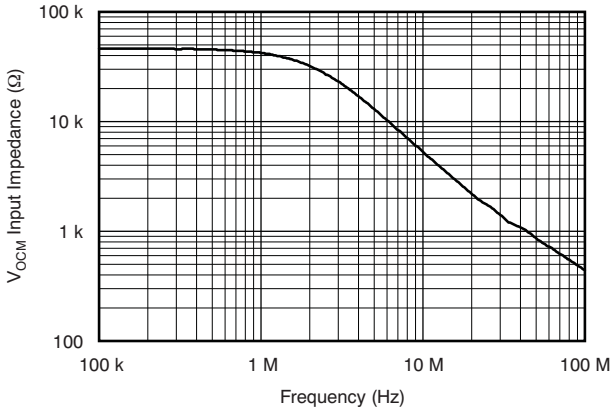


Figure 53. V_{OCM} Input Impedance vs Frequency

8 Detailed Description

8.1 Overview

The THS4521, THS4522, and THS4524 family is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the *Typical Applications* section for recommendations. Depending on the test conditions, component values change in accordance with Table 4 and Table 5, or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50-Ω sources. To balance the amplifier when ac-coupled, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across R_{IT}. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the *Typical Applications* section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The ***Atten*** column in Table 5 shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in Figure 55), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

Table 4. Gain Component Values for Single-Ended Input (see Figure 54)

Gain	R_F	R_G	R_{IT}
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	191 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

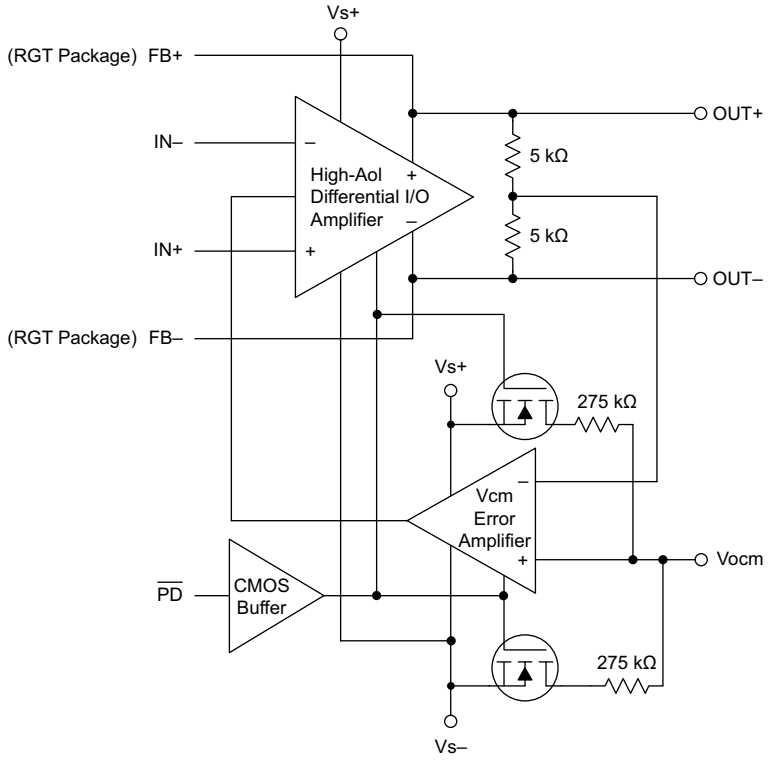
1. Gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 5. Load Component Values For 1:1 Differential To Single-Ended Output Transformer (See Figure 55)

R_L	R_O	R_{OT}	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

1. Total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Frequency Response

The circuit shown in Figure 54 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and the measurement device. The output impedance of the network analyzer is dc-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input.

The output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.

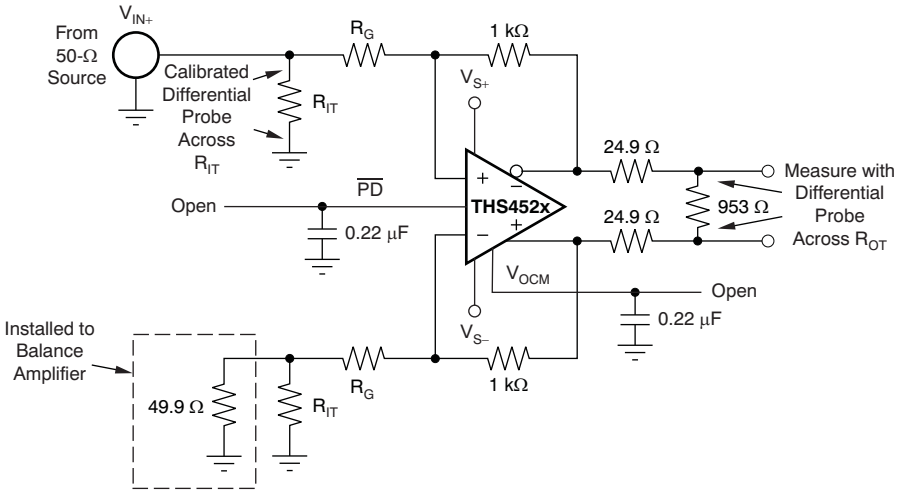


Figure 54. Frequency Response Test Circuit

Feature Description (continued)

8.3.2 Distortion

The circuit shown in Figure 55 is used to measure harmonic and intermodulation distortion of the amplifier.

A signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a notch filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1–1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

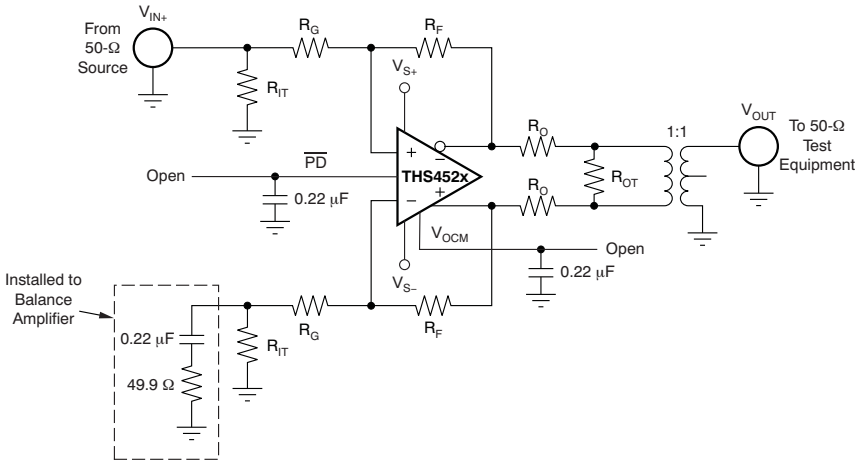


Figure 55. Distortion Test Circuit

8.3.3 Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 56 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and ampliifer turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50-Ω input impedance on the $\overline{PD}$ input by replacing the 0.22-µF capacitor with a 49.9-Ω resistor. For output impedance, the signal is injected at V_{OUT} with V_{IN} open; the drop across the 2x 49.9-Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

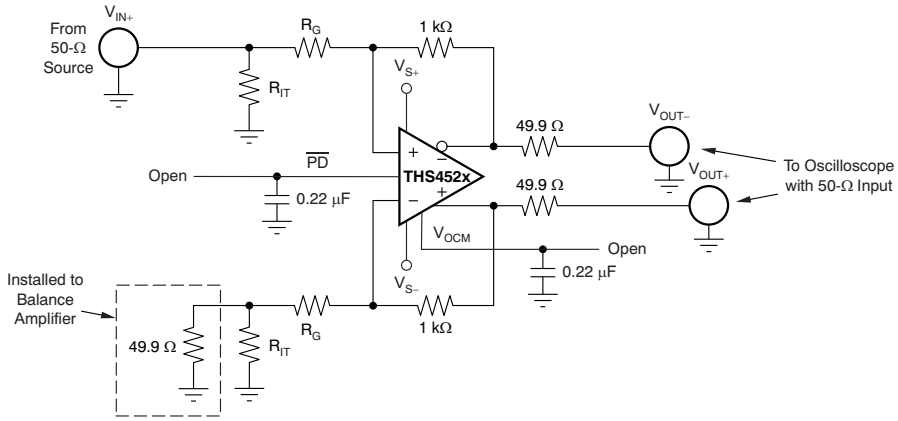


Figure 56. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Turn-Off Test Circuit

Feature Description (continued)

8.3.4 Common-Mode and Power-Supply Rejection

The circuit shown in Figure 57 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 58 is used to measure the PSRR of V_{S+} and V_{S-}. The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

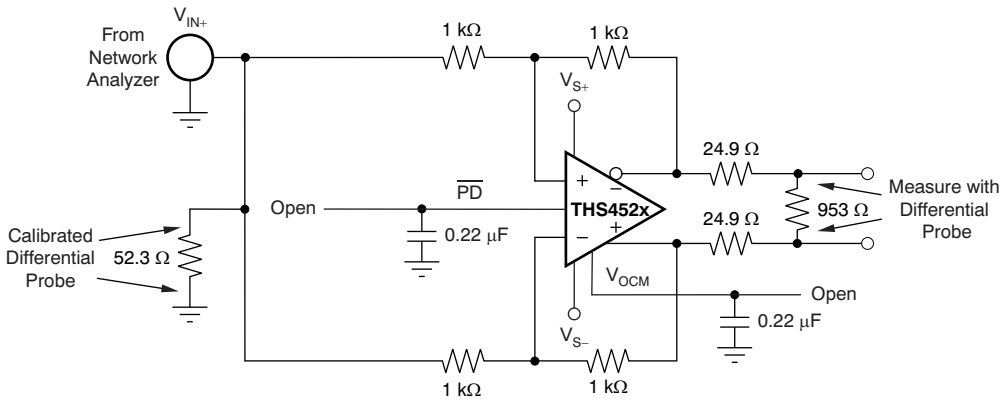


Figure 57. CMRR Test Circuit

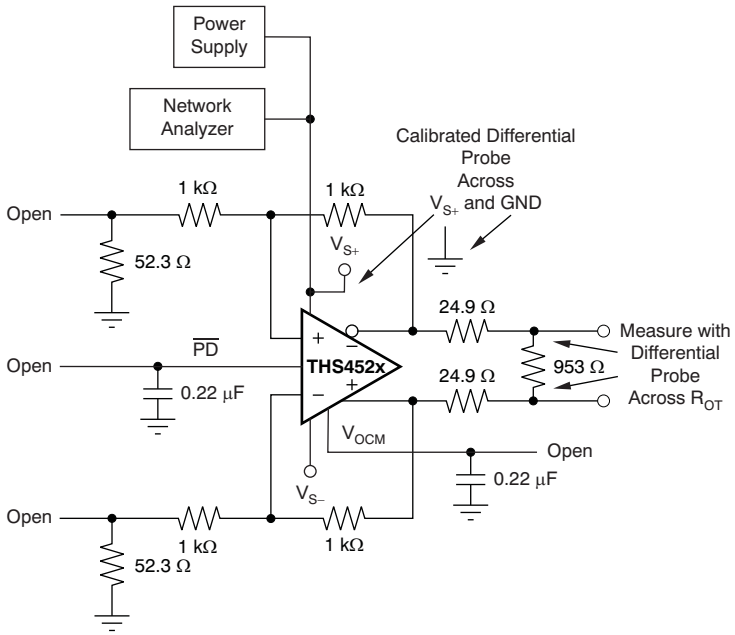


Figure 58. PSRR Test Circuit

Feature Description (continued)

8.3.5 V_{OCM} Input

The circuit illustrated in Figure 59 is used to measure the frequency response and skew rate of the V_{OCM} input. Frequency response is measured using a Tektronix high-impedance differential probe, with R_{CM} = 0 Ω at the common point of V_{OUT+} and $V_{OUT–}$, formed at the summing junction of the two matched 499-Ω resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the V_{OCM} input with R_{CM} = 10 kΩ and the drop across the 10-kΩ resistor is used to calculate the impedance seen looking into the amplifier V_{OCM} input.

The circuit shown in Figure 60 measures the transient response and slew rate of the V_{OCM} input. A 1-V step input is applied to the V_{OCM} input and the output is measured using a 50-Ω oscilloscope input referenced back to the amplifier output.

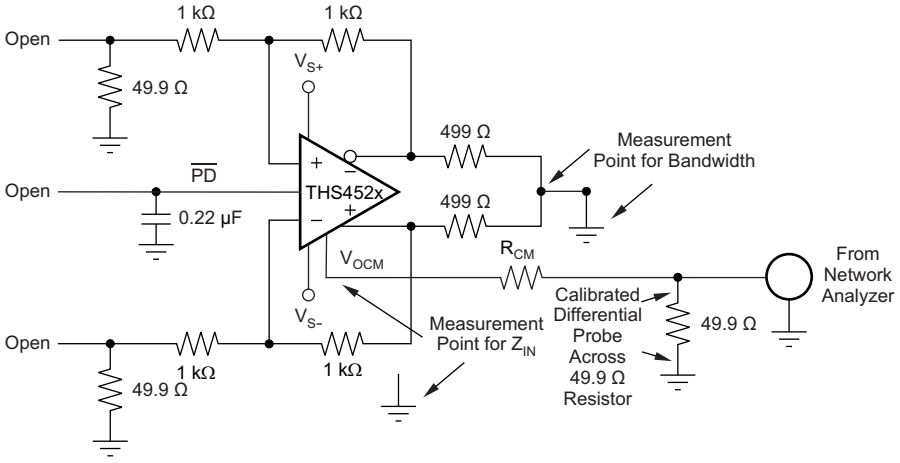


Figure 59. V_{OCM} Input Test Circuit

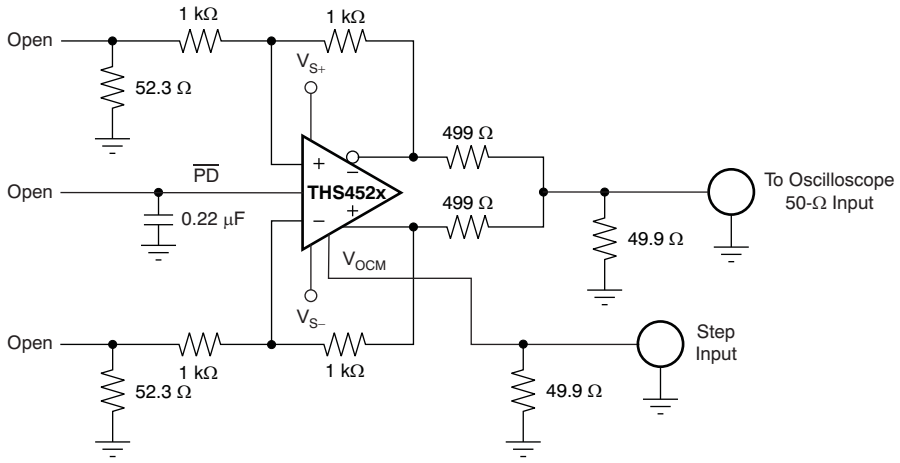


Figure 60. V_{OCM} Transient Response and Slew Rate Test Circuit

Feature Description (continued)

8.3.6 Typical Performance Variation With Supply Voltage

The THS4521, THS4522, and THS4524 family of devices provide excellent performance across the specified power-supply range of 2.5 V to 5.5 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, open-loop gain, bandwidth, and distortion. Table 6 shows the typical variation to be expected in these key performance parameters.

8.3.7 Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 61 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

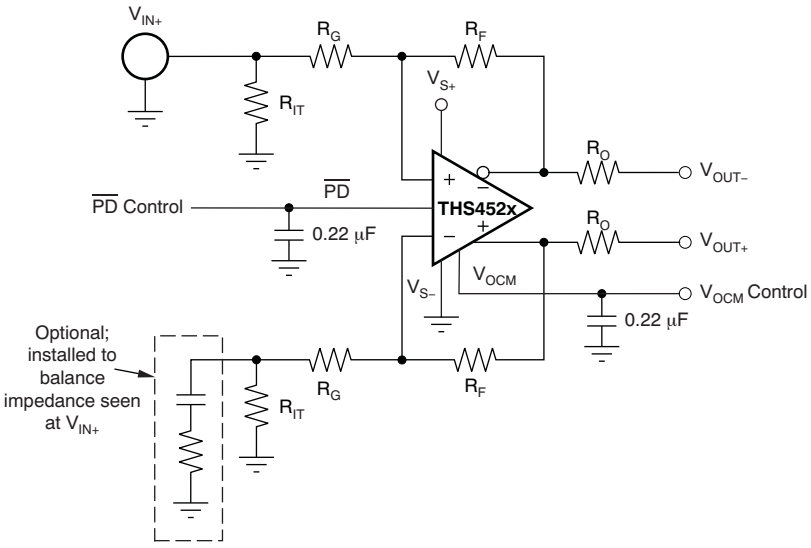


Figure 61. THS4521 DC-Coupled Single-Supply With Single-Ended Inputs

The input common-mode voltage range of the THS4521, THS4522, and THS4524 family is designed to include the negative supply voltage. in the circuit shown in Figure 61, the signal source is referenced to ground. V_{OCM} is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit, R_{IT} provides input termination, which is also referenced to ground.

Note that R_{IT} and optional matching components are added to the alternate input to balance the impedance at signal input.

Table 6. Typical Performance Variation Versus Power-Supply Voltage

PARAMETER		V_S = 5 V	V_S = 3.3 V	V_S = 2.5 V
–3-dB Small-signal bandwidth		145 MHz	135 MHz	125 MHz
Slew rate (2-V step)		490 V/µs	420 V/µs	210 V/µs
Harmonic distortion at 1 MHz, 2 V_{PP}, R_L = 1 kΩ	Second harmonic	–85 dBc	–85 dBc	–84 dBc
	Third harmonic	–91 dBc	–90 dBc	–88 dBc
Open-loop gain (dc)		119 dB	116 dB	115 dB
Linear output current drive		55 mA	35 mA	24 mA

8.3.8 Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521, THS4522, and THS4524 family as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance. Figure 62 shows the small-signal frequency response with 1-kΩ and 10-kΩ resistors for R_F, R_G, and R_L (impedance is assumed to typically increase for all three resistors in low-power applications).

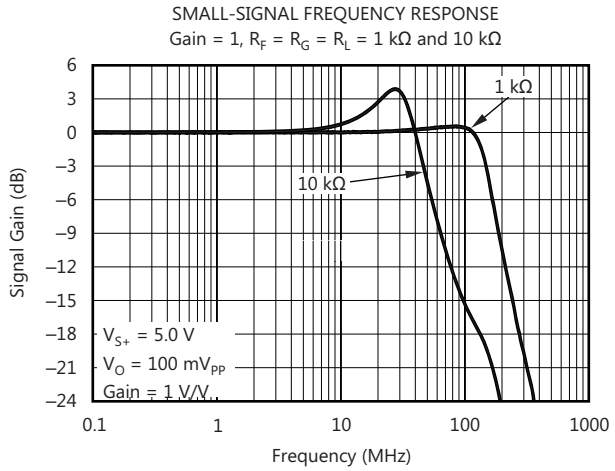


Figure 62. THS4521 Frequency Response With Various Gain Setting and Load Resistor Values

8.3.9 Frequency Response Variation due to Package Options

Users can see variations in the small-signal (V_{OUT} = 100 mV_{PP}) frequency response between the available package options for the THS4521, THS4522, and THS4524 family as a result of parasitic elements associated with each package and board layout changes. Figure 63 shows the variance measured in the lab; this variance is to be expected even when using a good layout.

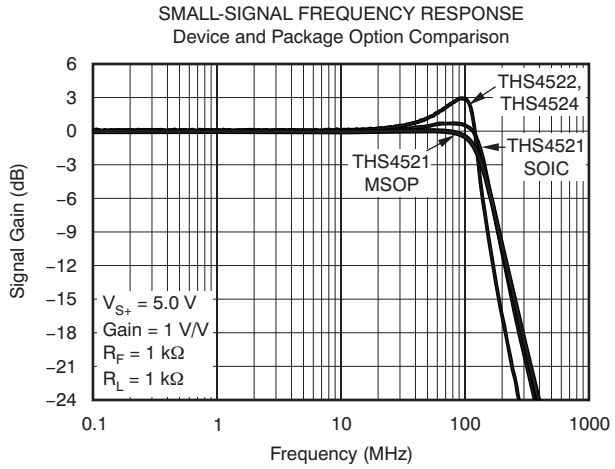


Figure 63. Small-Signal Frequency Response: Package Variations

8.3.10 Driving Capacitive Loads

The THS4521, THS4522, and THS4524 family is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors (R_O) in series with the output, placed as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in phase margin results in frequency response peaking; overshoot, undershoot, and/or ringing when a step or square-wave signal is applied; and may lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth. Figure 64 shows the recommended values of R_O versus capacitive loads (C_L), and Figure 65 shows an illustration of the frequency response with various values.

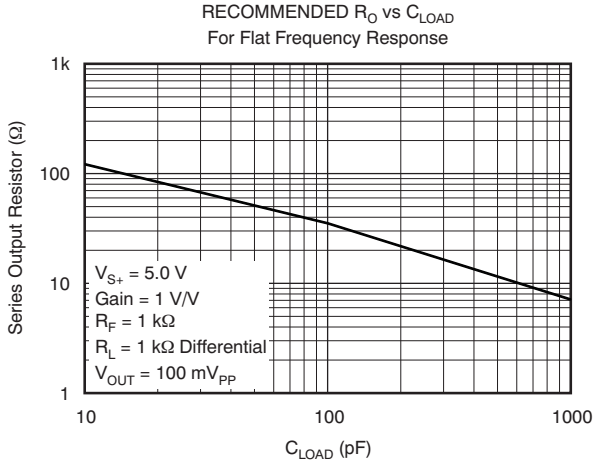


Figure 64. Recommended Series Output Resistor Versus Capacitive Load for Flat Frequency Response, With R_{LOAD} = 1 kΩ

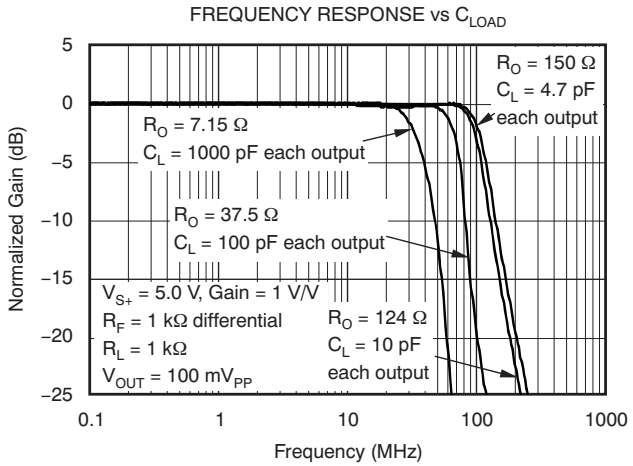


Figure 65. Frequency Response for Various R_O and C_L Values, With R_{LOAD} = 1 kΩ

8.3.11 Audio Performance

The THS4521, THS4522, and THS4524 family provide excellent audio performance with very low quiescent power. To show performance in the audio band, the device was tested with a SYS-2722 audio analyzer from Audio Precision. THD+N and FFT tests were performed at 1-V_{RMS} output voltage. Performance is the same on both 3.3-V and 5-V supplies. Figure 66 shows the test circuit used; see Figure 67 and Figure 68 for the performance of the analyzer using internal loopback mode (generator) together with the THS4521.

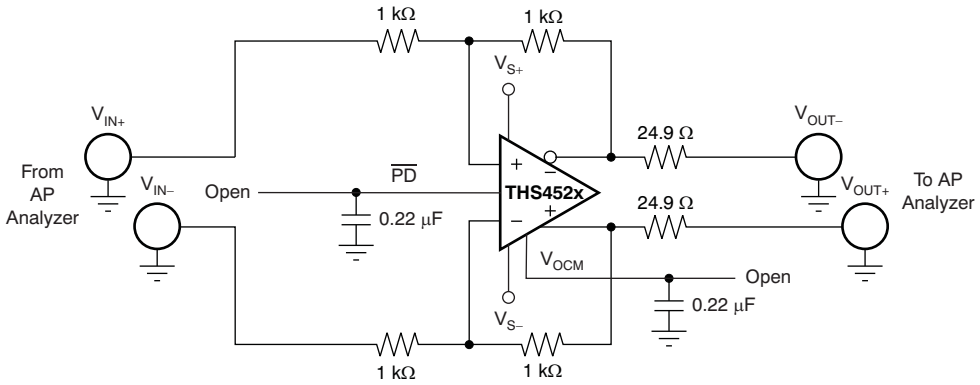


Figure 66. THS4521 AP Analyzer Test Circuit

Note that the harmonic distortion performance is very close to the same with and without the device meaning the THS4521 performance is actually much better than can be directly measured by this method. The actual device performance can be estimated by placing the device in a large noise gain and using the reduction in loop gain correction. The THS4521 is placed in a noise gain of 101 by adding a 10-Ω resistor directly across the input terminals of the circuit shown in Figure 66. This test was performed using the AP instrument as both the signal source and the analyzer. The second-order harmonic distortion at 1 kHz is estimated to be –122 dBc with V_O = 1V_{RMS}; third-order harmonic distortion is estimated to be –141 dBc. The third-order harmonic distortion result matches exactly with design simulations, but the second-order harmonic distortion is about 10 dB worse. This result is not unexpected because second-order harmonic distortion performance with a differential signal depends heavily on cancellation as a result of the differential nature of the signal, which depends on board layout, bypass capacitors, external cabling, and so forth. Note that the circuit of Figure 66 is also used to measure crosstalk between channels.

The THS4521 shows even better THD+N performance when driving higher amplitude output, such as 5 V_{PP} that is more typical when driving an ADC. To show performance with an extended frequency range, higher gain, and higher amplitude, the device was tested with 5 V_{PP} up to 80 kHz with the AP. Figure 69 shows the resulting THD+N graph with no weighting.

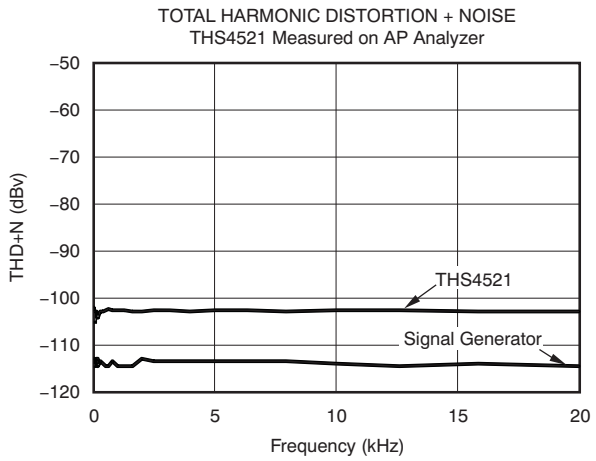


Figure 67. THS4521 1-V_{RMS} 20-Hz to 20-kHz Thd+N

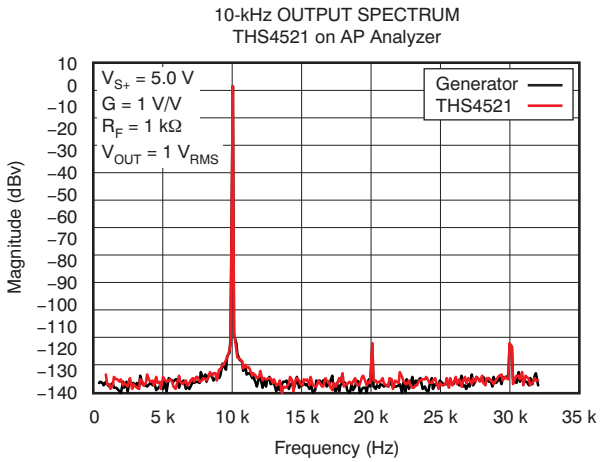


Figure 68. THS4521 1-V_{RMS} 10-kHz FFT Plot

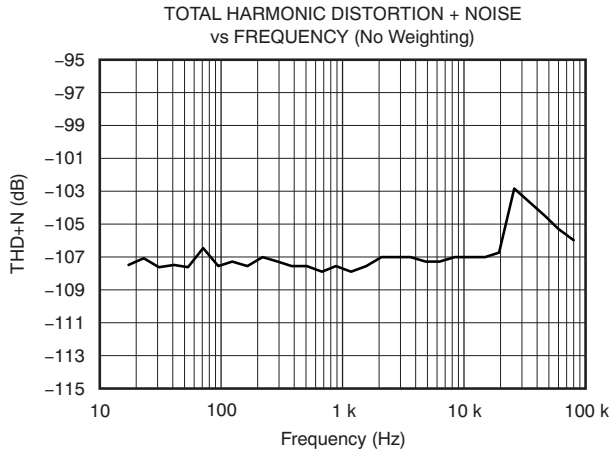


Figure 69. Thd+N (No Weighting) on Ap, 80-kHz Bandwidth at G = 1 With 5-V_{PP} Output

8.3.12 Audio On/Off Pop Performance

The THS4521 was tested to show on and off pop performance by connecting a speaker between the differential outputs and switching the power supply on and off, and also by using the $\overline{PD}$ function of the THS4521. Testing was done with and without tones. During these tests, no audible pop could be heard.

With no tone input, Figure 70 shows the pop performance when switching power on to the THS4521 and Figure 71 shows the device performance when turning the power off. The transients during power on and off illustrate that no audible pop should be heard

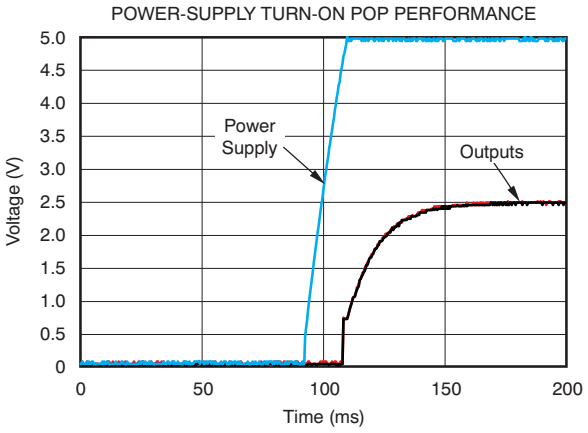


Figure 70. THS4521 Power-Supply Turn-On Pop Performance

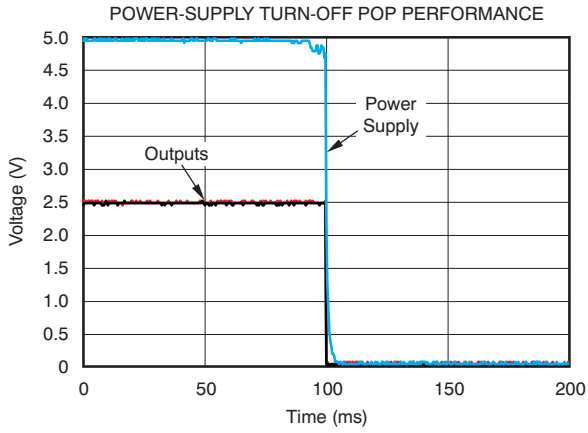


Figure 71. THS4521 Power-Supply Turn-Off Pop Performance

With no tone input, Figure 72 shows the pop performance using the $\overline{PD}$ pin to enable the THS4521, and Figure 73 shows performance using the $\overline{PD}$ pin to disable the device. Again, the transients during power on and off show that no audible pop should be heard. It should also be noted that the turn on/off times are faster using the $\overline{PD}$ pin technique.

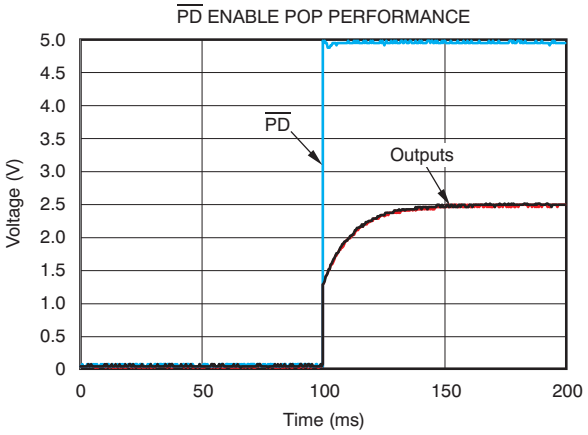


Figure 72. THS4521 $\overline{PD}$ Pin Enable Pop Performance

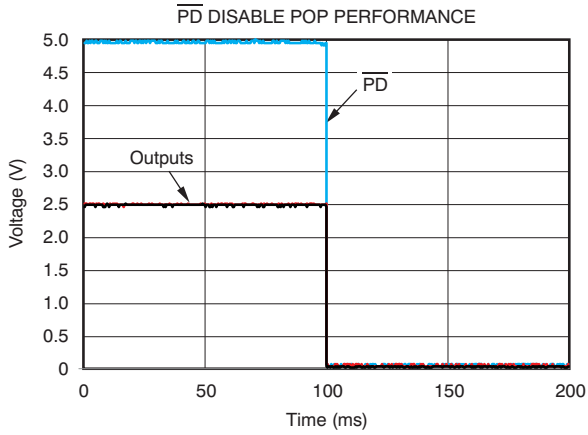


Figure 73. THS4521 $\overline{PD}$ Pin Disable Pop Performance

The power on/off pop performance of the THS4521, whether by switching the power supply or when using the power-down function built into the chip, shows that no special design should be required to prevent an audible pop.

8.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than V_{S-} + 1.7 V, or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The V_{OCM} control pin sets the output average voltage. Left open, V_{OCM} defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal V_{CM} error amplifier.

8.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the R_G value. This input-active-impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in the following subsections.

8.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be ac-coupled, the dc biasing for the THS452x family becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac-coupled and the output dc-coupled, or the output can be ac-coupled and the input dc-coupled, or they can both be ac-coupled.

One situation where the output might be dc-coupled (for an ac-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. In any case, the design starts by setting the desired V_{OCM}.

When an ac-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at midsupply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91 V greater than the negative supply and 1.1 V less than the positive supply). If the output path is also ac-coupled, simply letting the V_{OCM} control pin float is usually preferred in order to get a midsupply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the V_{OCM} pin to ground.

After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} plus the positive or negative output swing on each side do not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the non-signal input side are dc-blocked (see Figure 74), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher V_{OCM} voltages. Because the input V_{ICM} is the output V_{OCM} for ac-coupled sources, the 1.2-V minimum headroom for the input pins to the positive supply overrides the 1.1-V headroom limit for the output V_{OCM}. Also, the input signal moves this input V_{ICM} around the dc bias point, as described in the section *Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA*.

Device Functional Modes (continued)

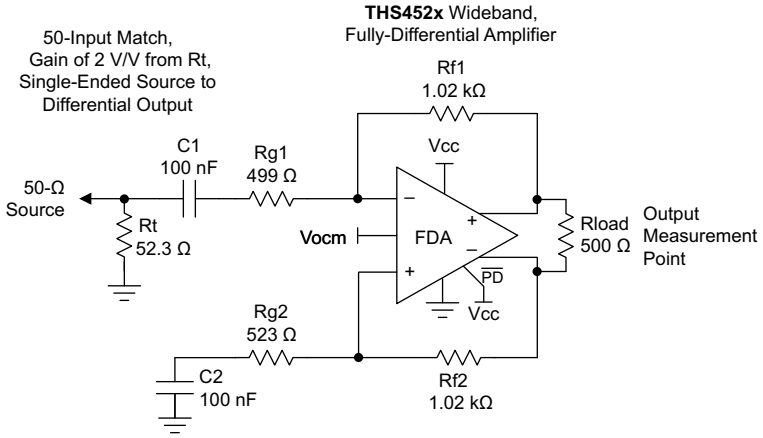


Figure 74. AC-coupled, Single-ended Source to a Differential Gain of 2 V/V Test Circuit

8.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc-coupled while the output is ac-coupled. A dc-coupled input with an ac-coupled output might have some advantages to move the input V_{ICM} down if the source is ground referenced. When the source is dc-coupled into the THS452x family (see Figure 75), both sides of the input circuit must be dc-coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around V_{OCM} at the outputs.

Often, R_{G2} is simply grounded for dc-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source is swinging around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around V_{OCM}.

One significant consideration for a dc-coupled input is that V_{OCM} sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_{IN} through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range.

If the average source is at ground, the negative rail input stage for the THS452x family is in range for applications using a single positive supply and a positive output V_{OCM} setting because this dc current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

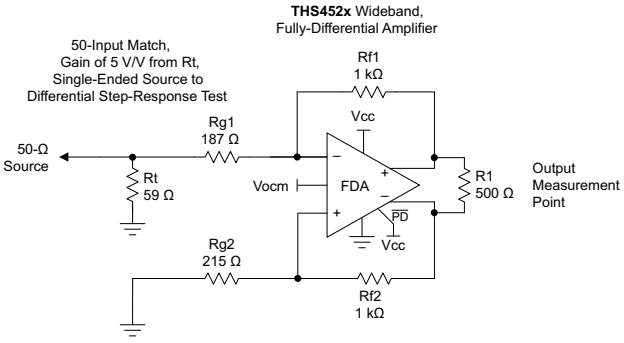


Figure 75. DC-Coupled, Single-Ended-to-Differential, Set for a Gain of 5 V/V

Device Functional Modes (continued)

8.4.1.3 Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA

The design equations for setting the resistors around an FDA to convert from a single-ended input signal to differential output can be approached from several directions. Here, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and set equal on the two sides.
- The dc and ac impedances from the summing junctions back to the signal source and ground (or a bias voltage on the non-signal input side) are set equal to retain feedback divider balance on each side of the FDA.

Both of these assumptions are typical for delivering the best dynamic range through the FDA signal path.

After the feedback resistor values are chosen, the aim is to solve for the R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the nonsignal input side); see Figure 74 and Figure 75. The same resistor solutions can be applied to either ac- or dc-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element (as shown in Figure 74) has the advantage of removing any dc currents in the feedback path from the output V_{OCM} to ground.

Earlier approaches to the solutions for R_T and R_{G1} (when the input must be matched to a source impedance, R_S) follow an iterative approach. This complexity arises from the active input impedance at the R_{G1} input. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the R_{G2} element. A more recent solution is shown as Equation 1, where a quadratic in R_T can be solved for an exact value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are:

1. The selected R_F value.
2. The target voltage gain (A_v) from the input of R_T to the differential output voltage.
3. The desired input impedance at the junction of R_T and R_{G1} to match R_S.

Solving this quadratic for R_T starts the solution sequence, as shown in Equation 1:

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2 + A_V) - R_S A_V(4 + A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2 + A_V) - R_S A_V(4 + A_V)} = 0 \quad (1)$$

Being a quadratic, there are limits to the range of solutions. Specifically, after R_F and R_S are chosen, there is physically a maximum gain beyond which Equation 1 starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, use Equation 2 to verify that the maximum gain is greater than the desired gain.

$$A_{V(MAX)} = \left(\frac{R_F}{R_S} - 2\right) \times \left[1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right] \quad (2)$$

If the achievable $A_{V(MAX)}$ is less than desired, increase the R_F value. After R_T is derived from Equation 1, the R_{G1} element is given by Equation 3:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \quad (3)$$

Device Functional Modes (continued)

Then, the simplest approach is to use a single $R_{G2} = R_T \parallel R_S + R_{G1}$ on the non-signal input side. Often, this approach is shown as the separate R_{G1} and R_S elements. Using these separate elements provides a better divider match on the two feedback paths, but a single R_{G2} is often acceptable. A direct solution for R_{G2} is given as Equation 4:

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \quad (4)$$

This design proceeds from a target input impedance matched to R_S, signal gain A_v from the matched input to the differential output voltage, and a selected R_F value. The nominal R_F value chosen for the THS452x family characterization is 402 Ω. As discussed previously, going lower improves noise and phase margin, but reduces the total output load impedance possibly degrading harmonic distortion. Going higher increases the output noise, and might reduce the loop-phase margin because of the feedback pole to the input capacitance, but reduces the total loading on the outputs.

Using Equation 2 to Equation 4 to sweep the target gain from 1 to $A_{V(MAX)}$ < 14.3 V/V gives Table 7, which shows exact values for R_T, R_{G1}, and R_{G2}, where a 50-Ω source must be matched while setting the two feedback resistors to 402 Ω. One possible solution for 1% standard values is shown, and the resulting actual input impedance and gain with % errors to the targets are also shown in Table 7.

Table 7. Rf = 1 kΩ, Matched Input to 50 Ω, Gain from 1 V to 10 V/V Single to Differential(1)

Av	Rt, EXACT (Ω)	Rt 1%	Rg1, EXACT (Ω)	Rg1 1%	Rg2, EXACT (Ω)	Rg2 1%	ACTUAL Z_{IN}	%ERR TO Rs	ACTUAL GAIN	%ERR TO Av
1	51.95	52.3	996.92	1000	1022.48	1020	50.32	0.64%	0.997	–0.30%
2	53.59	53.6	491.51	487	517.37	523	49.95	–0.10%	2.018	0.88%
3	55.21	54.9	322.74	324	348.90	348	49.70	–0.60%	2.989	–0.36%
4	56.88	56.2	238.14	237	264.60	267	49.37	–1.25%	4.017	0.43%
5	58.63	59	189.45	191	216.51	215	50.23	0.47%	4.964	–0.71%
6	60.47	60.4	155.01	154	182.37	182	49.82	–0.37%	6.033	0.56%
7	62.42	61.9	130.39	130	158.05	158	49.51	–0.98%	7.017	0.25%
8	64.49	64.9	112.97	113	141.21	140	50.12	0.23%	7.998	–0.02%
9	66.70	66.5	98.31	97.6	126.85	127	49.69	–0.62%	9.050	0.56%
10	69.06	69.8	87.40	86.6	116.53	118	50.29	0.57%	10.069	0.69%

(1) R_F = 1 kΩ, R_S = 50 Ω.

These equations and design flow apply to any FDA. Using the feedback resistor value as a starting point is particularly useful for current-feedback-based FDAs such as the LMH6554, where the value of these feedback resistors determines the frequency response flatness. Similar tables can be built using the equations provided here for other source impedances, R_F values, and gain ranges.

The TINA model correctly shows this actively-set input impedance in the single-ended to differential configuration, and is a good tool to validate the gains, input impedances, response shapes, and noise issues.

8.4.1.4 Input Impedance for the Single-Ended to Differential FDA Configuration

The designs so far have included a source impedance, R_S, that must be matched by R_T and R_{G1}. The total impedance at the junction of R_T and R_{G1} for the circuit of Figure 75 is the parallel combination of R_T to ground, and the ZA (active impedance) presented by R_{G1}. The expression for ZA, assuming R_{G2} is set to obtain the differential divider balance, is given by Equation 5:

$$ZA = R_{G1} \frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{5}$$

For designs that do not need impedance matching, for instance where the input is driven from the low-impedance output of another amplifier, $R_{G1} = R_{G2}$ is the single-to-differential design used without an R_T to ground. Setting $R_{G1} = R_{G2} = R_G$ in Equation 5 produces Equation 6, which is the input impedance of a simple-input FDA driven from a low-impedance, single-ended source.

$$ZA = 2R_G \frac{\left(1 + \frac{R_F}{R_G}\right)}{2 + \frac{R_F}{R_G}} \tag{6}$$

In this case, setting a target gain as $R_F / R_G \equiv \alpha$, and then setting the desired input impedance allows the R_G element to be resolved first. Then the R_F is set to get the target gain. For example, targeting an input impedance of 200 Ω with a gain of 4 V/V, Equation 7 calculates the R_G value. Multiplying this required R_G value by a gain of 4 gives the R_F value and the design of Figure 76.

$$R_G = ZA \frac{2 + \alpha}{2(1 + \alpha)} \tag{7}$$

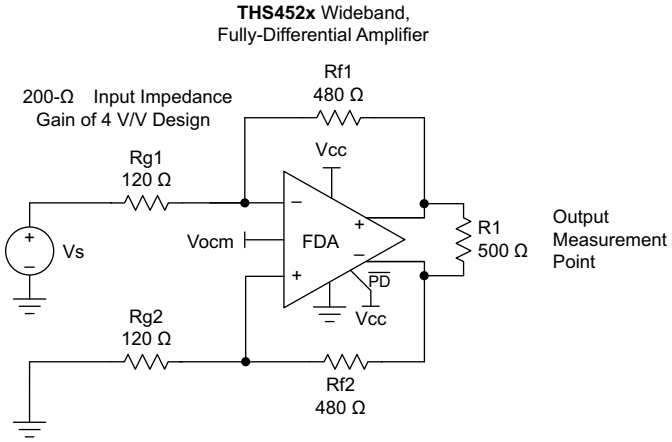


Figure 76. 200-Ω Input Impedance, Single-Ended to Differential DC-Coupled Design With Gain of 4 V/V

After being designed, this circuit can also be ac-coupled by adding blocking caps in series with the two 120-Ω R_G resistors. This active input impedance has the advantage of increasing the apparent load to the prior stage using lower resistors values, leading to lower output noise for a given gain target.

8.4.2 Differential-Input to Differential-Output Operation

In many ways, this method is a much simpler way to operate the FDA from a design-equations perspective. Again, assuming the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be dc biased in the allowable range for the input pins with consideration given to the voltage headroom required from each supply. Slightly different considerations apply to ac- or dc-coupled, differential-in to differential-out designs, as described in the following sections.

8.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the THS452x family with an ac-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). Figure 77 shows a typical blocking capacitor approach to a differential input. An optional differential-input termination resistor (R_M) is included in this design. This R_M element allows the input R_G resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the R_G elements sum to show a 500-Ω differential impedance, while the R_M element combines in parallel to give a net 100-Ω, ac-coupled, differential impedance to the source. Again, the design proceeds ideally by selecting the R_F element values, then the R_G to set the differential gain, then an R_M element (if needed) to achieve the target input impedance. Alternatively, the R_M element can be eliminated, the R_G elements set to the desired input impedance, and R_F set to the get the differential gain (R_F / R_G).

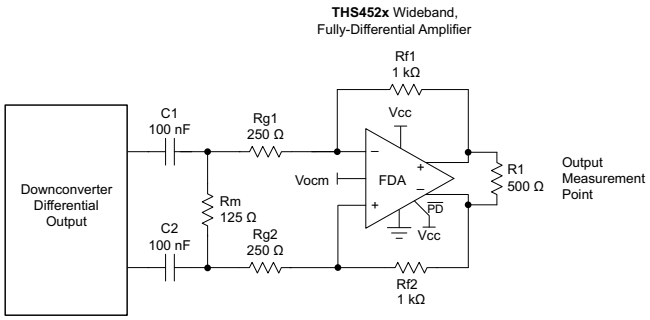


Figure 77. Example Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the THS452x

The dc biasing here is very simple. The output V_{OCM} is set by the input control voltage; and because there is no dc-current path for the output common-mode voltage, that dc bias also sets the input pins common-mode operating points.

8.5 Programming

8.5.1 Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential amplifier is the voltage at the **+** and **–** input pins of the device.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the amplifier. Assuming the amplifier is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the amplifier.

Treating the negative input as a summing node, the voltage is given by Equation 8:

$$\left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \tag{8}$$

To determine the V_{ICR} of the amplifier, the voltage at the negative input is evaluated at the extremes of V_{OUT+}. As the gain of the amplifier increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

8.5.1.1 Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

Figure 78 represents the V_{OCM} input. The internal V_{OCM} circuit has typically 23 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A 0.22-µF bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 9:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50\ k\Omega} \tag{9}$$

where:

- V_{OCM} is the voltage applied to the V_{OCM} pin

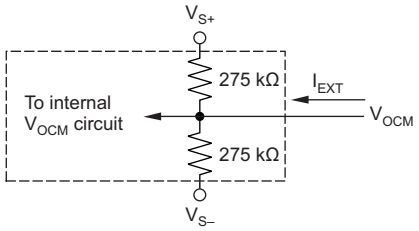


Figure 78. V_{OCM} Input Circuit

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following circuits show application information for the THS4521, THS4522, and THS4524 family. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see *Layout Guidelines* for suggested guidelines. For more details on the use and operation of fully differential amplifiers, refer to the Application Report *Fully-Differential Amplifiers* (SLOA054), available for download from the TI web site at www.ti.com.

9.2 Typical Applications

9.2.1 Audio ADC Driver Performance: THS4521 and PCM4204 Combined Performance

To show achievable performance with a high-performance audio ADC, the THS4521 is tested as the drive amplifier for the PCM4204. The PCM4204 is a high-performance, four-channel ADC designed for professional and broadcast audio applications. The PCM4204 architecture uses a 1-bit delta-sigma (ΔΣ) modulator per channel that incorporates an advanced dither scheme for improved dynamic performance, and supports PCM output data. The PCM4204 provides a flexible serial port interface and many other advanced features. Refer to the PCM4204 product data sheet for more information.

The PCM4204EVM can test the audio performance of the THS4521 as a drive amplifier. The standard PCM4204EVM is provided with four OPA1632 fully-differential amplifiers, which use the same device pinout as the THS4521. For testing, one of these amplifiers is replaced with a THS4521 device in same package (MSOP), and the power supply changes to a single-supply +5V. Figure 79 shows the modifications made to the circuit. Note the resistor connecting the V_{OCM} input of the THS4521 to the input common-mode drive from the PCM4204 is shown removed and is optional; no performance change was noted with it connected or removed. The THS4521 is operated with a +5-V single-supply so the output common-mode defaults to +2.5 V as required at the input of the PCM4204. The EVM power connections were modified by connecting positive supply inputs, +15 V, +5 VA and +5 VD, to a +5-V external power supply (EXT +3.3 was not used) and connecting –15 V and all ground inputs to ground on the external power supply. Note only one external +5-V supply was needed to power all devices on the EVM.

A SYS-2722 Audio Analyzer from Audio Precision (AP) provides an analog audio input to the EVM; the PCM-formatted digital output is read by the digital input on the AP.

Data were taken using a 256-f_S system clock to achieve f_S = 48-kHz measurements, and audio output uses PCM format. Other data rates and formats are expected to show similar performance in line with that shown in the product data sheet.

Figure 82 shows the THD+N vs Frequency response with no weighting; Figure 83 shows an FFT of the output with 1-kHz input tone. Input signals to the PCM4204 for these tests is 0.5 dBFS. Dynamic range is also tested at –60 dBFS, f_{IN} = 1 kHz, and A-weighted. Table 8 summarizes testing results using the THS4521 together with the PCM4204 versus typical data sheet performance measurements, and show that it make an excellent drive amplifier for this ADC.

Typical Applications (continued)

The test circuit shown in Figure 79 has a gain = 0.27 and attenuates the input signal. For applications that require higher gain, the circuit was modified to gains of G = 1, G = 2, and G = 5 by replacing the feedback resistors (R33 and R34) and re-tested to show performance.

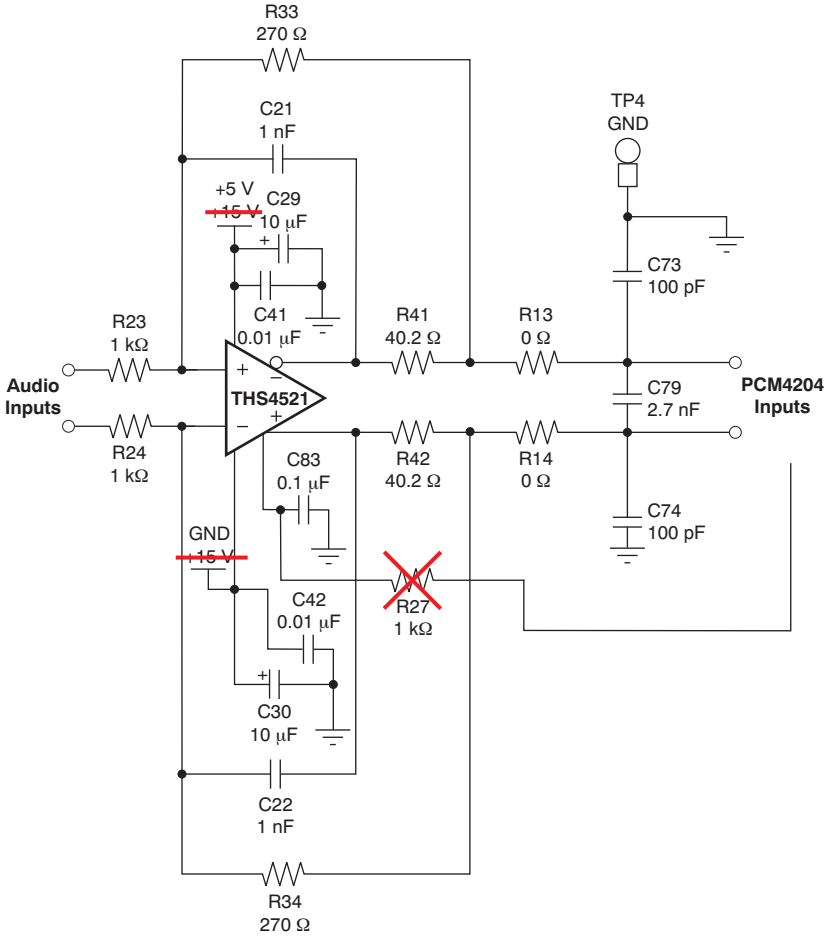


Figure 79. THS4521 and PCM4204 Test Circuit

Typical Applications (continued)

Figure 84 shows the THS4521 and PCM4204 THD+N versus frequency with no weighting at higher gains.

9.2.1.1 Design Requirements

Table 8. 1-kHz AC Analysis: Test Circuit Versus PCM4204 Data Sheet Typical Specifications (F_S = 48 kSPS)

Configuration	Tone	THD+N	Dynamic Range
THS4521 and PCM4204	1 kHz	–106 dBc	117 dB
PCM4204 Data sheet (typ)	1 kHz	–105 dBc	118 dB

9.2.1.2 Detailed Design Procedure

Table 9. THS4521EVM Parts List

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QTY	MANUFACTURER PART NUMBER
1	Capacitor, 10.0 µF, ceramic, X5R, 6.3 V	0805	C7, C8, C9, C10	4	(AVX) 08056D106KAT2A
2	Capacitor, 0.1 µF, ceramic, X7R, 16 V	0603	C3, C5, C11, C12	4	(AVX) 0603YC104KAT2A
3	Capacitor, 0.22 µF, ceramic, X7R, 10 V	0603	C1, C4, C6	3	(AVX) 0603ZC224KAT2A
4	Open	0603	C2, C13, C14, C15, C16	5	
5	Open	0603	R1, R2, R3, R7, R8, R9, R18, R19, R21, R22, R23, R26	12	
6	Resistor, 0 Ω	0603	R24, R25	2	(ROHM) MCR03EZPJ000
7	Resistor, 49.9 Ω, 1/10W, 1%	0603	R6	1	(ROHM) MCR03EZPFX49R9
8	Resistor, 52.3 Ω, 1/10W, 1%	0603	R10, R11, R20	3	(ROHM) MCR03EZPFX52R3
9	Resistor, 487 Ω, 1/10W, 1%	0603	R16, R17	2	(ROHM) MCR03EZPFX4870
10	Resistor, 1k Ω, 1/10W, 1%	0603	R12, R13, R14, R15	4	(ROHM) MCR03EZPFX1001
11	Resistor, 0 Ω	0805	R4, R5	2	(ROHM) MCR10EZPJ000
12	Open		T1	1	
13	Transformer, RF		T2	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, Banana receptance, 0.25-in dia. hole		J4, J5, J8	3	(SPC) 813
15	Open		J1, J3, J6, J7, J10, J11	6	
16	Connector, edge, SMA PCB jack		J2, J9	2	(JOHNSON) 142-0701-801
17	Header, 0.1 in CTRS, 0.025-in sq. pins	2 POS.	JP1	1	(SULLINS) PBC36SAAN
18	Shunts		JP1	1	(SULLINS) SSC02SYAN
19	Test point, Red		TP1	1	(KEYSTONE) 5000
20	Test point, Black		TP2, TP3	2	(KEYSTONE) 5001
21	IC, THS4521		U1	1	(TI) THS4521D
22	Standoff, 4-40 hex, 0.625 in length			4	(KEYSTONE) 1808
23	Screw, Phillips, 4-40, .250 in			4	SHR-0440-016-SN
24	Board, printed circuit			1	(TI) EDGE# 6494532

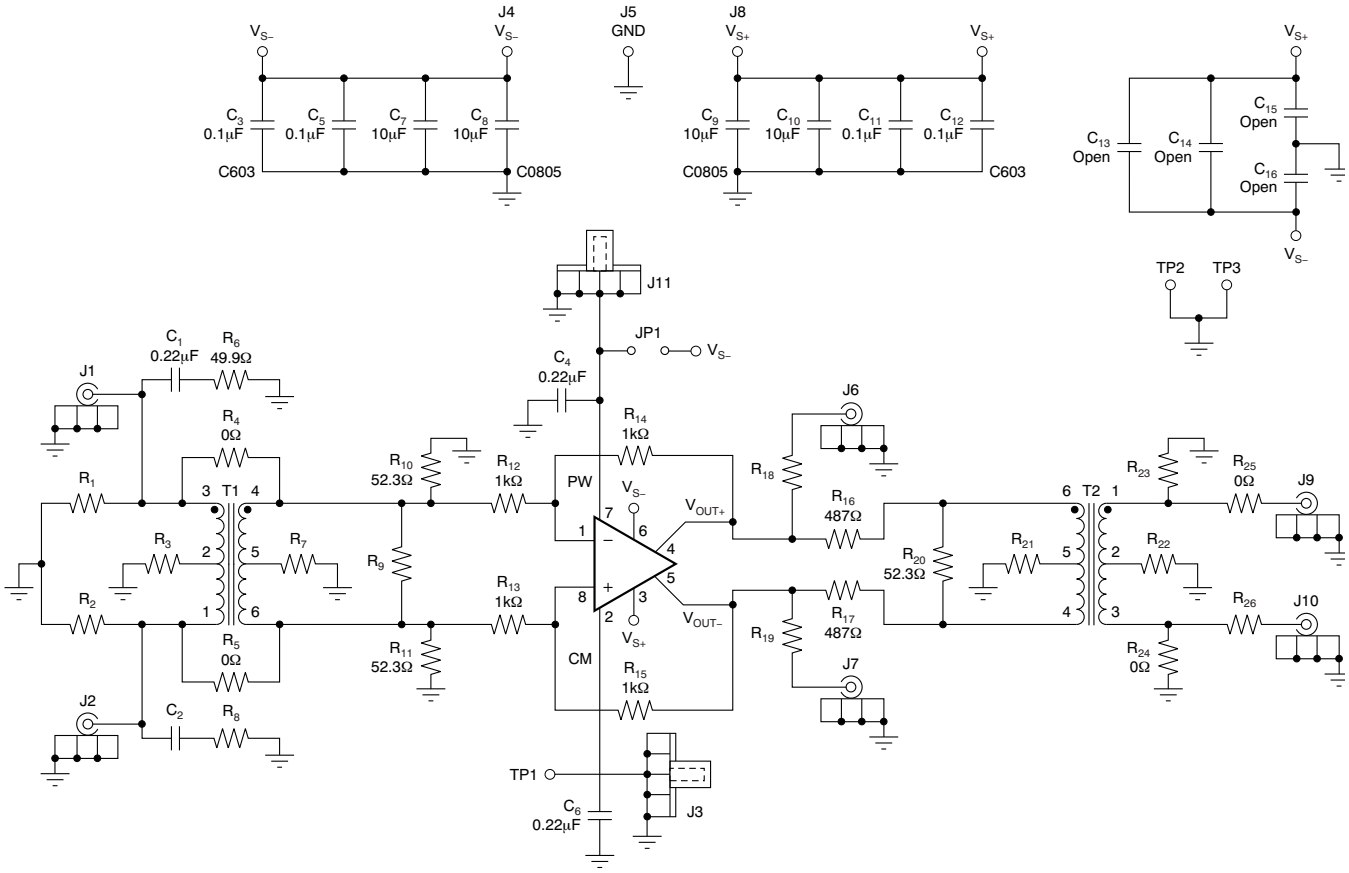


Figure 80. THS4521EVM: Schematic

9.2.1.2.1 Audio ADC Driver Performance: THS4521 and PCM3168 Combined Performance

The THS4521 is also tested as the drive amplifier for the PCM3168A ADC input. The PCM3168A is a high-performance, single-chip, 24-bit, 6-in/8-out, audio coder/decoder (codec) with single-ended and differential selectable analog inputs and differential outputs. The six-channel, 24-bit ADC employs a ΔΣ modulator and supports 8-kHz to 96-kHz sampling rates and a 16-bit/24-bit width digital audio output word on the audio interface. The eight-channel, 24-bit digital-to-analog converter (DAC) employs a ΔΣ modulator and supports 8-kHz to 192-kHz sampling rates and a 16-bit/24-bit width digital audio input word on the audio interface. Each audio interface supports I^2S™, left-/right-justified, and DSP formats with 16-bit/24-bit word width. In addition, the PCM3168A supports the time-division-multiplexed (TDM) format.. The PCM3168A provides flexible serial port interface and many other advanced features. Refer to the PCM3168A product data sheet for more information.

The PCM3168A EVM is used to test the audio performance of the THS4521 as a drive amplifier. The standard PCM3168A EVM is provided with OPA2134 operational amplifiers that are used to convert single-ended inputs to differential to drive the ADC. For testing, the operational amplifier output series resistors are removed from one of the channels and a THS4521, mounted on its standard EVM, is connected to the ADC inputs via short coaxial cables. The THS4521 EVM is configured for both differential inputs as shown in Figure 91 and for single-ended input as shown in Figure 92 with 1-kΩ resistors for R_F and R_G, and 24.9-Ω resistors in series with each output to isolate the outputs from the reactive load of the coaxial cables. To limit the noise from the external EVM and cables, a 2.7-nF capacitor is placed differentially across the PCM3168A inputs. The THS4521 is operated with a single-supply +5-V supply so the output common-mode of the THS4521 defaults to +2.5 V as required at the input of the PCM3168A. The PCM3168A EVM is configured and operated as described in the *PCM3168AEVM User's Guide*. The ADC was tested with an external THS4521 EVM with both single-ended input and differential inputs. In both configurations, the results are the same. Figure 81 shows the THD+N versus frequency and Table 10 compares the result to the PCM3168 data sheet typical specification at 1 kHz. Both graphs show that it makes an excellent drive amplifier for this ADC. **Note:** a 2700 series Audio Analyzer from Audio Precision is used to generate the input signals to the THS4521 and to analyze the digital data from the PCM3168.

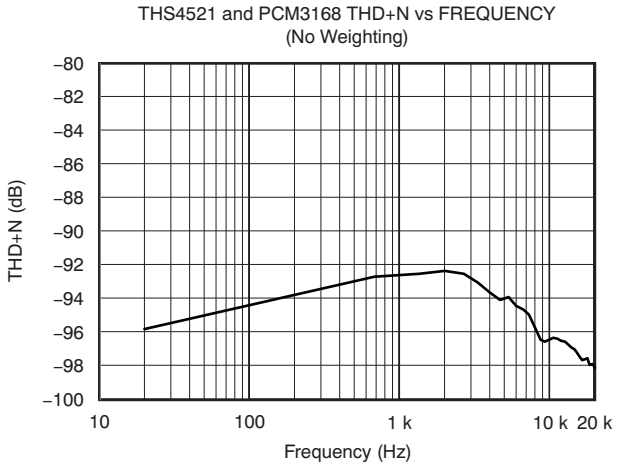


Figure 81. THS4521 and PCM3168: Thd+N Versus Frequency With No Weighting

Table 10. 1-kHz AC Analysis: Test Circuit vs PCM3168 Data Sheet Typical Specifications (F_S = 48 kSPS)

Configuration	Tone	THD+N
THS4521 and PCM3168	1 kHz	–92.6 dBc
PCM3168A Data sheet (typ)	1 kHz	–93 dBc

9.2.1.3 Application Curves

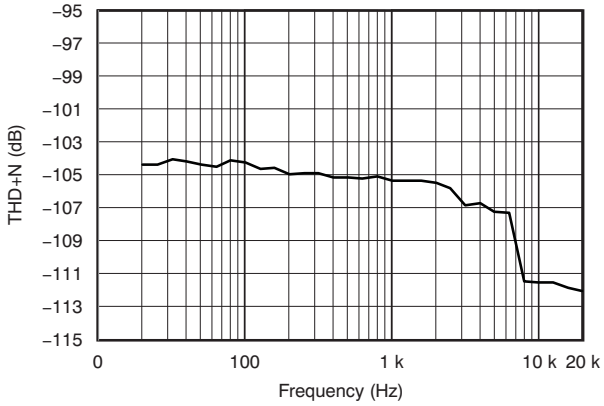


Figure 82. THS4521 and PCM4204: Thd+N Versus Frequency With No Weighting

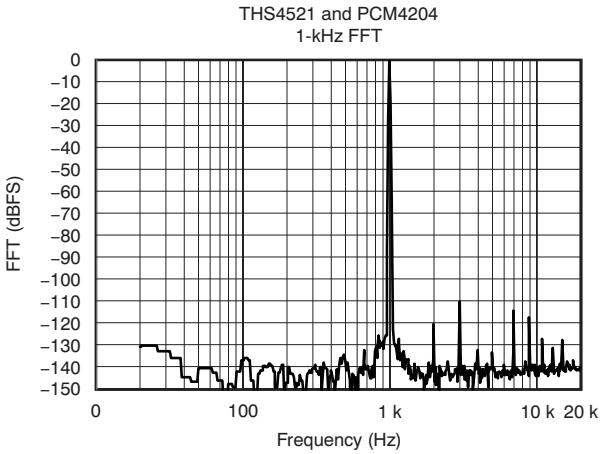


Figure 83. THS4521 and PCM4204 1-kHz FFT

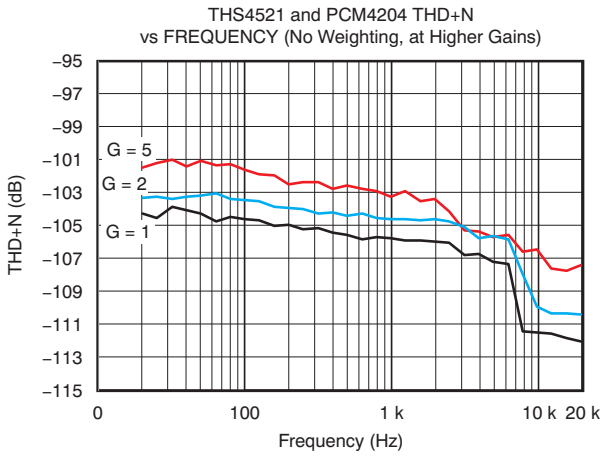


Figure 84. THS4521 and PCM4204: Thd+N Versus Frequency With No Weighting at Higher Gains

9.2.2 ADC Driver Performance: THS4521 and ADS1278 Combined Performance

The THS4521 provides excellent performance when driving high-performance ΔΣ and successive approximation register (SAR) ADCs in audio and industrial applications using a single 3-V to 5-V power supply. To show achievable performance, the THS4521 is tested as the drive amplifier for the ADS1278 24-bit ADC. The ADS1278 offers excellent ac and DC performance, with four selectable operating

modes from 10 kSPS to 128 kSPS to enable the user to fine-tune performance and power for specific application needs. The circuit shown in Figure 85 was used to test the performance. Data were taken using the High-Resolution mode (52 kSPS) of the ADS1278 with input frequencies at 1 kHz and 10 kHz and signal levels 1/2 dB below full-scale (–0.5 dBFS). FFT plots showing the spectral performance are given in Figure 87 and Figure 88; tabulated ac analysis results are shown in Table 11 and compared to the ADS1278 data sheet typical performance specifications.

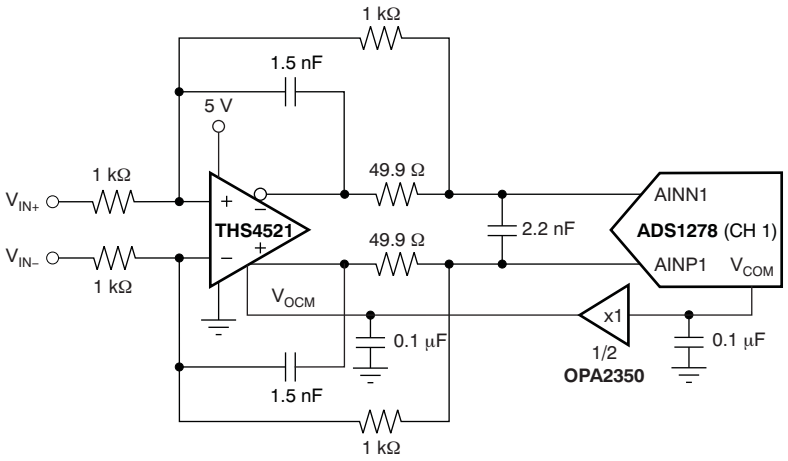


Figure 85. THS4521 and ADS1278 (Ch 1) Test Circuit

9.2.2.1 Design Requirements

Table 11. AC Analysis

Configuration	Tone	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
THS4521 and ADS1278	1 kHz	–0.5	109	–108	105	114
	10 kHz	–0.5	102	–110	101	110
ADS1278 Data sheet (typ)	1 kHz	–0.5	110	–108	—	109

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 ADC Driver Performance: THS4521 and ADS8321 Combined Performance

To demonstrate achievable performance, the THS4521 is tested as the drive amplifier for the ADS8321 16-bit SAR ADC. The ADS8321 offers excellent ac and dc performance, with ultra-low power and small size. The circuit shown in Figure 86 was used to test the performance.

Data were taken using the ADS8321 at 100 kSPS with input frequencies of 2 kHz and 10 kHz and signal levels that were -0.5 dBFS. FFT plots that illustrate the spectral performance are given in Figure 89 and Figure 90. Tabulated ac analysis results are listed in Table 12 and compared to the ADS8321 data sheet typical performance. Note the significant improvement in SFD using the THS4521 driver over just the ADC by itself.

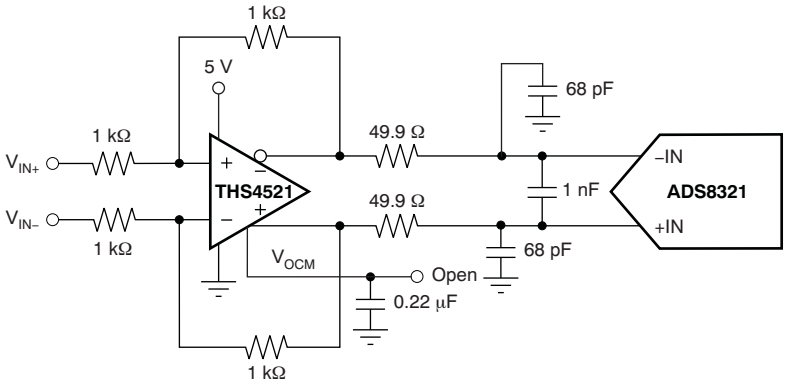


Figure 86. THS4521 and ADS8321 Test Circuit

Table 12. AC Analysis

Configuration	Tone	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
THS4521 and ADS8321	2 kHz	–0.5	86.7	–97.8	86.4	100.7
	10 kHz	–0.5	85.2	–98.1	85.2	102.2
ADS8321 Data sheet (typ)	10 kHz	–0.5	87	–86	84	86

9.2.2.3 Application Curves

The application curves below apply to the ADS14278 test.

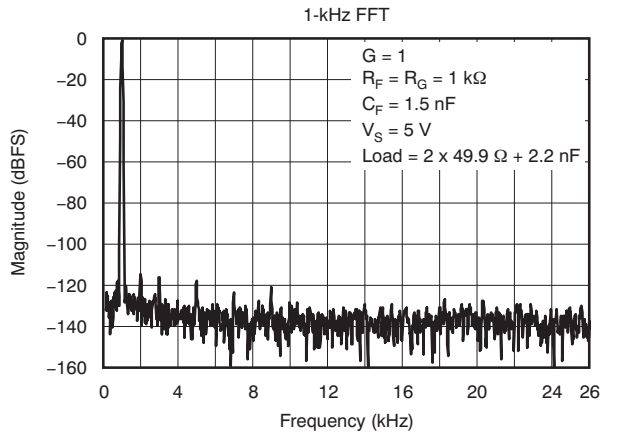


Figure 87. 1-kHz FFT

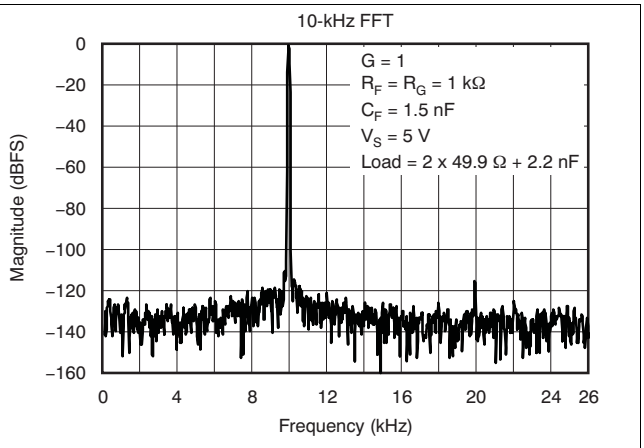


Figure 88. 10-kHz FFT

The application curves below apply to the ADS8321 test.

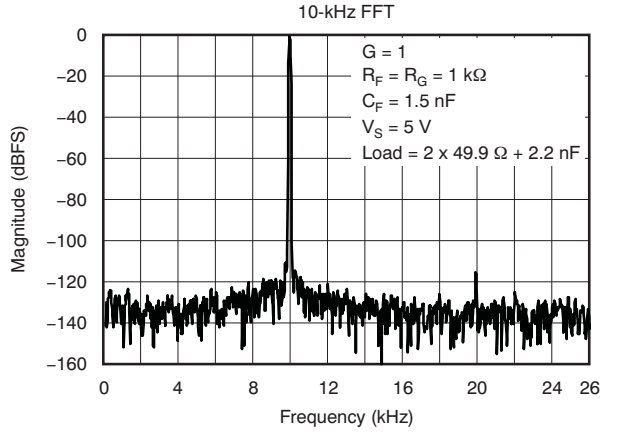


Figure 89. 2-kHZ FFT

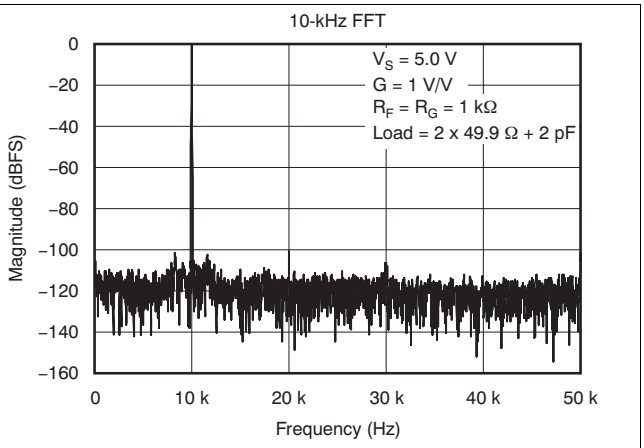


Figure 90. 10-kHz FFT

9.2.3 Differential Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family are fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. Figure 91 shows a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is set by R_F divided by R_G.

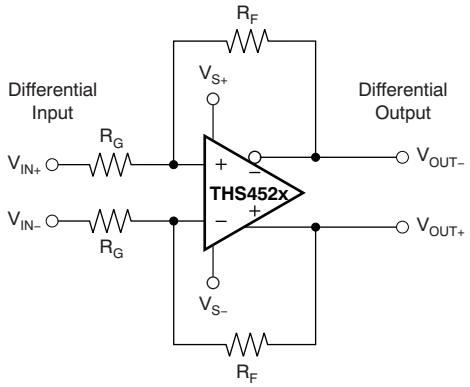


Figure 91. Differential Input to Differential Output Amplifier

9.2.4 Single-Ended Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family can also amplify and convert single-ended input signals to differential output signals. Figure 92 illustrates a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is again set by R_F divided by R_G.

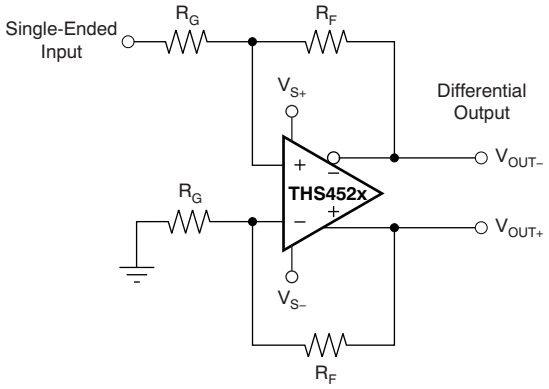


Figure 92. Single-Ended Input to Differential Output Amplifier

10 Power Supply Recommendations

The THS452x family is principally intended to operate with a nominal single-supply voltage of +3 V to +5 V. Supply-voltage tolerances are supported with the specified operating range of 2.5 V (10% low on a 3-V nominal supply) and 5.5 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in the *Application and Implementation*. Split (or bipolar) supplies can be used with the THS452x family, as long as the total value across the device remains less than 5.5 V (absolute maximum).

Using a negative supply to deliver a true swing to ground output in driving SAR ADCs may be desired. While the THS452x family quotes a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3- to 5-V positive supply input used by the THS452x and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective solution, as shown in the TI Designs TIDU187, Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts.

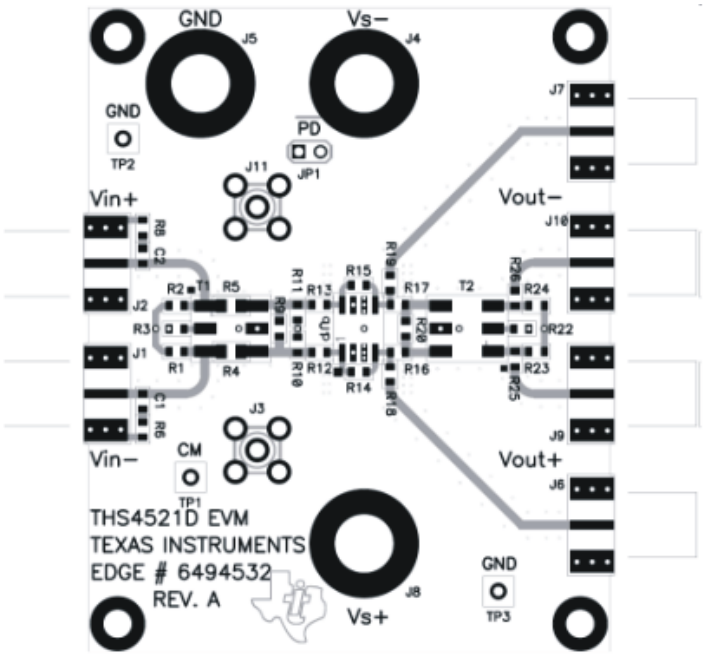
11 Layout

11.1 Layout Guidelines

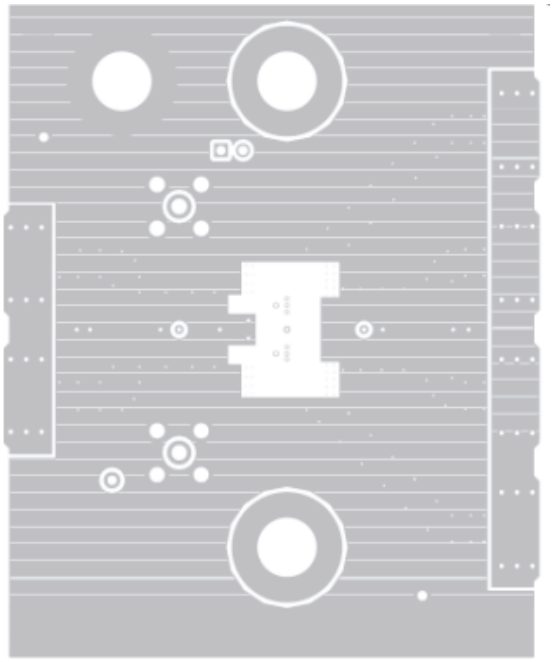
Figure 80 shows the THS4521EVM schematic. PCB layers 1 through 4 are shown in Figure 93; Table 9 lists the bill of materials for the THS4521EVM as supplied from TI. It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

- Signal routing should be direct and as short as possible into and out of the amplifier circuit.
- The feedback path should be short and direct.
- Ground or power planes should be removed from directly under the amplifier input and output pins.
- An output resistor is recommended in each output lead, placed as near to the output pins as possible.
- Two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
- Two 10-µF power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multiple analog devices.
- A 0.22-µF capacitor should be placed between the V_{OCM} input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
- The $\overline{PD}$ pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.
- If input termination resistors R_{10} and R_{11} are used, a single point connection to ground on L2 is recommended.

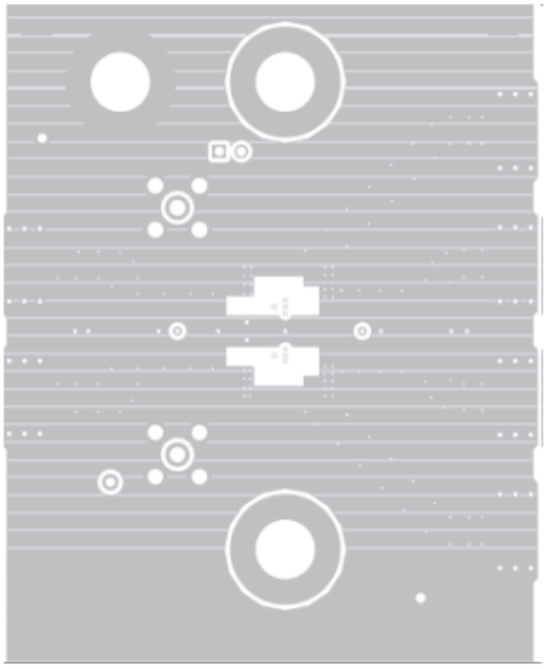
11.2 Layout Example



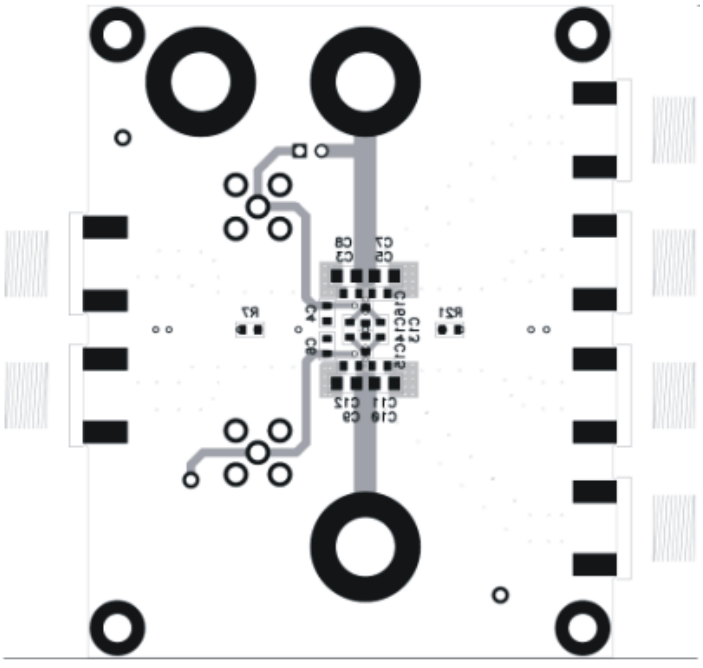
(a) Top Layer



(b) Power Layer



(c) Ground Layer



(d) Bottom Layer

Figure 93. THS4521EVM: Layer 1 to Layer 4 Images

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

Table 13 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 13. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THS4521	Click here	Click here	Click here	Click here	Click here
THS4522	Click here	Click here	Click here	Click here	Click here
THS4524	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
I^2S is a trademark of NXP Semiconductor.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4521ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4521ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4521IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	4521
THS4521IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4521
THS4521IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	4521
THS4521IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4521
THS4521IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4521IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4521IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4521IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521
THS4522IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4522
THS4522IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	-	Call TI	Call TI	-40 to 85	
THS4522IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4522
THS4522IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
THS4522IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4522
THS4522IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
THS4524IDBT	Active	Production	TSSOP (DBT) | 38	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4524
THS4524IDBT.B	Active	Production	TSSOP (DBT) | 38	50 | TUBE	-	Call TI	Call TI	-40 to 85	
THS4524IDBTR	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4524
THS4524IDBTR.B	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
THS4524IDBTRG4	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4524
THS4524IDBTRG4.B	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF THS4521, THS4524 :

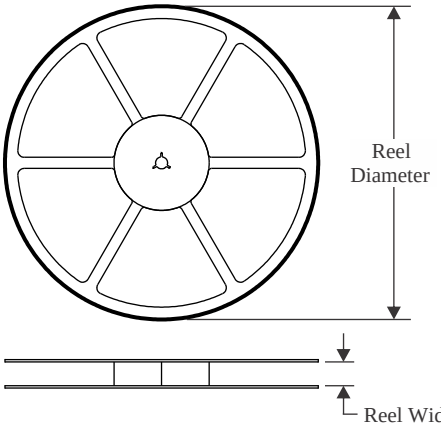
- Enhanced Product : THS4524-EP

NOTE: Qualified Version Definitions:

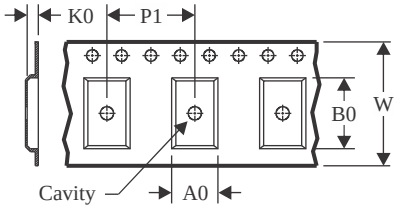
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

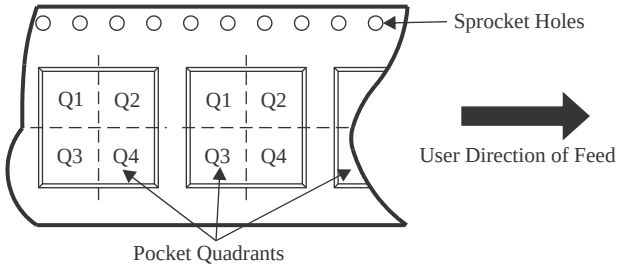


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

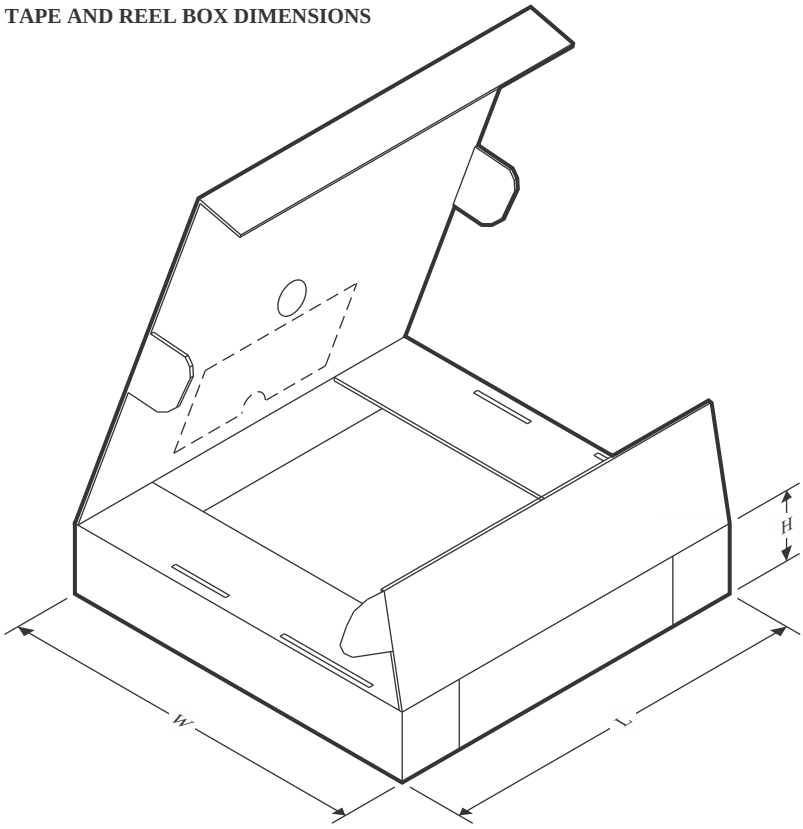
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4521IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4521IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4522IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
THS4522IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
THS4524IDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
THS4524IDBTRG4	TSSOP	DBT	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

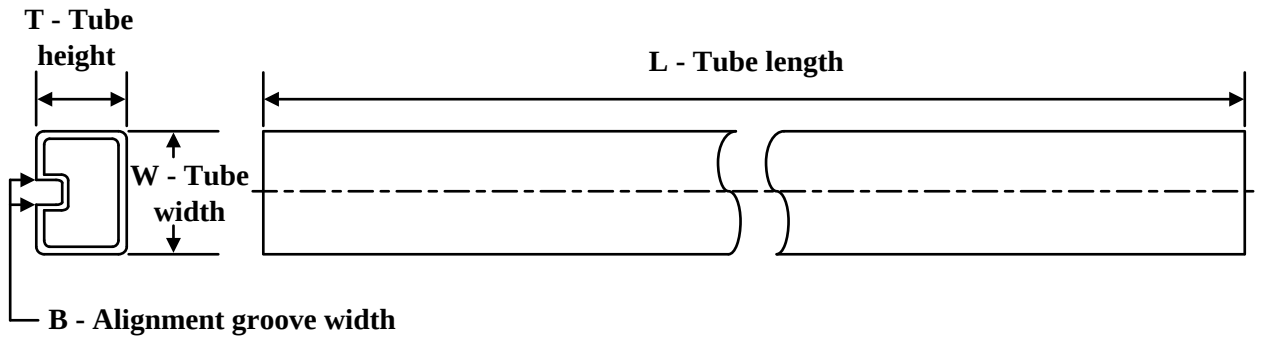
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4521IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THS4521IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
THS4521IDR	SOIC	D	8	2500	353.0	353.0	32.0
THS4521IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
THS4522IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
THS4522IPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
THS4524IDBTR	TSSOP	DBT	38	2000	353.0	353.0	32.0
THS4524IDBTRG4	TSSOP	DBT	38	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

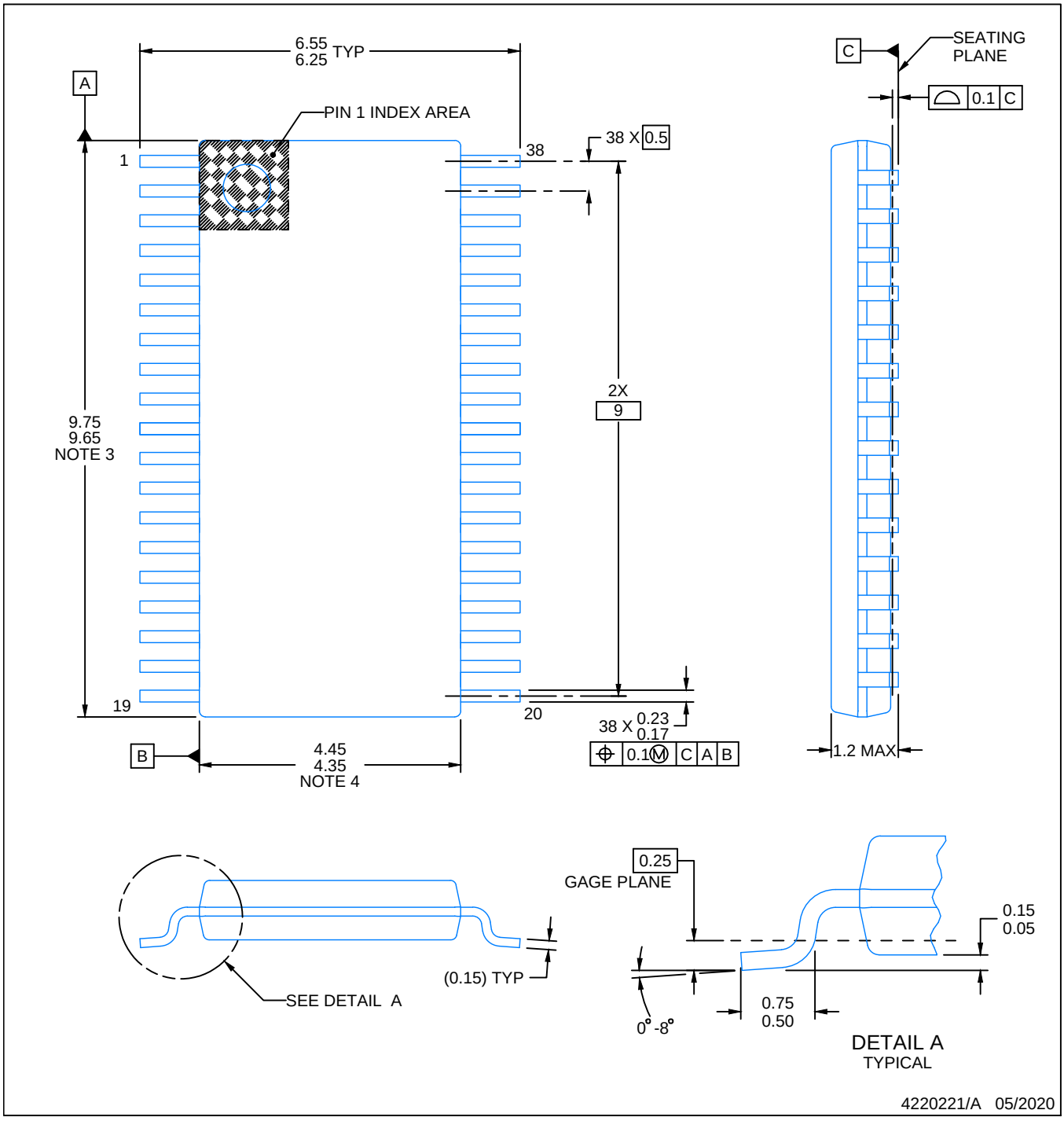
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4521ID	D	SOIC	8	75	506.6	8	3940	4.32
THS4521ID.B	D	SOIC	8	75	506.6	8	3940	4.32
THS4522IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
THS4524IDBT	DBT	TSSOP	38	50	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0038A

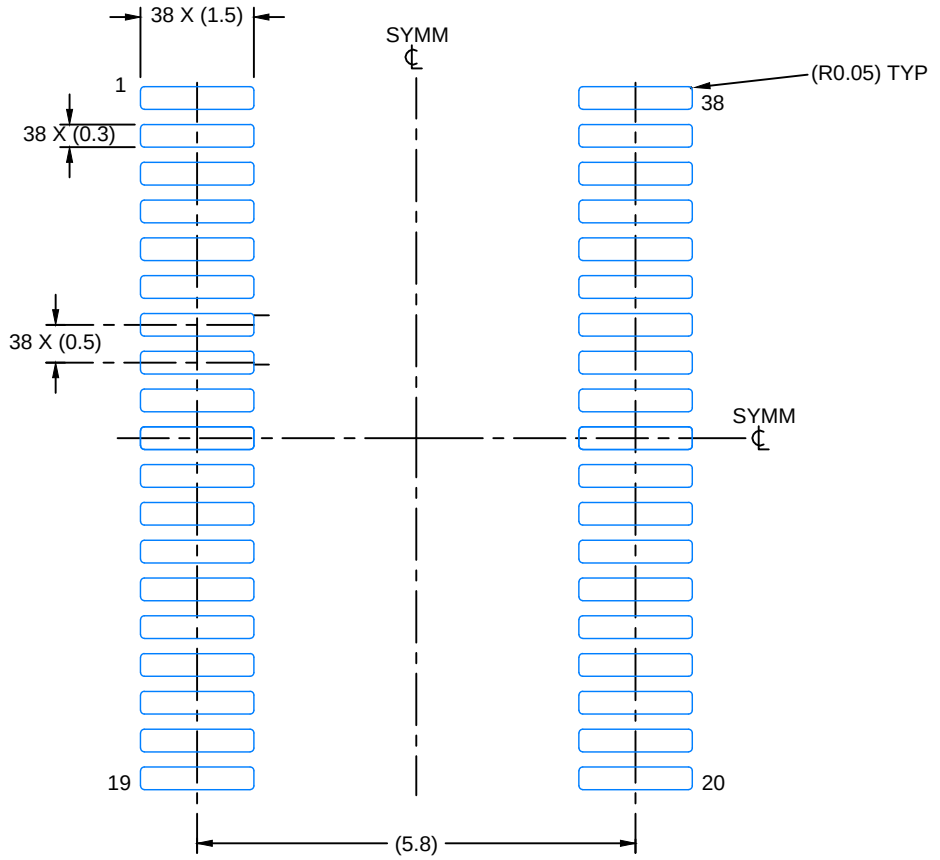
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

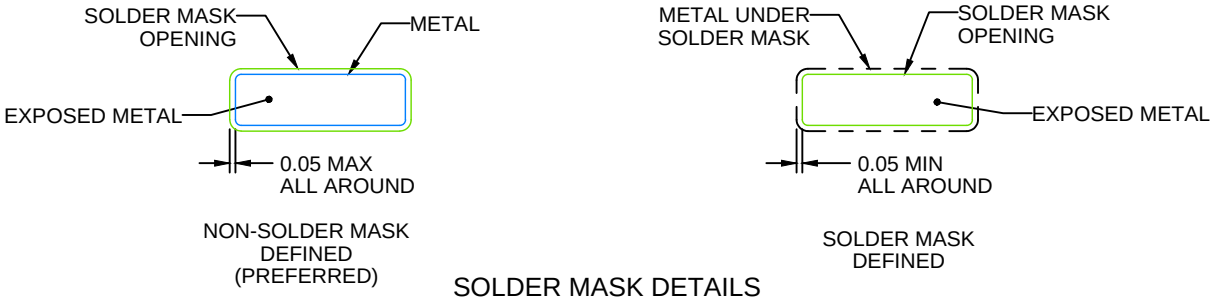


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

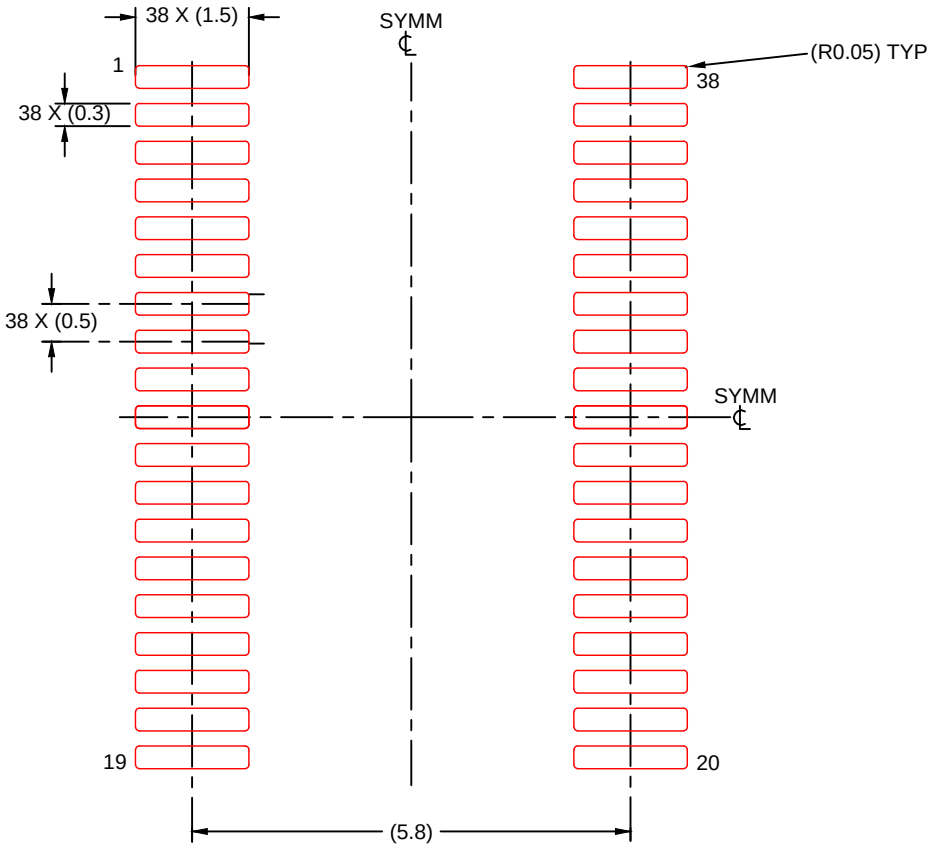


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

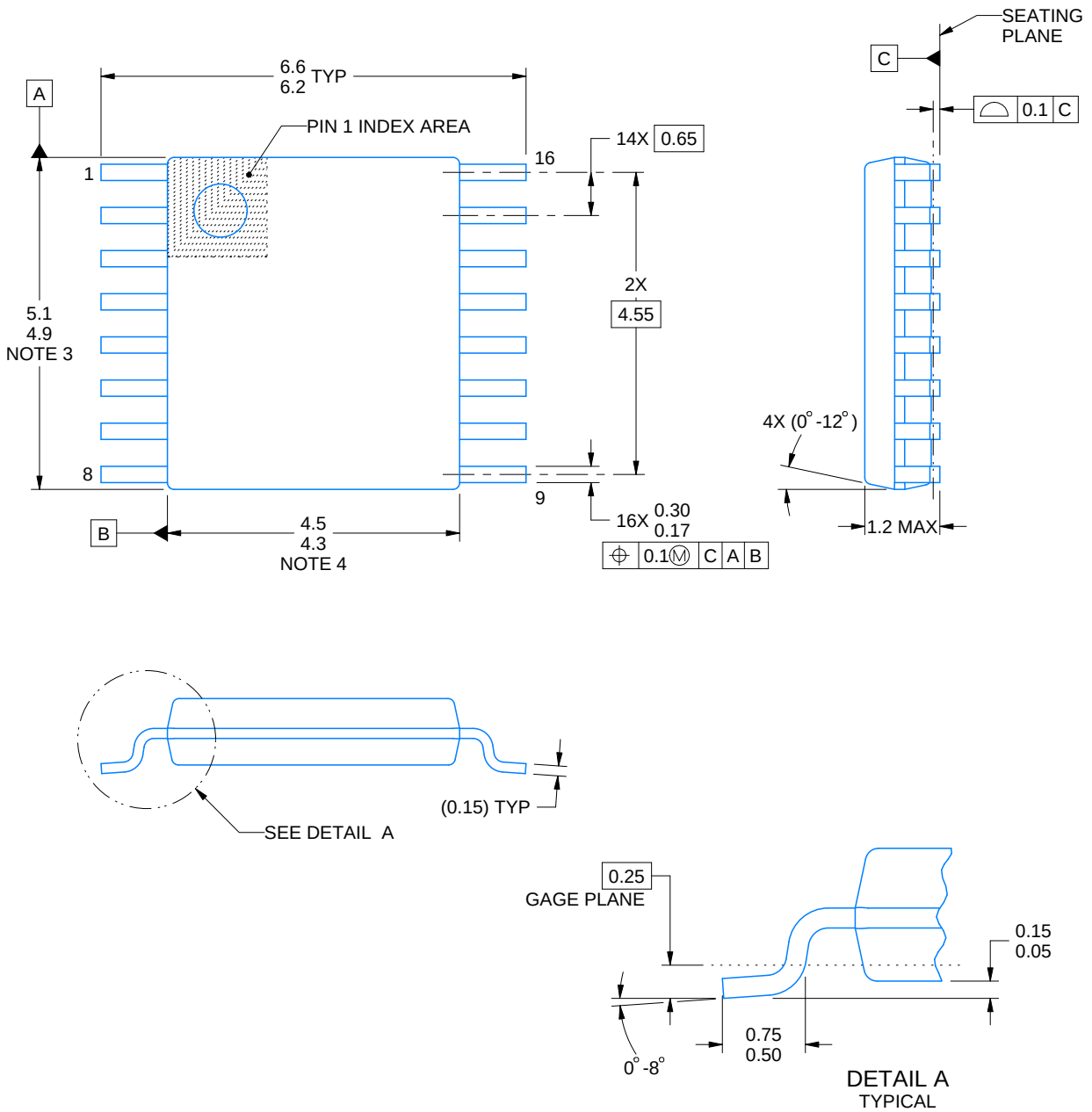
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

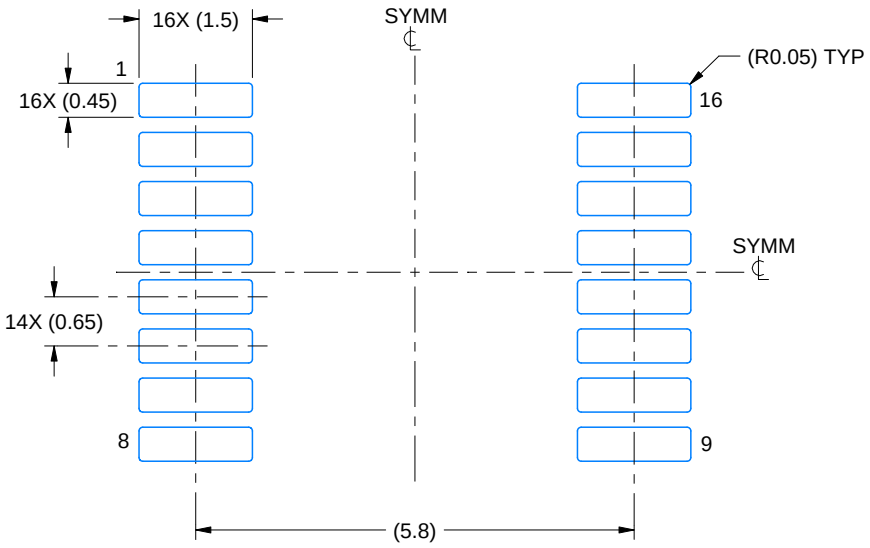
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



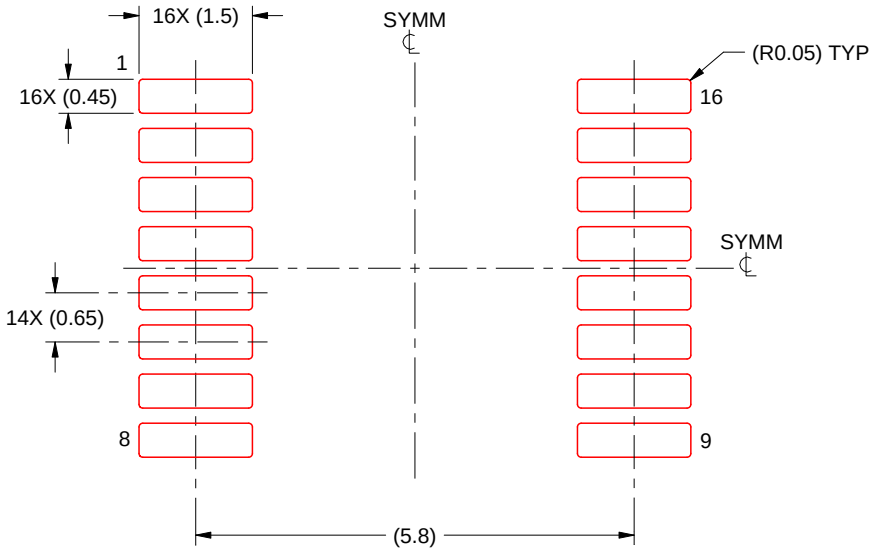
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

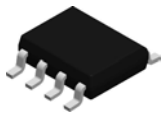


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

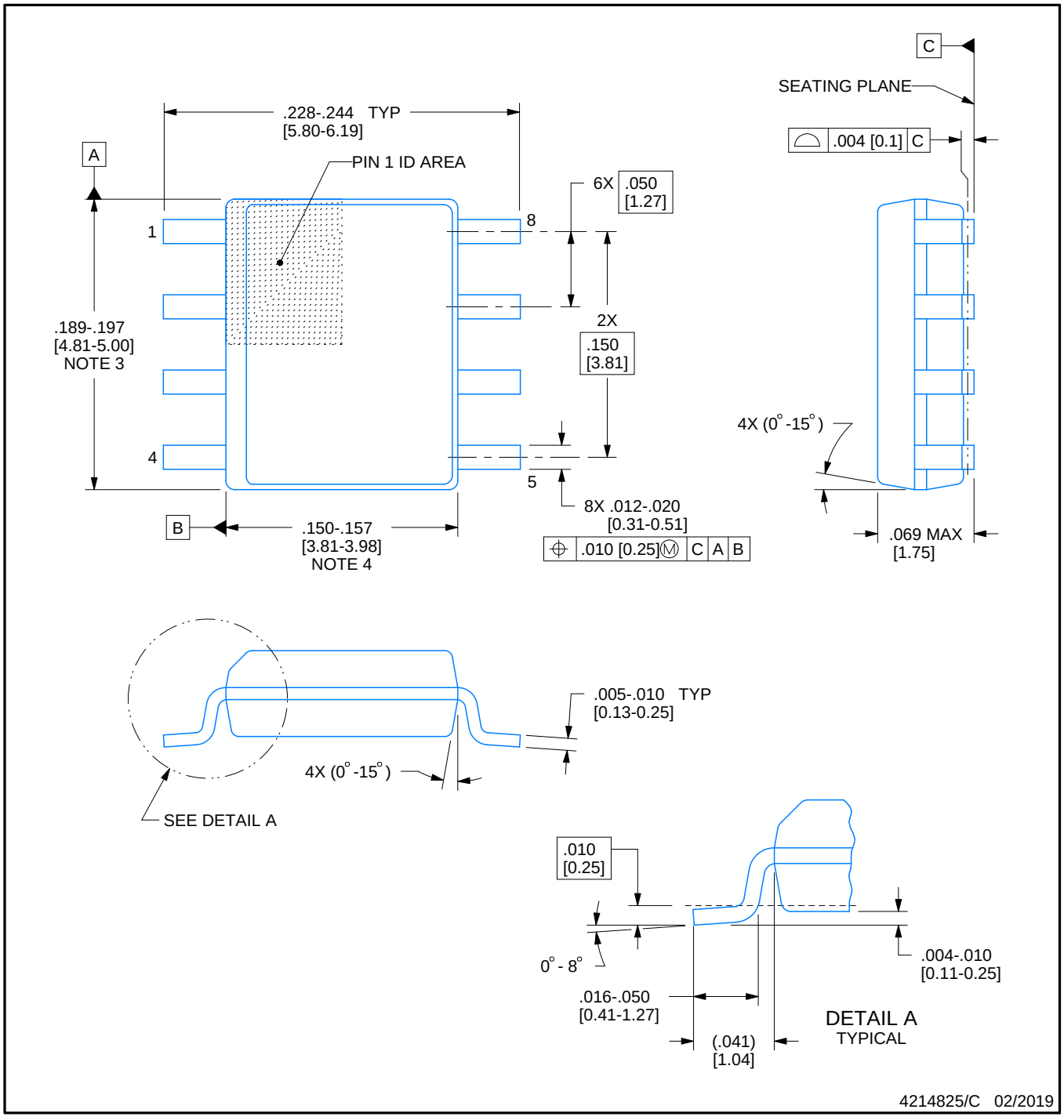


PACKAGE OUTLINE

D0008A

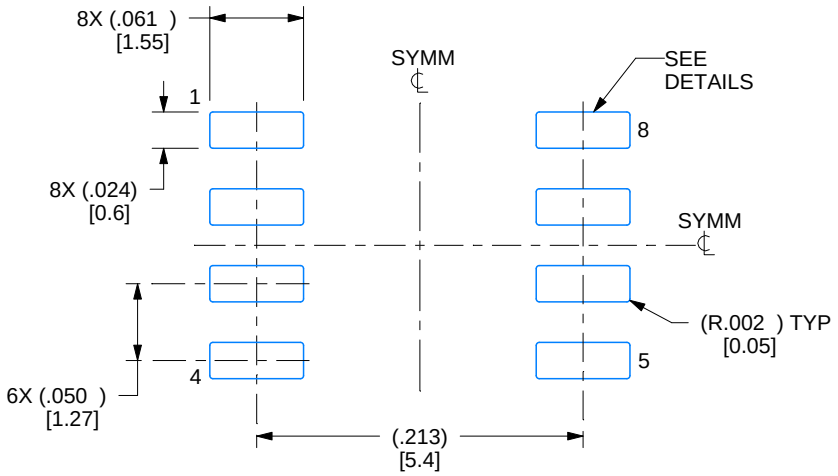
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

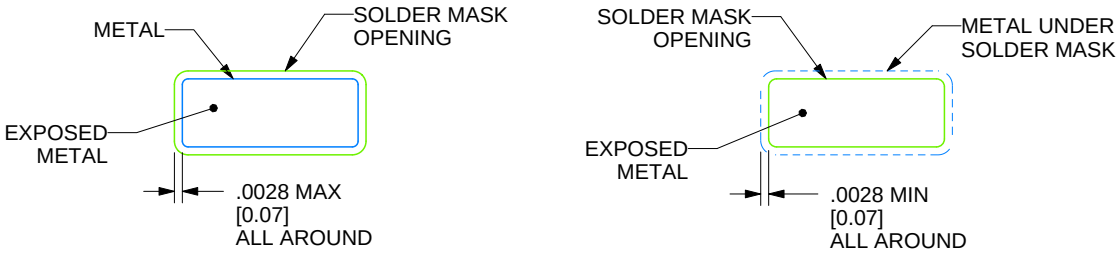


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

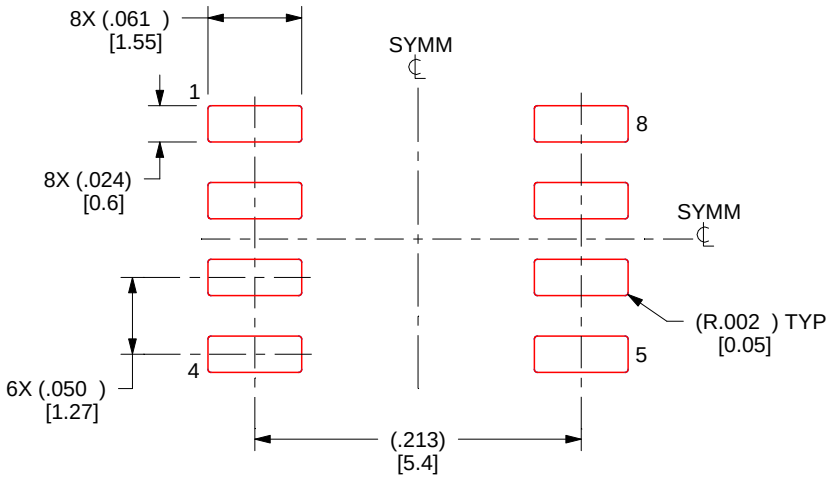
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

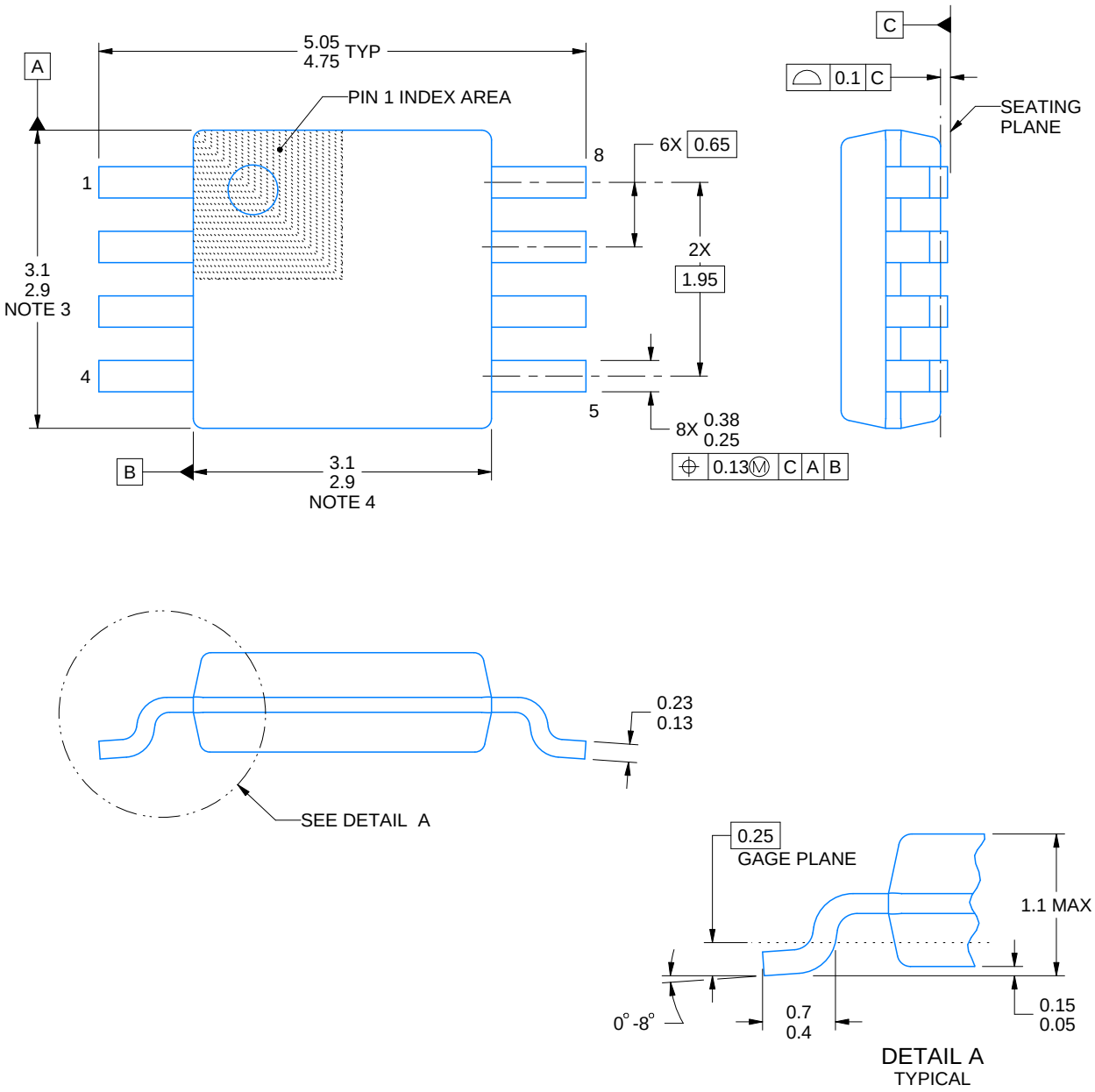
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

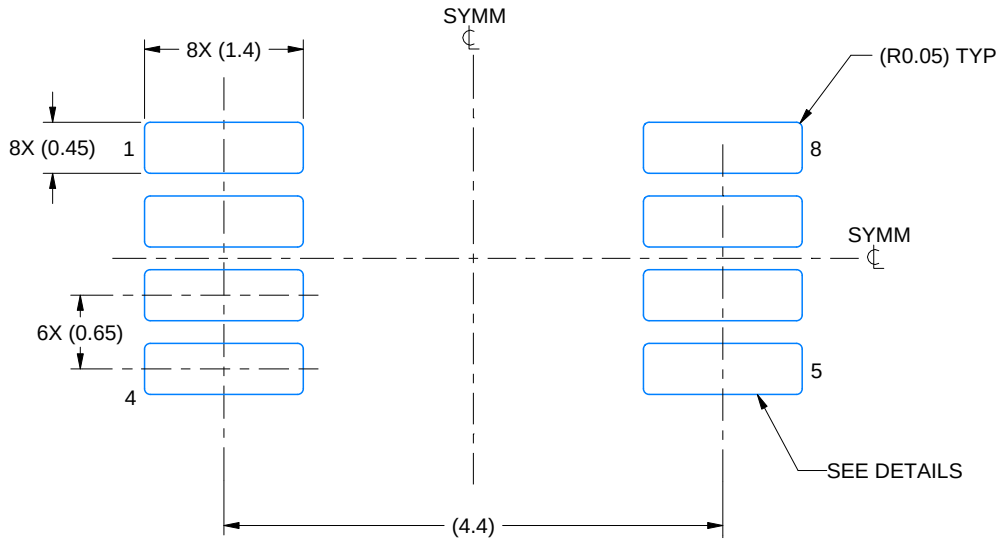
SMALL OUTLINE PACKAGE



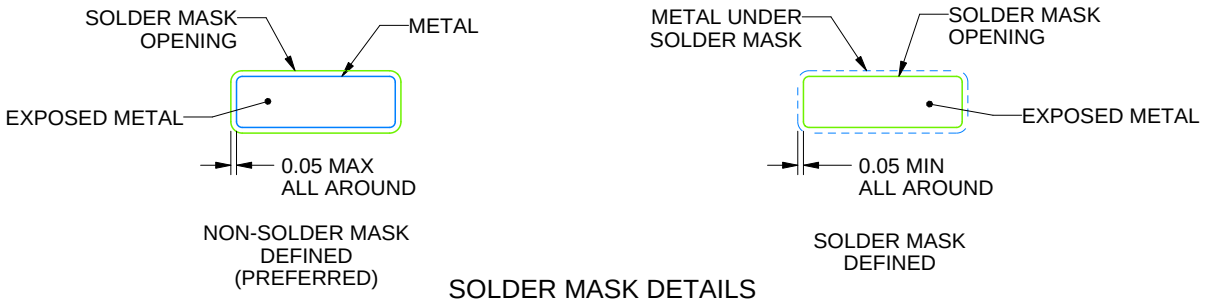
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

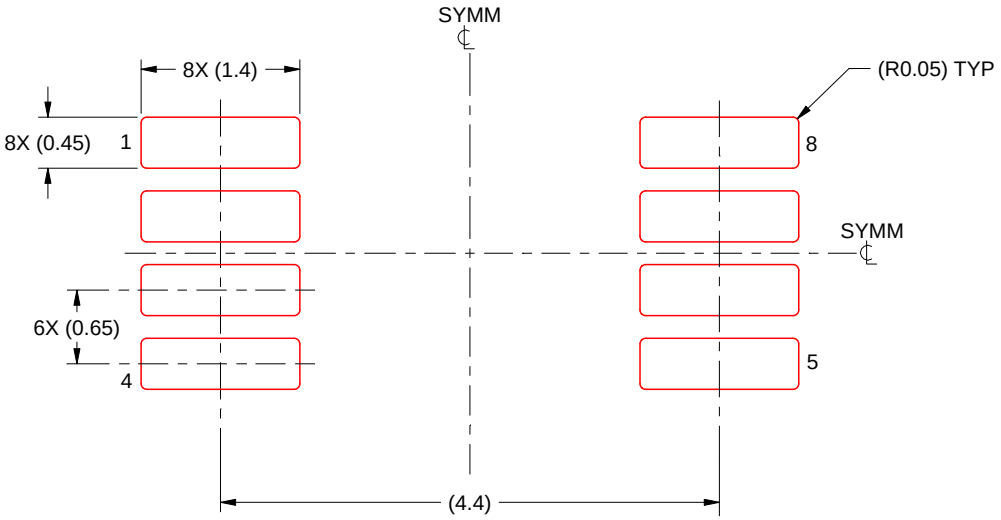


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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