

## 支持复位的 TCA9548A 低电压 8 通道 I<sup>2</sup>C 开关

### 1 特性

- 1 至 8 个双向转换开关
- 与 I<sup>2</sup>C 总线和 SMBus 兼容
- 低电平有效复位输入
- 三个地址引脚，I<sup>2</sup>C 总线最多支持八个 TCA9548A 器件
- 通过 I<sup>2</sup>C 总线进行通道选择，可任意组合
- 加电时所有开关通道取消选定
- 低 R<sub>ON</sub> 开关
- 支持在 1.8V、2.5V、3.3V 和 5V 总线间进行电压电平转换
- 加电时无干扰
- 支持热插入
- 低待机电流
- 工作电源电压范围为 1.65V 至 5.5V
- 5V 耐压输入
- 0 至 400kHz 时钟频率
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - ±2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - ±1000V 充电器件模型 (C101)

### 2 应用

- 服务器
- 路由器 ( 电信交换设备 )
- 工厂自动化
- 具有 I<sup>2</sup>C 目标地址冲突 ( 例如，多个完全一样的温度传感器 ) 的产品

### 3 说明

TCA9548A 器件配有八个可通过 I<sup>2</sup>C 总线控制的双向转换开关。SCL/SDA 上行对扩展到八个下行对，或者通道。根据可编程控制寄存器的内容，可选择任一单独 SCn/SDn 通道或者通道组合。这些下游通道可用于解决 I<sup>2</sup>C 目标地址冲突。例如，如果应用中需要八个完全相同的数字温度传感器，则每个通道 (0-7) 可以连接一个传感器。

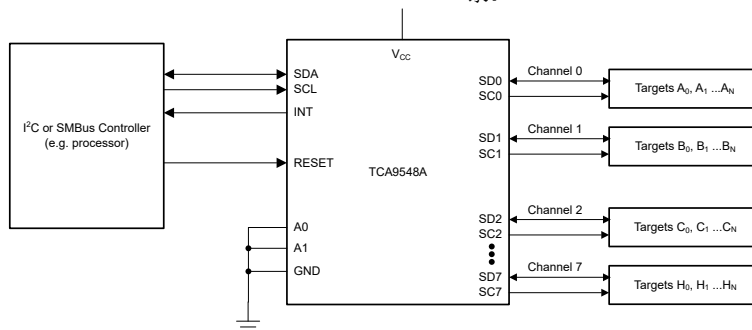
发生超时或其他不当操作时，系统控制器可通过将 **RESET** 输入置为低电平来复位 TCA9548A。同样，上电复位即可取消选中所有通道并初始化 I<sup>2</sup>C/SMBus 状态机。将 **RESET** 置为有效也可实现复位和初始化，并且无需将部件断电。这样可以在下游 I<sup>2</sup>C 总线之一卡在低电平状态时进行恢复。

由于在开关上有导通栅极，因此可使用 VCC 引脚来限制 TCA9548A 传递的最大高电压。限制最大高电压后，可以在每个对上使用不同的总线电压，从而让 1.8V、2.5V 或 3.3V 器件能够在没有任何额外保护的情况下与 5V 器件通信。对于每个通道，外部上拉电阻器将总线电压上拉至所需的电压水平。所有 I/O 引脚可耐受 5V 电压。

#### 封装信息

器件型号	封装 (1)	本体尺寸 ( 标称值 )
TCA9548A	PW ( TSSOP , 24 )	7.80mm × 4.40mm
	RGE ( VQFN , 24 )	4.00mm × 4.00mm
	DGS ( VSSOP , 24 )	6.10mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用示意图



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## 4 Pin Configuration and Functions

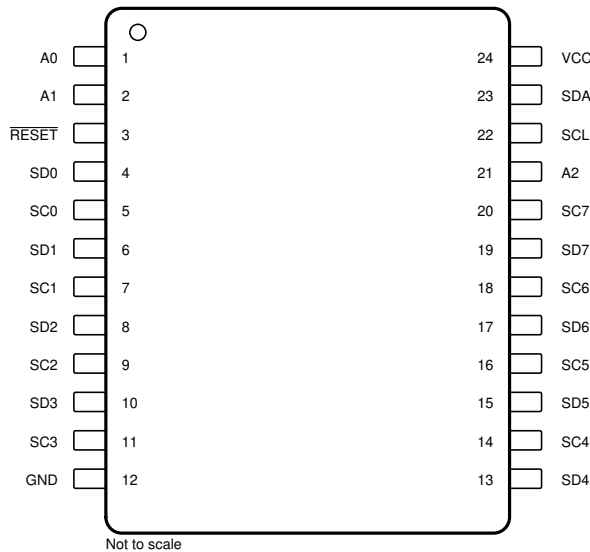


图 4-1. PW, DGS Package, 24-Pin TSSOP, VSSOP (Top View)

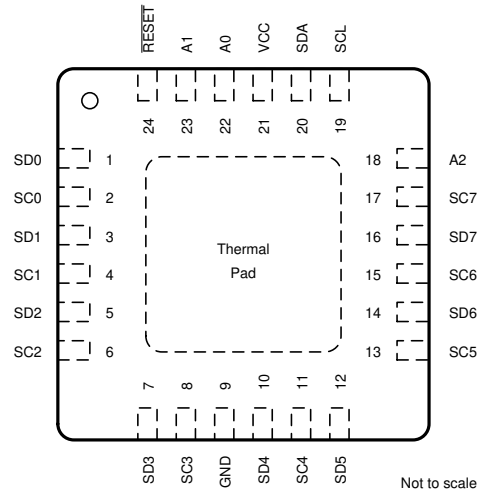


图 4-2. RGE Package, 24-Pin VQFN (Top View)

表 4-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	TSSOP, VSSOP (PW, DGS)	VQFN (RGE)		
A0	1	22	I	Address input 0. Connect directly to $V_{CC}$ or ground
A1	2	23	I	Address input 1. Connect directly to $V_{CC}$ or ground
A2	21	18	I	Address input 2. Connect directly to $V_{CC}$ or ground
GND	12	9	—	Ground
RESET	3	24	I	Active-low reset input. Connect to $V_{CC}$ or $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor, if not used
SD0	4	1	I/O	Serial data 0. Connect to $V_{DPU0}$ <sup>(1)</sup> through a pull-up resistor
SC0	5	2	I/O	Serial clock 0. Connect to $V_{DPU0}$ <sup>(1)</sup> through a pull-up resistor
SD1	6	3	I/O	Serial data 1. Connect to $V_{DPU1}$ <sup>(1)</sup> through a pull-up resistor
SC1	7	4	I/O	Serial clock 1. Connect to $V_{DPU1}$ <sup>(1)</sup> through a pull-up resistor
SD2	8	5	I/O	Serial data 2. Connect to $V_{DPU2}$ <sup>(1)</sup> through a pull-up resistor
SC2	9	6	I/O	Serial clock 2. Connect to $V_{DPU2}$ <sup>(1)</sup> through a pull-up resistor
SD3	10	7	I/O	Serial data 3. Connect to $V_{DPU3}$ <sup>(1)</sup> through a pull-up resistor
SC3	11	8	I/O	Serial clock 3. Connect to $V_{DPU3}$ <sup>(1)</sup> through a pull-up resistor
SD4	13	10	I/O	Serial data 4. Connect to $V_{DPU4}$ <sup>(1)</sup> through a pull-up resistor
SC4	14	11	I/O	Serial clock 4. Connect to $V_{DPU4}$ <sup>(1)</sup> through a pull-up resistor
SD5	15	12	I/O	Serial data 5. Connect to $V_{DPU5}$ <sup>(1)</sup> through a pull-up resistor
SC5	16	13	I/O	Serial clock 5. Connect to $V_{DPU5}$ <sup>(1)</sup> through a pull-up resistor
SD6	17	14	I/O	Serial data 6. Connect to $V_{DPU6}$ <sup>(1)</sup> through a pull-up resistor
SC6	18	15	I/O	Serial clock 6. Connect to $V_{DPU6}$ <sup>(1)</sup> through a pull-up resistor
SD7	19	16	I/O	Serial data 7. Connect to $V_{DPU7}$ <sup>(1)</sup> through a pull-up resistor
SC7	20	17	I/O	Serial clock 7. Connect to $V_{DPU7}$ <sup>(1)</sup> through a pull-up resistor
SCL	22	19	I/O	Serial clock bus. Connect to $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor
SDA	23	20	I/O	Serial data bus. Connect to $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor
VCC	24	21	Power	Supply voltage

(1)  $V_{DPUX}$  is the pull-up reference voltage for the associated data line.  $V_{DPUM}$  is the controller I<sup>2</sup>C reference voltage and  $V_{DPU0}$ - $V_{DPU7}$  are the target channel reference voltages.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	- 0.5	7	V
I <sub>I</sub>	Input current	- 20	20	mA
I <sub>O</sub>	Output current	- 25		mA
I <sub>CC</sub>	Supply current	- 100	100	mA
T <sub>stg</sub>	Storage temperature	- 65	150	°C
T <sub>J</sub>	Max Junction Temperature	V <sub>CC</sub> ≤ 3.6 V		130
T <sub>J</sub>		V <sub>CC</sub> ≤ 5.5 V		90

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-40 °C ≤ T <sub>A</sub> ≤ 85 °C	1.65	5.5	V
		85 °C < T <sub>A</sub> ≤ 125 °C	1.65	3.6	
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6	V
		A2 - A0, $\overline{\text{RESET}}$	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	- 0.5	0.3 × V <sub>CC</sub>	V
		A2 - A0, $\overline{\text{RESET}}$	- 0.5	0.3 × V <sub>CC</sub>	
T <sub>A</sub>	Operating free-air temperature	3.6 V < V <sub>CC</sub> ≤ 5.5 V	- 40	85	°C
		1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V	- 40	125	

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9548A			UNIT
		PW (TSSOP)	RGE (VQFN)	DGS (VSSOP)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	57.2	86.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	62.5	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.7	34.4	47.3	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	10.9	3.8	1.5	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	62.3	34.4	47.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	15.5	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

$V_{CC} = 1.65\text{ V to }5.5\text{ V}$ , over recommended operating free-air temperature ranges supported by Recommended Operating Conditions (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{PORR}$	Power-on reset voltage, $V_{CC}$ rising	No load, $V_I = V_{CC}$ or GND <sup>(3)</sup>			1.2	1.5	V	
$V_{PORF}$	Power-on reset voltage, $V_{CC}$ falling <sup>(4)</sup>	No load, $V_I = V_{CC}$ or GND <sup>(3)</sup>		0.8	1		V	
$V_{O(sw)}$	Switch output voltage	$V_{I(sw)} = V_{CC}$ , $I_{SWout} = -100\ \mu\text{A}$	5 V		3.6		V	
			4.5 V to 5.5 V	2.6		4.5		
			3.3 V		1.9			
			3 V to 3.6 V	1.6		2.8		
			2.5 V		1.5			
			2.3 V to 2.7 V	1.1		2		
			1.8 V		1.1			
$I_{OL}$	SDA	$V_{OL} = 0.4\text{ V}$	1.65 V to 5.5 V	3	6		mA	
		$V_{OL} = 0.6\text{ V}$		6	9			
$I_I$	SCL, SDA	$V_I = V_{CC}$ or GND <sup>(3)</sup>	1.65 V to 5.5 V	-1		1	$\mu\text{A}$	
	SC7 - SC0, SD7 - SD0			-1		1		
	A2 - A0			-1		1		
	RESET			-1		1		
$I_{CC}$	Operating mode	$f_{SCL} = 400\text{ kHz}$	$V_I = V_{CC}$ or GND <sup>(3)</sup> , $I_O = 0$	5.5 V	50	80	$\mu\text{A}$	
				3.6 V	20	35		
				2.7 V	11	20		
				1.65 V	6	10		
		$f_{SCL} = 100\text{ kHz}$	$V_I = V_{CC}$ or GND <sup>(3)</sup> , $I_O = 0$	5.5 V	9	30		
				3.6 V	6	15		
				2.7 V	4	8		
				1.65 V	2	4		
	Standby mode	Low inputs	$V_I = \text{GND}^{(3)}$ , $I_O = 0$ , $-40\text{ }^\circ\text{C} \leq TA \leq 85\text{ }^\circ\text{C}$	5.5 V	0.2	2		
				3.6 V	0.1	2		
				2.7 V	0.1	1		
		High inputs		$V_I = V_{CC}$ , $I_O = 0$ , $-40\text{ }^\circ\text{C} \leq TA \leq 85\text{ }^\circ\text{C}$	5.5 V	0.2		2
					3.6 V	0.1		2
					2.7 V	0.1		1
Low and High Inputs	$V_I = V_{CC}$ or GND <sup>(3)</sup> , $I_O = 0$ , $85\text{ }^\circ\text{C} < TA \leq 125\text{ }^\circ\text{C}$	3.6 V	1		2			
		2.7 V	0.7		1.5			
		1.65 V	0.4		1			
$\Delta I_{CC}$		Supply-current change	SCL, SDA	1.65 V to 5.5 V	SCL or SDA input at 0.6 V, Other inputs at $V_{CC}$ or GND <sup>(3)</sup>		3	20
					SCL or SDA input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND <sup>(3)</sup>		3	20
$C_i$		A2 - A0	$V_I = V_{CC}$ or GND <sup>(3)</sup>	1.65 V to 5.5 V	4	5	pF	
	RESET	4			5			
	SCL	20			28			
$C_{Io(off)}$ <sup>(5)</sup>	SDA	$V_I = V_{CC}$ or GND <sup>(3)</sup> , Switch OFF	1.65 V to 5.5 V	20	28	pF		
	SC7 - SC0, SD7 - SD0			5.5	7.5			

$V_{CC} = 1.65\text{ V to }5.5\text{ V}$ , over recommended operating free-air temperature ranges supported by Recommended Operating Conditions (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$R_{ON}$	Switch-on resistance	$V_O = 0.4\text{ V}, I_O = 15\text{ mA}$	4.5 V to 5.5 V	4	10	20	$\Omega$
			3 V to 3.6 V	5	12	30	
		$V_O = 0.4\text{ V}, I_O = 10\text{ mA}$	2.3 V to 2.7 V	7	15	45	
			1.65 V to 1.95 V	10	25	70	

- (1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges
- (2) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V  $V_{CC}$ ),  $T_A = 25^\circ\text{C}$
- (3)  $\overline{\text{RESET}} = V_{CC}$  (held high) when all other input voltages,  $V_I = \text{GND}$ .
- (4) The power-on reset circuit resets the I<sup>2</sup>C bus logic with  $V_{CC} < V_{PORF}$
- (5)  $C_{iO(ON)}$  depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

## 5.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [图 6-1](#))

			MIN	MAX	UNIT
<b>STANDARD MODE</b>					
$f_{scl}$	I <sup>2</sup> C clock frequency		0	100	kHz
$t_{sch}$	I <sup>2</sup> C clock high time		4		$\mu\text{ s}$
$t_{scl}$	I <sup>2</sup> C clock low time		4.7		$\mu\text{ s}$
$t_{sp}$	I <sup>2</sup> C spike time			50	ns
$t_{sds}$	I <sup>2</sup> C serial-data setup time		250		ns
$t_{sdh}$	I <sup>2</sup> C serial-data hold time		0 <sup>(1)</sup>		$\mu\text{ s}$
$t_{icr}$	I <sup>2</sup> C input rise time			1000	ns
$t_{icf}$	I <sup>2</sup> C input fall time			300	ns
$t_{ocf}$	I <sup>2</sup> C output (SDn) fall time (10-pF to 400-pF bus)			300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between stop and start		4.7		$\mu\text{ s}$
$t_{sts}$	I <sup>2</sup> C start or repeated start condition setup		4.7		$\mu\text{ s}$
$t_{sth}$	I <sup>2</sup> C start or repeated start condition hold		4		$\mu\text{ s}$
$t_{sps}$	I <sup>2</sup> C stop condition setup		4		$\mu\text{ s}$
$t_{vdL(Data)}$	Valid-data time (high to low) <sup>(2)</sup>	SCL low to SDA output low valid		1	$\mu\text{ s}$
$t_{vdH(Data)}$	Valid-data time (low to high) <sup>(2)</sup>	SCL low to SDA output high valid		0.6	$\mu\text{ s}$
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	$\mu\text{ s}$
$C_b$	I <sup>2</sup> C bus capacitive load			400	pF
<b>FAST MODE</b>					
$f_{scl}$	I <sup>2</sup> C clock frequency		0	400	kHz
$t_{sch}$	I <sup>2</sup> C clock high time		0.6		$\mu\text{ s}$
$t_{scl}$	I <sup>2</sup> C clock low time		1.3		$\mu\text{ s}$
$t_{sp}$	I <sup>2</sup> C spike time			50	ns
$t_{sds}$	I <sup>2</sup> C serial-data setup time		100		ns
$t_{sdh}$	I <sup>2</sup> C serial-data hold time		0 <sup>(1)</sup>		$\mu\text{ s}$
$t_{icr}$	I <sup>2</sup> C input rise time		$20 + 0.1C_b$ <sup>(3)</sup>	300	ns
$t_{icf}$	I <sup>2</sup> C input fall time		$20 + 0.1C_b$ <sup>(3)</sup>	300	ns
$t_{ocf}$	I <sup>2</sup> C output (SDn) fall time (10-pF to 400-pF bus)		$20 + 0.1C_b$ <sup>(3)</sup>	300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between stop and start		1.3		$\mu\text{ s}$
$t_{sts}$	I <sup>2</sup> C start or repeated start condition setup		0.6		$\mu\text{ s}$
$t_{sth}$	I <sup>2</sup> C start or repeated start condition hold		0.6		$\mu\text{ s}$
$t_{sps}$	I <sup>2</sup> C stop condition setup		0.6		$\mu\text{ s}$
$t_{vdL(Data)}$	Valid-data time (high to low) <sup>(2)</sup>	SCL low to SDA output low valid		1	$\mu\text{ s}$
$t_{vdH(Data)}$	Valid-data time (low to high) <sup>(2)</sup>	SCL low to SDA output high valid		0.6	$\mu\text{ s}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

			MIN	MAX	UNIT
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	$\mu s$
$C_b$	$I^2C$ bus capacitive load			400	pF

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IH}$  min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
- (2) Data taken using a 1-k $\Omega$  pull-up resistor and 50-pF load.
- (3)  $C_b$  = total bus capacitance of one bus line in pF.

## 5.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{W(L)}$	Pulse duration, $\overline{RESET}$ low	6		ns
$t_{REC(STA)}$	Recovery time from $\overline{RESET}$ to start	0		ns

## 5.8 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see 图 6-1)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{(1)}$	Propagation delay time	$R_{ON} = 20 \Omega, C_L = 15$ pF	SDA or SCL	SDn or SCn	0.3		ns
		$R_{ON} = 20 \Omega, C_L = 50$ pF			1		
$t_{rst}^{(2)}$	$\overline{RESET}$ time (SDA clear)		$\overline{RESET}$	SDA	500		ns

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{rst}$  is the propagation delay measured from the time the  $\overline{RESET}$  pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of  $t_{WL}$ .



### 5.9 Typical Characteristics

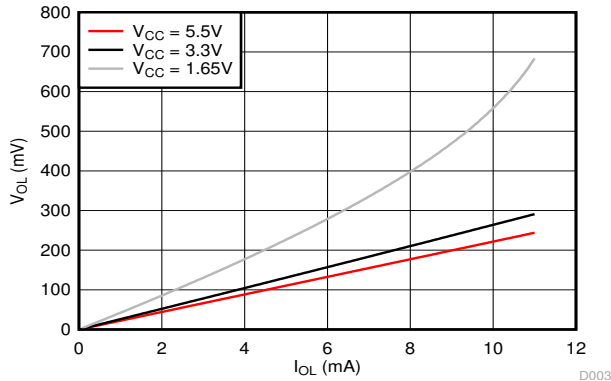


图 5-1. SDA Output Low Voltage ( $V_{OL}$ ) vs Load Current ( $I_{OL}$ ) at Three  $V_{CC}$  Levels ( $T_A = 25\text{ }^\circ\text{C}$ )

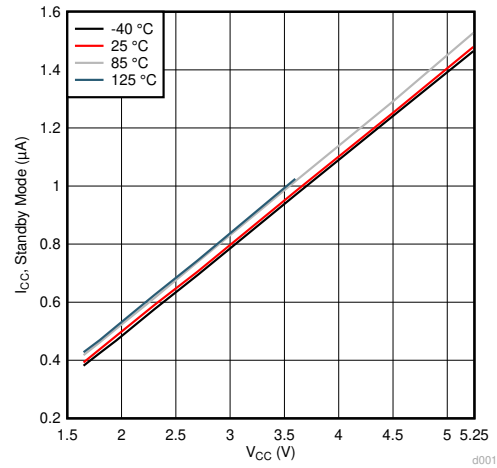


图 5-2. Standby Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ ) at Four Temperature Points

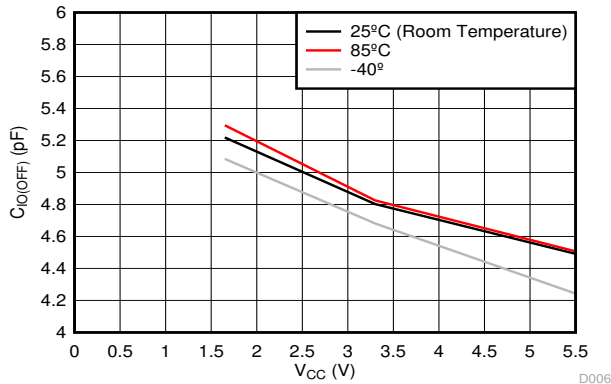


图 5-3. Target Channel (SCn/SDn) Capacitance ( $C_{IO(OFF)}$ ) vs Supply Voltage ( $V_{CC}$ ) at Four Temperature Points

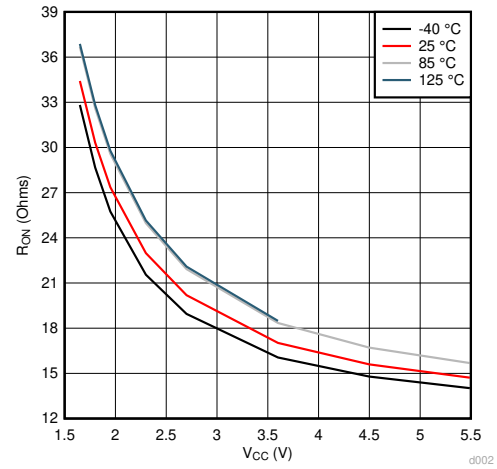
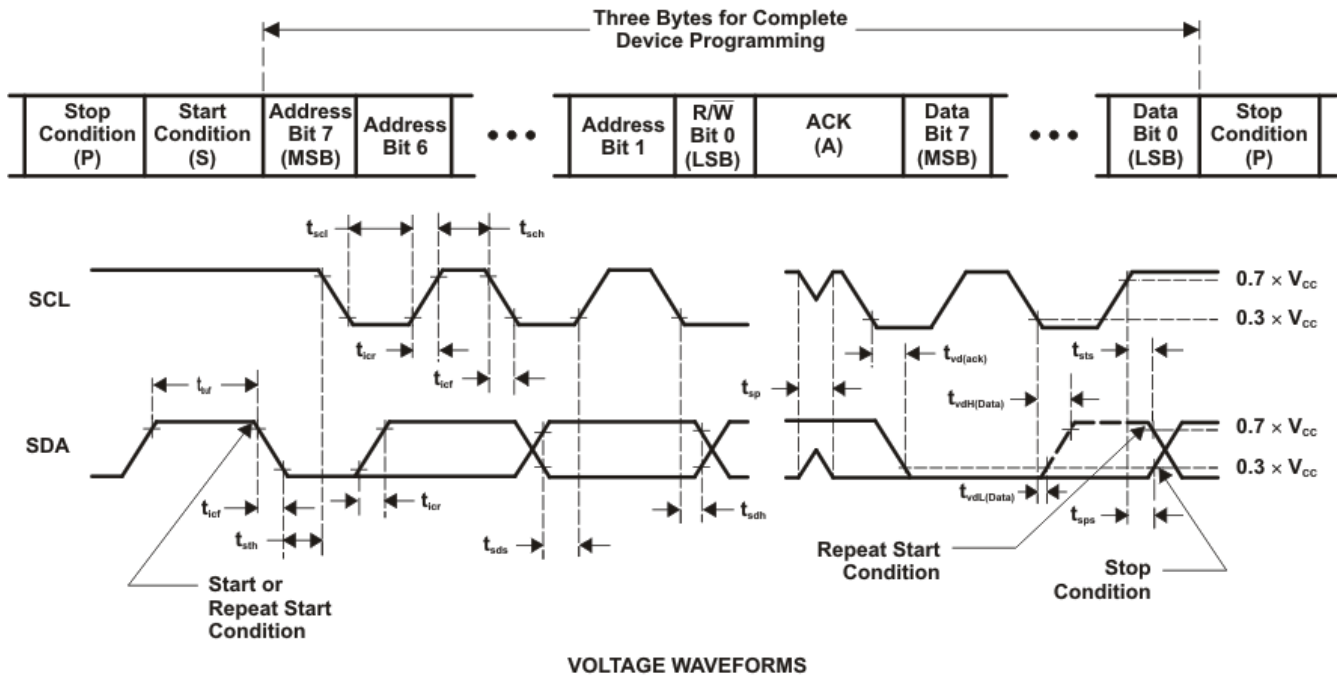
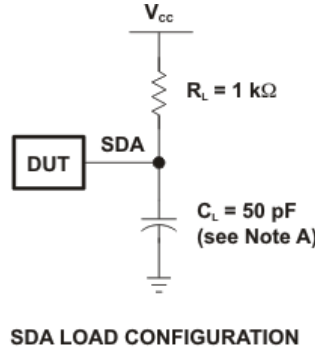


图 5-4. On-Resistance ( $R_{ON}$ ) vs Supply Voltage ( $V_{CC}$ ) at Four Temperature Points

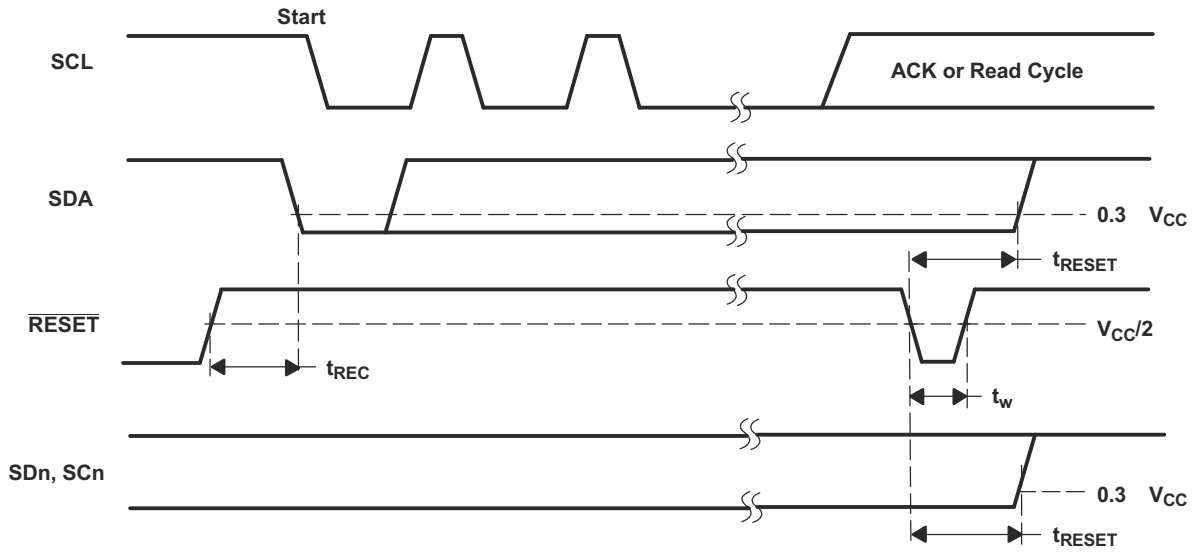
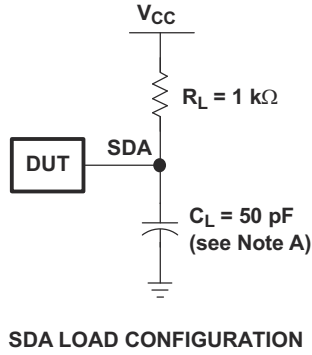
## 6 Parameter Measurement Information



BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30 \text{ ns}$ .
- C. Not all parameters and waveforms are applicable to all devices.

**图 6-1. I<sup>2</sup>C Load Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r/t_f \leq 30\text{ ns}$ .
- C. I/Os are configured as inputs.
- D. Not all parameters and waveforms are applicable to all devices.

**图 6-2. Reset Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

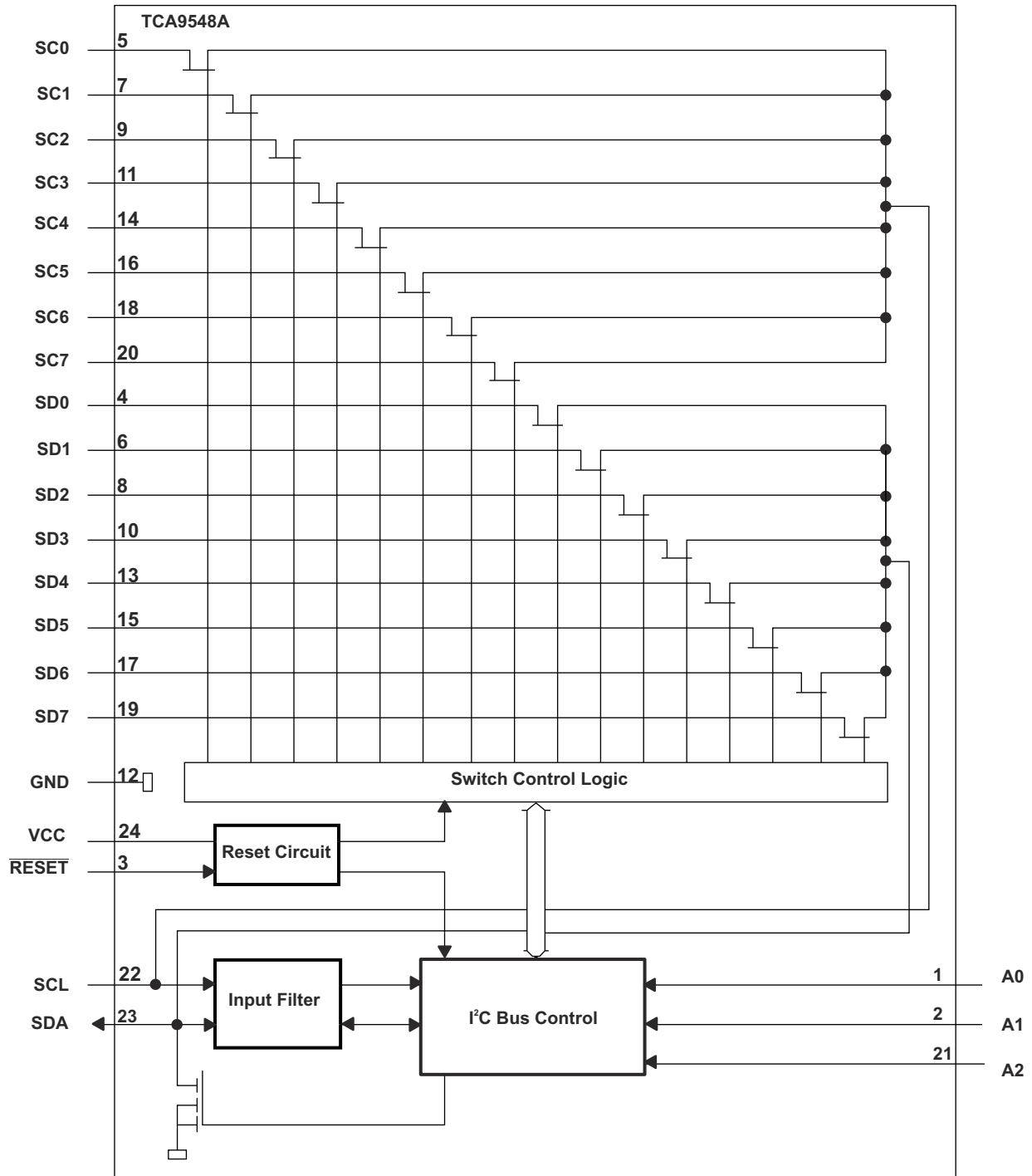
The TCA9548A is an 8-channel, bidirectional translating I<sup>2</sup>C switch. The controller SCL/SDA signal pair is directed to eight channels of target devices, SC0/SD0-SC7/SD7. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the TCA9548A to recover must one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply,  $V_{CC}$ , also known as a power-on reset (POR). Both the  $\overline{\text{RESET}}$  function and a POR cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C controller device that is switched to communicate with multiple I<sup>2</sup>C targets. After the successful acknowledgment of the target address (hardware selectable by A0, A1, and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The TCA9548A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the controller and each target channel.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

The TCA9548A is an 8-channel, bidirectional translating switch for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9548A features I<sup>2</sup>C control using a single 8-bit control register in which each bit controls the enabling and disabling of one of the corresponding 8 switch channels for I<sup>2</sup>C data flow. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the TCA9548A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that

communication on the I<sup>2</sup>C bus enters a fault state, the TCA9548A can be reset to resume normal operation using the RESET pin feature or by a power-on reset which results from cycling power to the device.

## 7.4 Device Functional Modes

### 7.4.1 RESET Input

The RESET input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{WL}$ , the TCA9548A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The RESET input must be connected to V<sub>CC</sub> through a pull-up resistor.

### 7.4.2 Power-On Reset

When power is applied to the VCC pin, an internal power-on reset holds the TCA9548A in a reset condition until V<sub>CC</sub> has reached V<sub>PORR</sub>. At this point, the reset condition is released, and the TCA9548A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V<sub>CC</sub> must be lowered below V<sub>PORF</sub> to reset the device.

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C Interface

The TCA9548A has a standard bidirectional I<sup>2</sup>C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I<sup>2</sup>C bus has a specific device address to differentiate between other target devices that are on the same I<sup>2</sup>C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V<sub>CC</sub> through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. (For further details, see the [I<sup>2</sup>C Pull-up Resistor Calculation](#) application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (See [图 7-1](#) and [图 7-2](#)).

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
  - Controller-transmitter sends a START condition and addresses the target-receiver.
  - Controller-transmitter sends data to target-receiver.
  - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
  - Controller-receiver sends a START condition and addresses the target-transmitter.
  - Controller-receiver sends the requested register to read to target-transmitter.
  - Controller-receiver receives data from the target-transmitter.

- Controller-receiver terminates the transfer with a STOP condition.

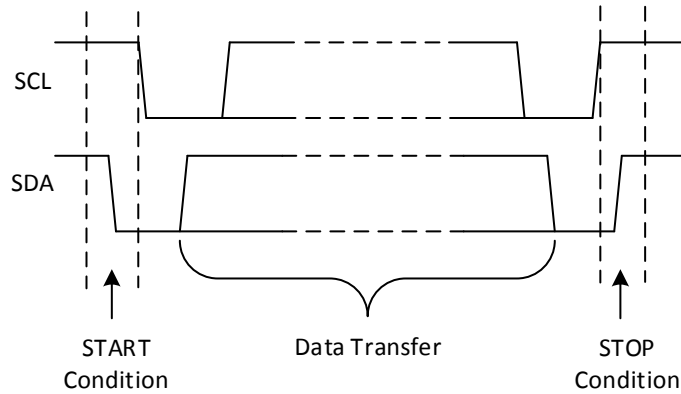


图 7-1. Definition of Start and Stop Conditions

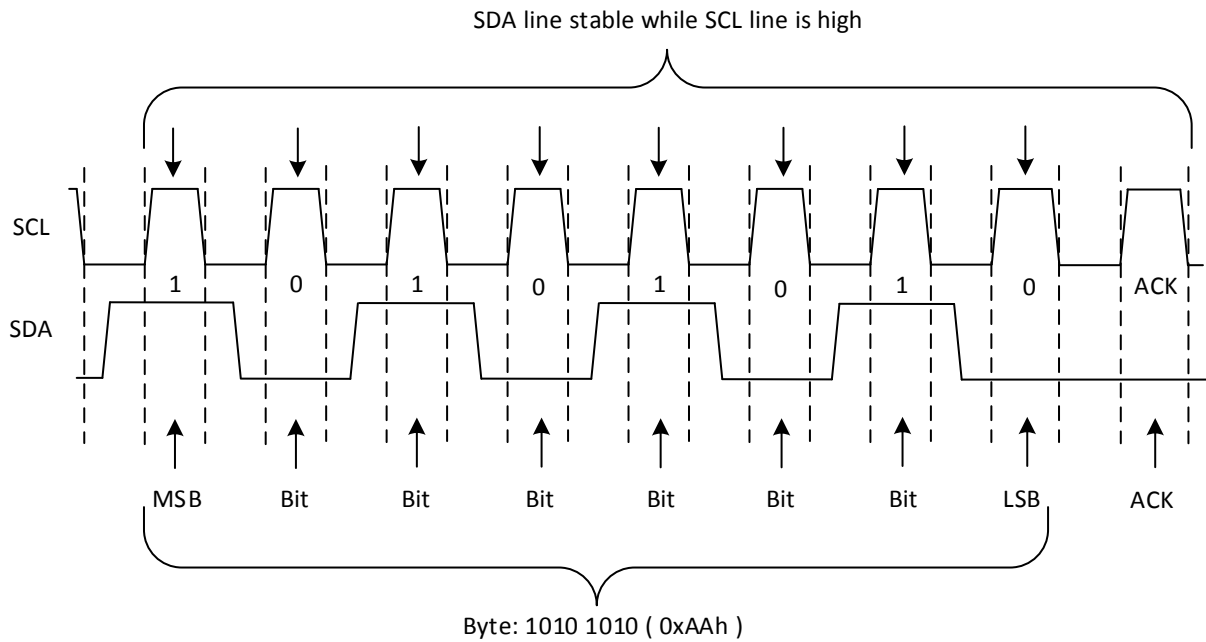


图 7-2. Bit Transfer

### 7.5.2 Device Address

图 7-3 shows the address byte of the TCA9548A.

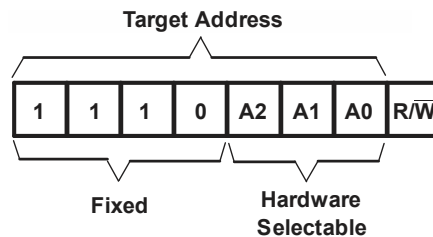


图 7-3. TCA9548A Address

The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

表 7-1 shows the TCA9548A address reference.

表 7-1. Address Reference

INPUTS			I <sup>2</sup> C BUS TARGETADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)



### 7.5.3 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

While it is common to have registers in I<sup>2</sup>C targets, note that not all target devices have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the target address, instead of addressing a register. The TCA9548A is example of a single-register device, which is controlled via I<sup>2</sup>C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

#### 7.5.3.1 Writes

To write on the I<sup>2</sup>C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/  $\bar{W}$  bit) set to 0, which signifies a write. The target acknowledges, letting the controller know it is ready. After this, the controller starts sending the control register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what is in the register.

图 7-4 shows an example of writing a single byte to a target register.

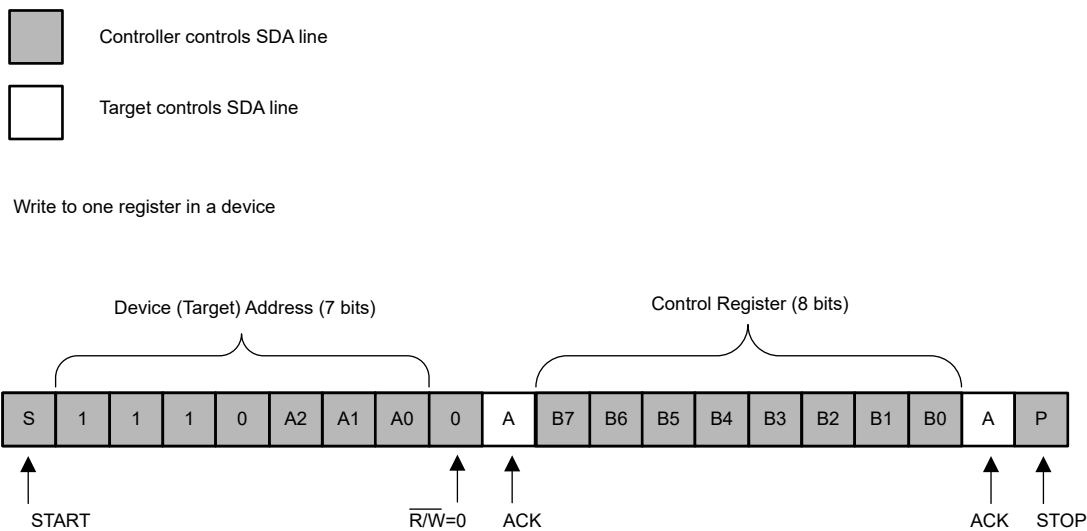


图 7-4. Write to Register

#### 7.5.3.2 Reads

Reading from a target is very similar to writing, but the controller sends a START condition, followed by the target address with the R/  $\bar{W}$  bit set to 1 (signifying a read). The target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. Once the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

图 7-5 shows an example of reading a single byte from a target register.

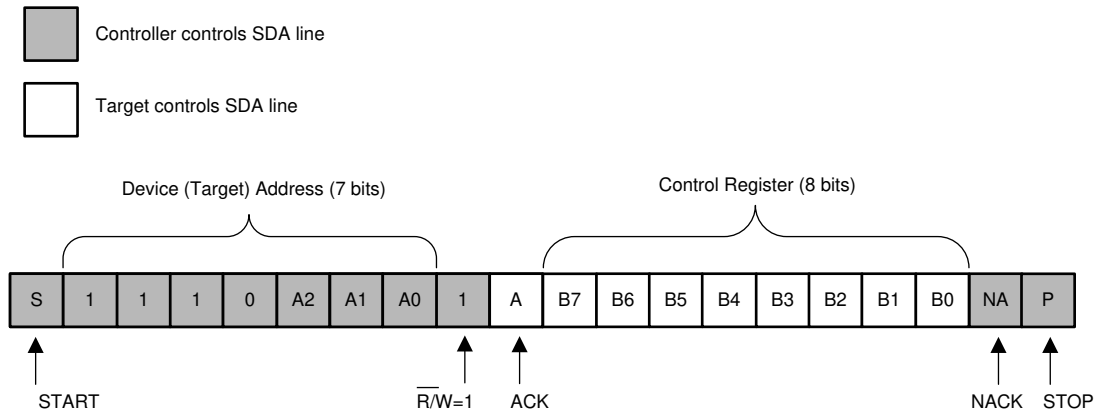


图 7-5. Read from Control Register

### 7.5.4 Control Register

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the TCA9548A (see 图 7-6). This register can be written and read via the I<sup>2</sup>C bus. Each bit in the command byte corresponds to a SC<sub>n</sub>/SD<sub>n</sub> channel and a high (or 1) selects this channel. Multiple SC<sub>n</sub>/SD<sub>n</sub> channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This makes sure that all SC<sub>n</sub>/SD<sub>n</sub> lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the TCA9548A, it saves the last byte received.

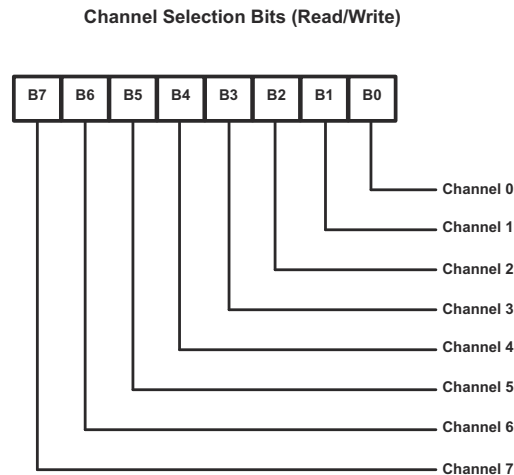


图 7-6. Control Register

表 7-2 shows the TCA9548A Command Byte Definition.

**表 7-2. Command Byte Definition**

CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	X	X	0	Channel 2 disabled
							1	Channel 2 enabled
X	X	X	X	X	X	X	0	Channel 3 disabled
							1	Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

### 7.5.5 RESET Input

The **RESET** input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{WL}$ , the TCA9548A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The **RESET** input must be connected to V<sub>CC</sub> through a pull-up resistor.

### 7.5.6 Power-On Reset

When power (from 0 V) is applied to V<sub>CC</sub>, an internal power-on reset holds the TCA9548A in a reset condition until V<sub>CC</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the TCA9548A registers and I<sup>2</sup>C state machine initialize to their default states. After that, V<sub>CC</sub> must be lowered to below V<sub>POR</sub> and then back up to the operating voltage for a power-reset cycle.

## 8 Application and Implementation

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### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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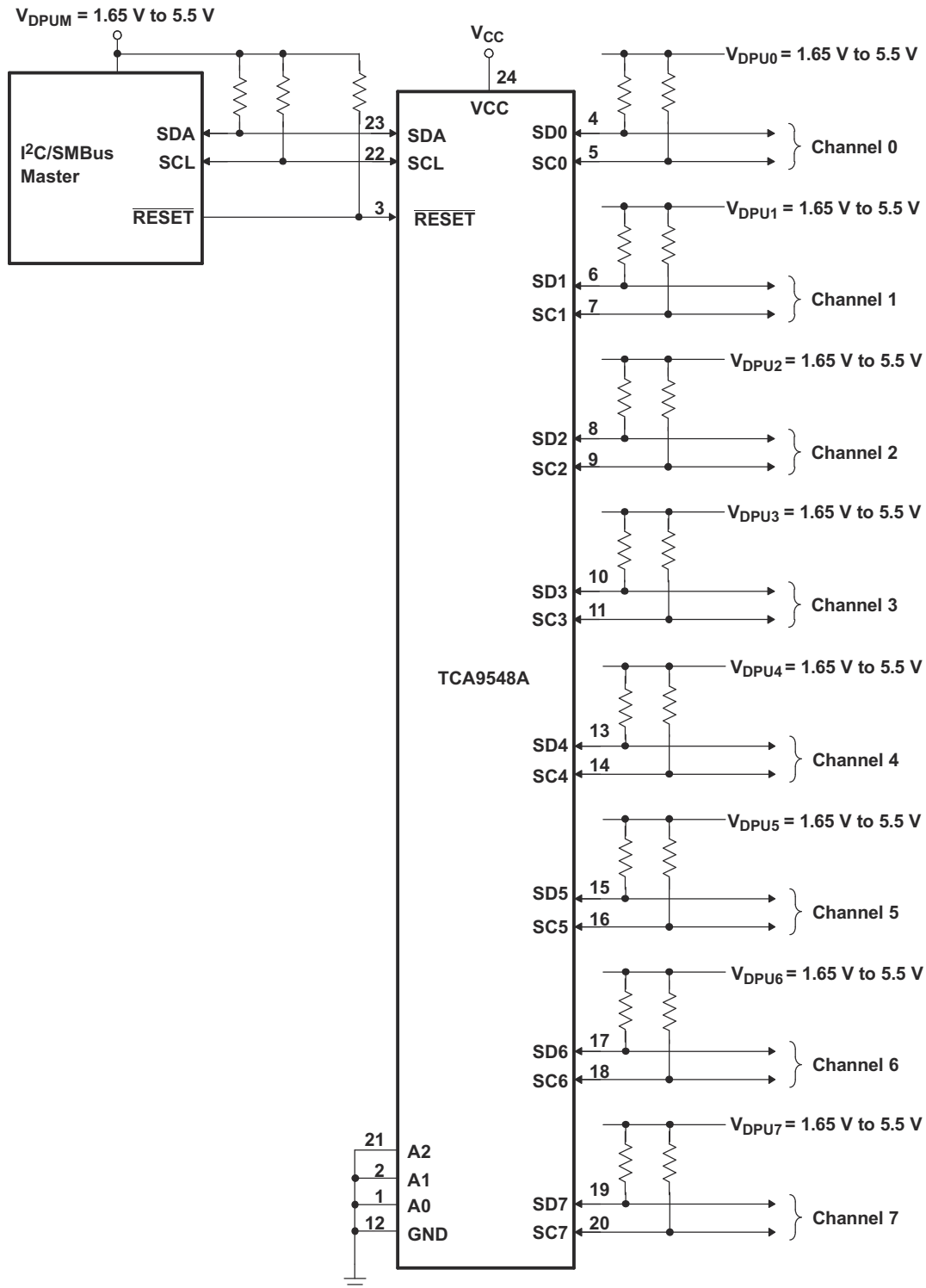
### 8.1 Application Information

Applications of the TCA9548A contain an I<sup>2</sup>C (or SMBus) controller device and up to eight I<sup>2</sup>C target devices. The downstream channels are used to resolve I<sup>2</sup>C target address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7. When the temperature at a specific location is read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I<sup>2</sup>C controller can move on and read the next channel.

In an application where the I<sup>2</sup>C bus contains many additional target devices that do not result in I<sup>2</sup>C target address conflicts, these target devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (see the [Design Requirements](#) section and [Detailed Design Procedure](#) section).

### 8.2 Typical Application

图 8-1 shows an application in which the TCA9548A can be used.



Pin numbers shown are for the PW package.

图 8-1. Typical Application Schematic

### 8.2.1 Design Requirements

A typical application of the TCA9548A contains one or more data pull-up voltages,  $V_{DPUX}$ , one for the controller device ( $V_{DPUM}$ ) and one for each of the selectable target channels ( $V_{DPU0} - V_{DPU7}$ ). In the event where the controller device and all target devices operate at the same voltage, then  $V_{DPUM} = V_{DPUX} = V_{CC}$ . In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate  $V_{CC}$  voltage.

The A0, A1, and A2 pins are hardware selectable to control the target address of the TCA9548A. These pins may be tied directly to GND or  $V_{CC}$  in the application.

If multiple target channels are activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the controller side is the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the TCA9548A are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

图 8-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the 节 5.5 table). In order for the TCA9548A to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in 图 8-2,  $V_{pass(max)}$  is 2.7 V when the TCA9548A supply voltage is 4 V or lower, so the TCA9548A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see 图 8-1).

### 8.2.2 Detailed Design Procedure

Once all the targets are assigned to the appropriate target channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of  $V_{DPUX}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in 方程式 1:

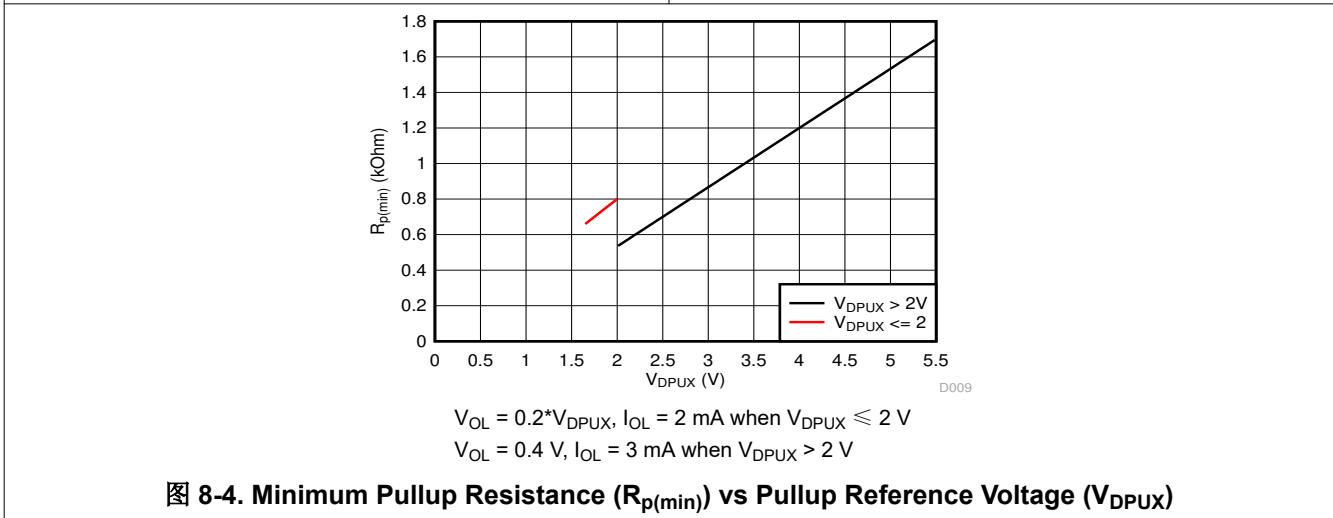
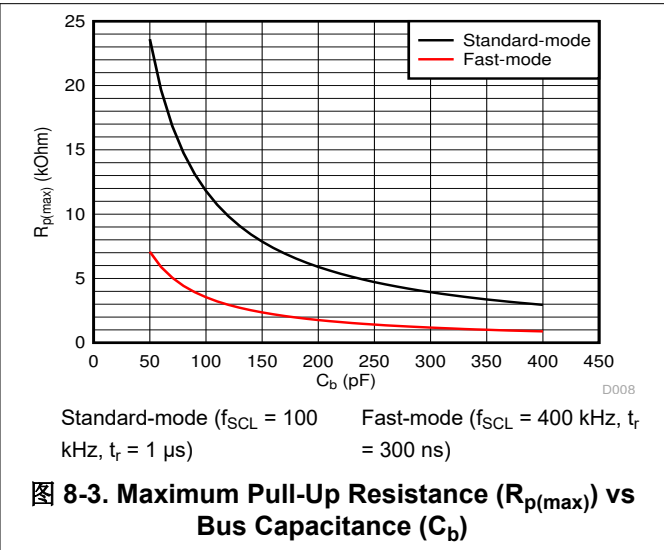
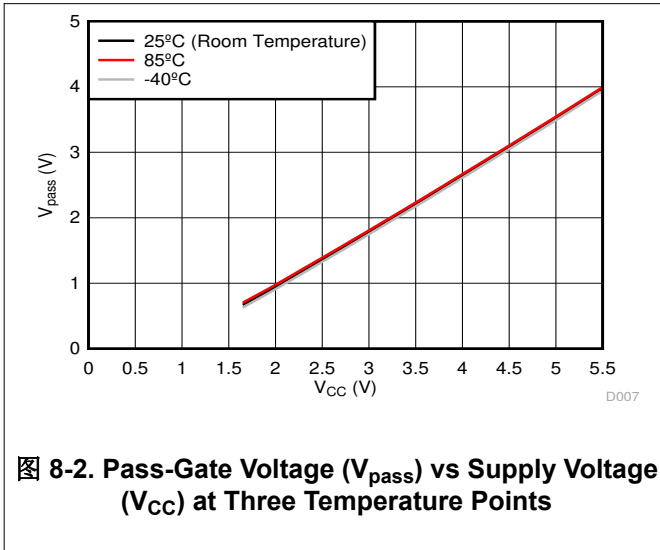
$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in 方程式 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9548A,  $C_{io(OFF)}$ , the capacitance of wires, connections and traces, and the capacitance of each individual target on a given channel. If multiple channels are activated simultaneously, each of the targets on all channels contribute to total bus capacitance.

### 8.2.3 Application Curves



### 8.3 Power Supply Recommendations

The operating power-supply voltage range of the TCA9548A is 1.65 V to 5.5 V applied at the VCC pin. When the TCA9548A is powered on for the first time or anytime, the device must be reset by cycling the power supply. The power-on reset requirements must be followed to make sure the I<sup>2</sup>C bus logic is initialized properly.

#### 8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9548A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in [图 8-5](#).

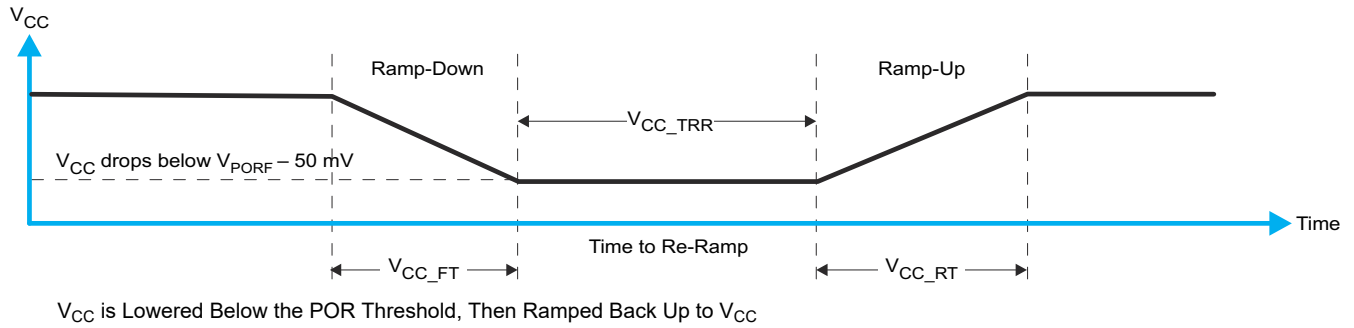


图 8-5. Power-On Reset Waveform

表 8-1 specifies the performance of the power-on reset feature for PCA9548A for both types of power-on reset.

表 8-1. Recommended Supply Sequencing and Ramp Rates <sup>(1)</sup>

PARAMETER			MIN	MAX	UNIT
$V_{CC\_FT}$	Fall time	See 图 8-5	1	100	ms
$V_{CC\_RT}$	Rise time	See 图 8-5	0.1	100	ms
$V_{CC\_TRR}$	Time to re-ramp (when $V_{CC}$ drops below $V_{PORF(min)} - 50$ mV or when $V_{CC}$ drops to GND)	See 图 8-5	40		$\mu$ s
$V_{CC\_GH}$	Level that $V_{CC}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW} = 1$ $\mu$ s	See 图 8-6		1.2	V
$V_{CC\_GW}$	Glitch width that does not cause a functional disruption when $V_{CC\_GH} = 0.5 \times V_{CC}$	See 图 8-6		10	$\mu$ s

(1) All supply sequencing and ramp rate values are measured at  $T_A = 25^\circ\text{C}$

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 图 8-6 and 表 8-1 provide more information on how to measure these specifications.

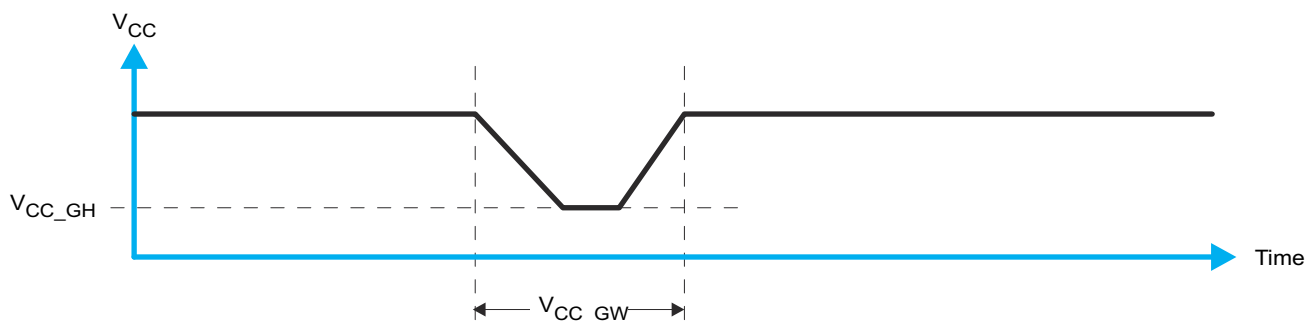


图 8-6. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. 图 8-7 and 表 8-1 provide more details on this specification.



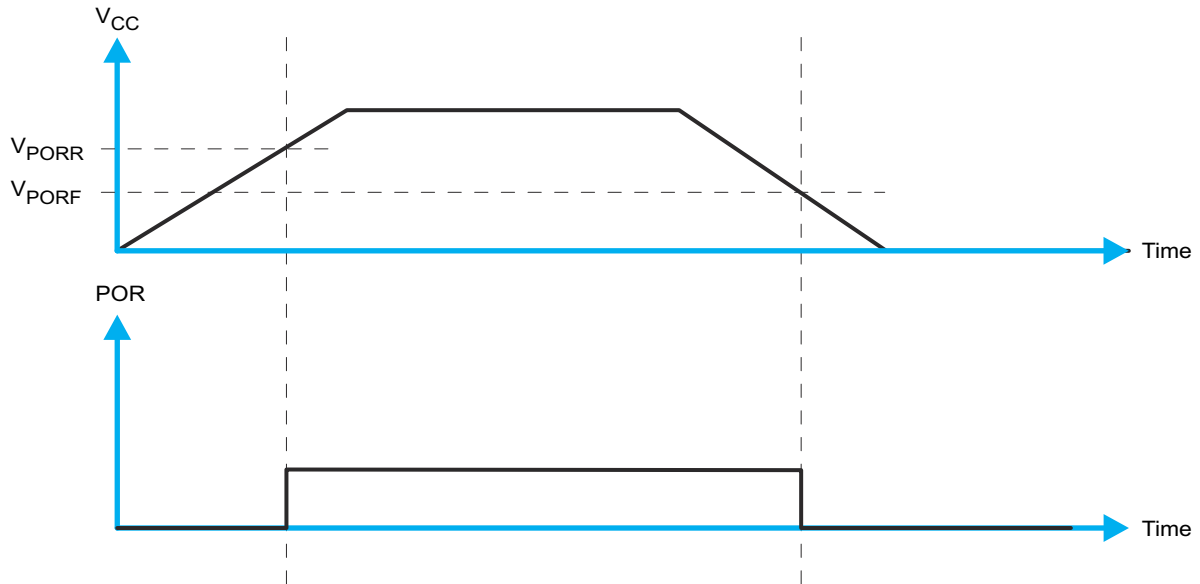


图 8-7.  $V_{POR}$

## 8.4 Layout

### 8.4.1 Layout Guidelines

For PCB layout of the TCA9548A, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all  $V_{DPUX}$  voltages and  $V_{CC}$  could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required,  $V_{DPU0}$  and  $V_{DPU0} - V_{DPU7}$ , may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SC<sub>n</sub> and SD<sub>n</sub>) must be as short as possible and the widths of the traces must also be minimized (for example, 5-10 mils depending on copper weight).

### 8.4.2 Layout Example

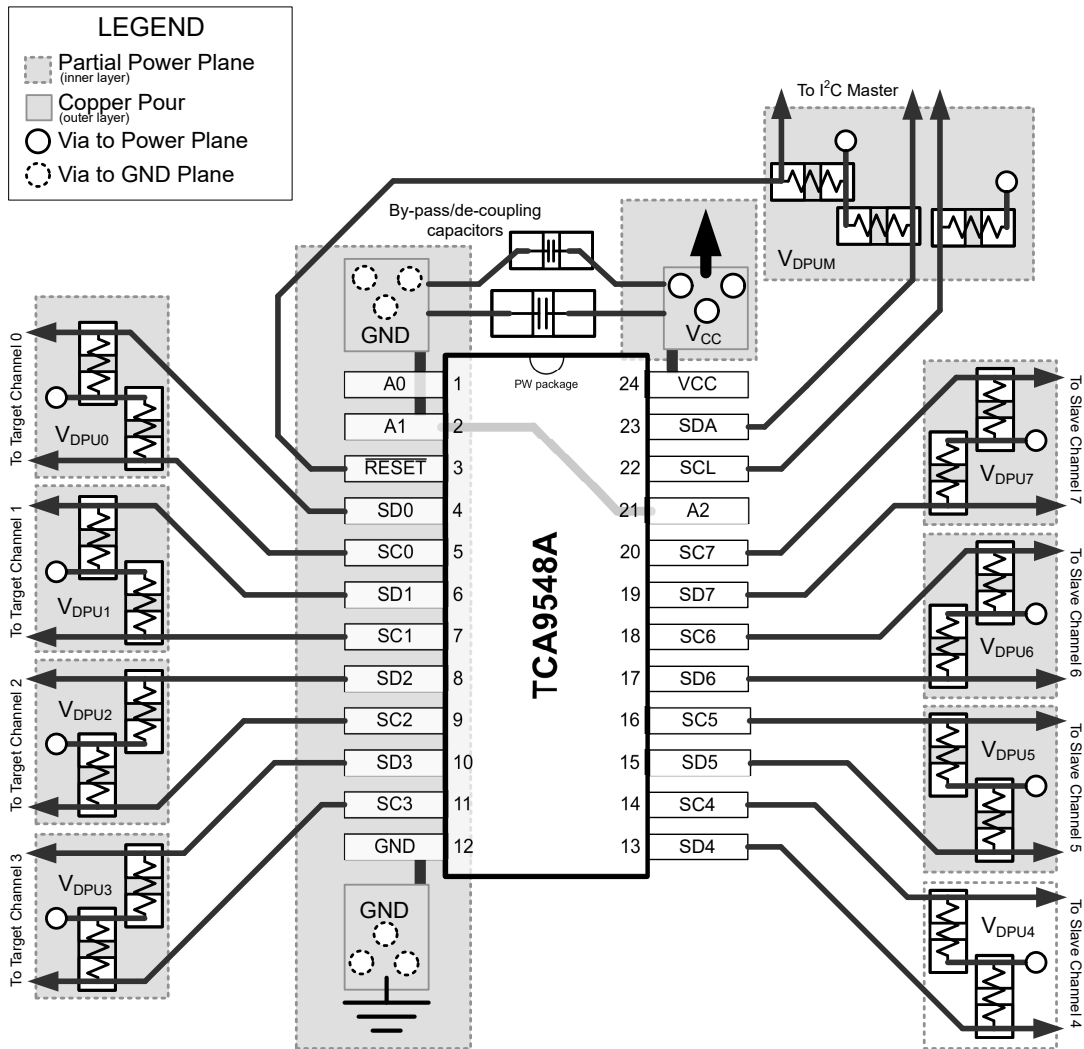


图 8-8. Layout Schematic

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [Choosing the Correct I2C Device for New Designs](#)
- [TCA9548AEVM User's Guide](#)

### 9.2 接收文档更新通知

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### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 商标

TI E2E™ is a trademark of Texas Instruments.

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### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (October 2019) to Revision H (September 2024)	Page
• 将提到的旧术语实例更改为控制器和目标.....	1
• 添加了 DGS 封装.....	1
<hr/>	
Changes from Revision F (November 2016) to Revision G (October 2019)	Page
• Changed the appearance of the PW package and the RGE package images .....	3
• Updated typical characteristic curves for 125C.....	9
• Changed $R_L = 1 \text{ kW To: } R_L = 1 \text{ K } \Omega$ in <a href="#">图 6-2</a> .....	10

<b>Changes from Revision E (October 2015) to Revision F (November 2016)</b>	<b>Page</b>
• 更新了说明部分.....	1
• 添加了新的可订购器件型号 , TCA9548AMRGER.....	1

<b>Changes from Revision D (January 2015) to Revision E (October 2015)</b>	<b>Page</b>
• Updated <i>Pin Functions</i> table. ....	3
• Added new I <sup>2</sup> C Sections and read/write description .....	17

<b>Changes from Revision C (November 2013) to Revision D (January 2015)</b>	<b>Page</b>
• 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Updated Typical Application schematic. ....	20

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TCA9548ADGSR</a>	Active	Production	VSSOP (DGS)   24	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	548A
TCA9548ADGSR.B	Active	Production	VSSOP (DGS)   24	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	548A
<a href="#">TCA9548AMRGER</a>	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548AMRGER.B	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548AMRGERG4	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548AMRGERG4.B	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
<a href="#">TCA9548APWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A
TCA9548APWR.B	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A
TCA9548APWRG4	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A
TCA9548APWRG4.B	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A
<a href="#">TCA9548ARGER</a>	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548ARGER.B	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548ARGERG4	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A
TCA9548ARGERG4.B	Active	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF TCA9548A :**

- Automotive : [TCA9548A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9548ADGSR	VSSOP	DGS	24	5000	330.0	16.4	5.44	6.4	1.45	8.0	16.0	Q1
TCA9548AMRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1
TCA9548AMRGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1
TCA9548APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9548APWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9548ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9548ARGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9548ADGSR	VSSOP	DGS	24	5000	353.0	353.0	32.0
TCA9548AMRGER	VQFN	RGE	24	3000	353.0	353.0	32.0
TCA9548AMRGERG4	VQFN	RGE	24	3000	353.0	353.0	32.0
TCA9548APWR	TSSOP	PW	24	2000	353.0	353.0	32.0
TCA9548APWRG4	TSSOP	PW	24	2000	353.0	353.0	32.0
TCA9548ARGER	VQFN	RGE	24	3000	353.0	353.0	32.0
TCA9548ARGERG4	VQFN	RGE	24	3000	353.0	353.0	32.0



**RGE 24**

**GENERIC PACKAGE VIEW**

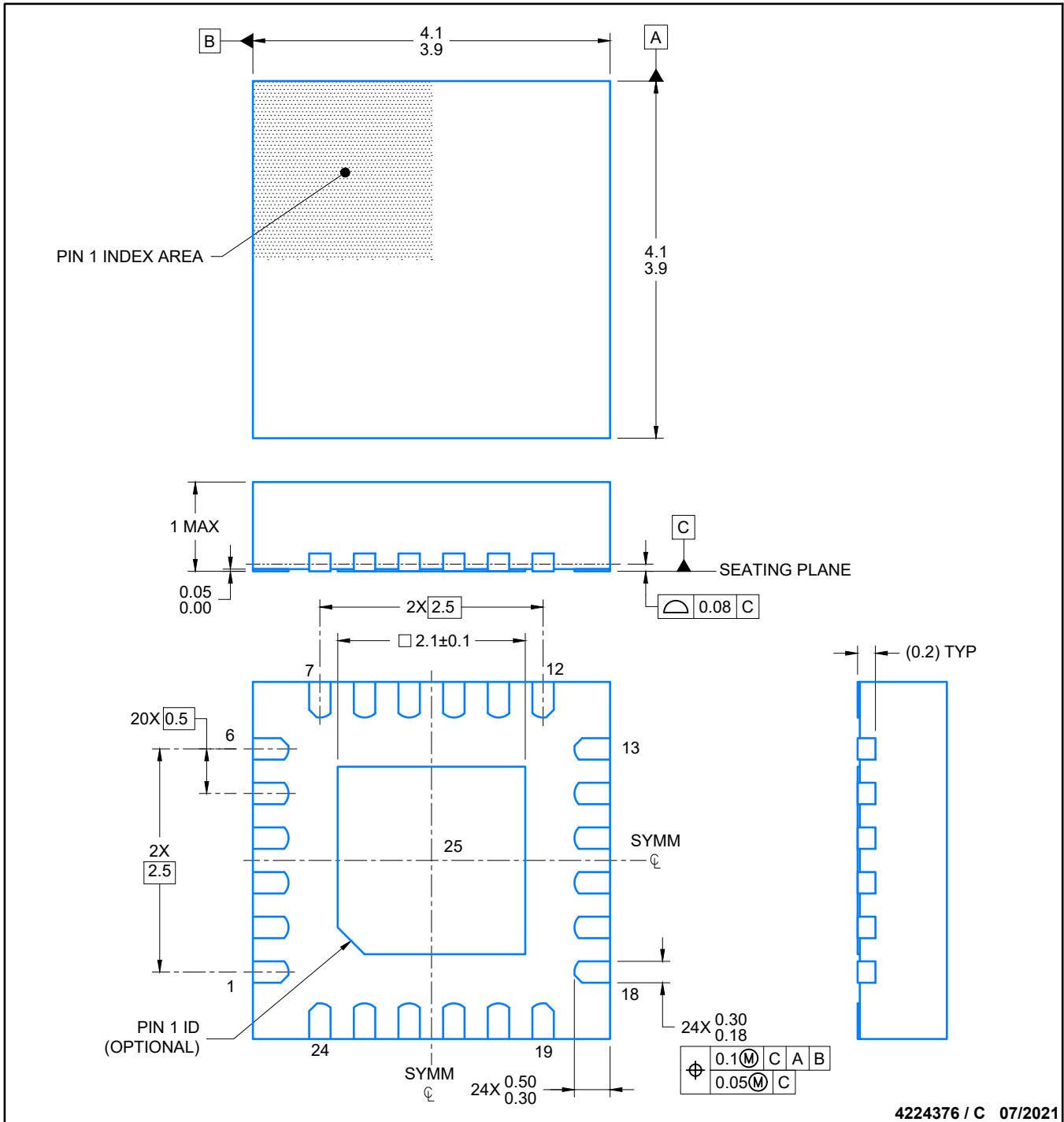
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



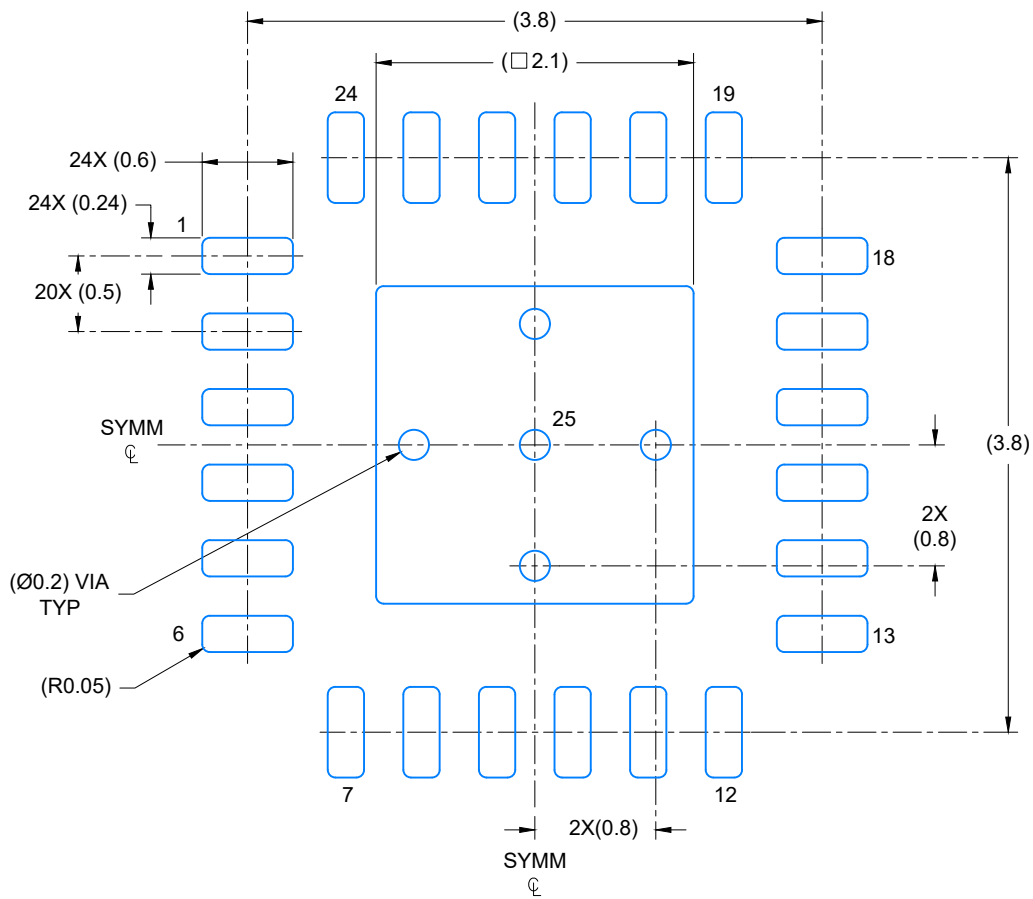
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H

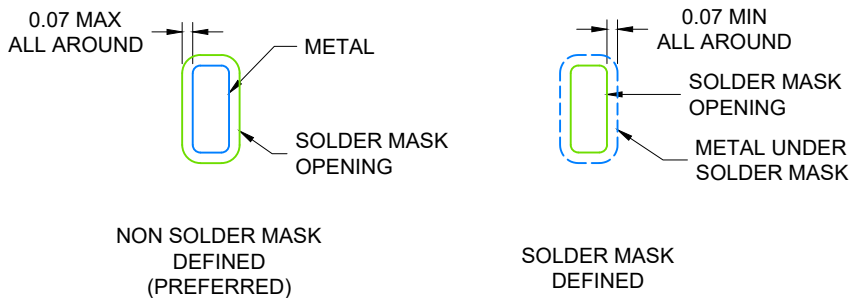


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE  
SCALE: 20X

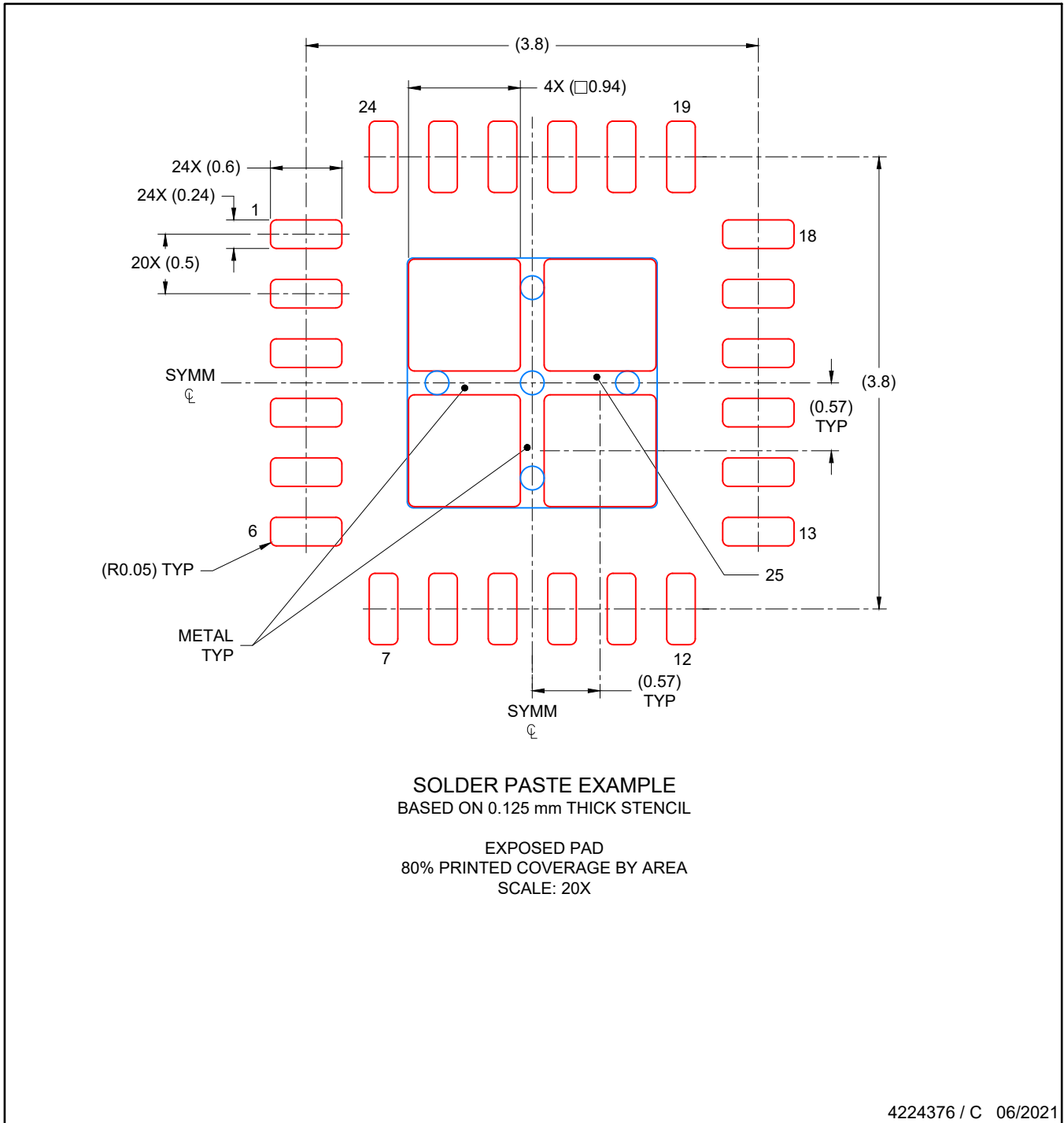


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PW0024A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

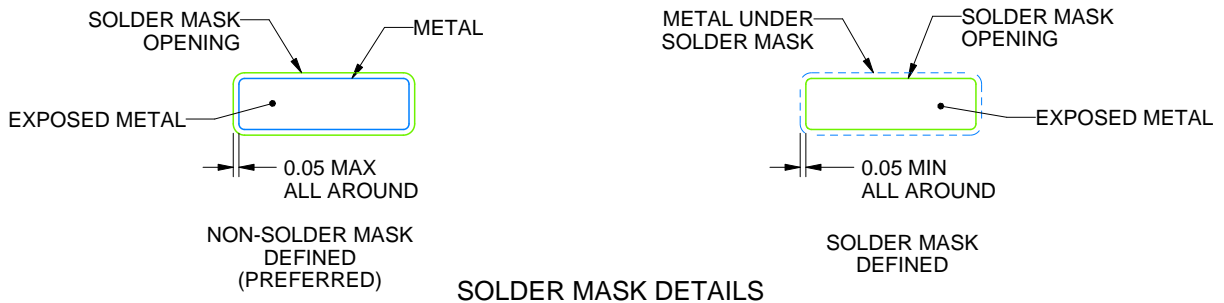
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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