

ZHCSA65-SEPTEMBER 2012

TCA6418E

由 I²C 控制的 18 通道通用输入输出 (GPIO) 扩展器

查询样品: TCA6418E

应用范围

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智能电话

MP3 播放器

数码照相机

掌上电脑 (PDA)

全球卫星定位 (GPS) 设备

特性

- 1.65 V 至 3.6 V 的工作电源电压范围
- 18 个可被置为输入或输出的 GPIO
- 在非 GPIO 引脚上静电放电 (ESD) 保护超过 JESD 22 标准
 - 2000V 人体模型 (A114-A)
 - 1000V 充电器件模型 (C101)
- 低待机(空闲)电流消耗: 3µA
- 支持 1MHz 快速模式加上 I²C 总线
- 开漏低电平有效中断输出,当键被按下或者键被释 放时置为有效
- 50µs 的可选消抖时间
- 施密特触发器操作可在 SCL 和 SDA 输入端实现慢速输入转换和更佳的噪声抗扰度:在 1.8V 时 V_{hys} 典型值为 0.18V
- 锁断性能超过 200mA (符合 JESD 78, II 类规范 的要求)
- 极小型封装
 - 晶圆级芯片封装 (WCSP)(YFP): 2mm x
 2mm; 0.4mm 焊球间距

说明/订购信息

TCA6418E 是一款带有集成 ESD 保护的 18 通道 GPIO 扩展器件。 它能够在 1.65V 至 3.6V 电源电压下运行,并 且具有可通过I²C 接口 [串行时钟 (SCL),串行数据 (SDA)] 使用的 18 个通用输入/输出 (GPIO) 接口。

这个器件的主要优势是将处理器从必须单独监视多个输入变化中解放出来并且也使得处理器上的 GPIO 能够驱动其 它输出。 这样就节省了功耗和带宽。 TCA6418E 还是具有有限数量 GPIO 用法的理想选择。

订购信息(1)									
T _A	封装(2)		可订购部件号	正面标记					
-40°C 至85°C	WCSP-YFP	卷带	TCA6418EYFPR	AZ2					

(1) 要获得最新的封装和订货信息,请参阅本文档末尾的封装选项附录,或者登录 TI 网站www.ti.com进行查询。

(2) 封装图样、热数据和符号可登录www.ti.com/packaging获取。



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



Table 1. YFP Package Terminal Assignments

Е	INT	GND	GPIO13	GPIO8	GPIO4
D	SCL	GPIO17	GPIO12	GPIO7	GPIO3
С	SDA	GPIO16	GPIO11	GPIO6	GPIO2
в	V _{CC}	GPIO15	GPIO10	GND	GPIO1
Α	RESET	GPIO14	GPIO9	GPIO5	GPIO0
	5	4	3	2	1



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TERMINAL FUNCTIONS							
TEF	MINAL						
NO.		TYPE	DESCRIPTION				
WCSP (YFP)	NAME						
A1	GPIO0	I/O	GPIO port				
B1	GPIO1	I/O	GPIO port				
C1	GPIO2	I/O	GPIO port				
D1	GPIO3	I/O	GPIO port				
E1	GPIO4	I/O	GPIO port				
A2	GPIO5	I/O	GPIO port				
B2	GND	-	Ground				
C2	GPIO6	I/O	GPIO port				
D2	GPIO7	I/O	GPIO port				
E2	GPIO8	I/O	GPIO port				
A3	GPIO9	I/O	GPIO port				
B3	GPIO10	I/O	GPIO port				
C3	GPIO11	I/O	GPIO port				
D3	GPIO12	I/O	GPIO port				
E3	GPIO13	I/O	GPIO port				
A4	GPIO14	I/O	GPIO port				
B4	GPIO15	I/O	GPIO port				
C4	GPIO16	I/O	GPIO port				
D4	GPIO17	I/O	GPIO port				
E4	GND	-	Ground				
A5	RESET	I	Active-low reset input. Connect to V_{CC} through a pullup resistor, if no active connection is used.				
B5	V _{CC}	Pwr	Supply voltage of 1.65 V to 3.6 V				
C5	SDA	I/O	Serial data bus. Connect to V _{CC} through a pullup resistor.				
D5	SCL	I	Serial clock bus. Connect to V _{CC} through a pullup resistor.				
E5	INT	0	Active-low interrupt output. Open drain structure. Connect to V _{CC} through a pullup resistor.				

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V _{CC}	Supply voltage range			-0.5	4.6	V
VI	Input voltage range ⁽²⁾			-0.5	4.6	V
Vo	Voltage range applied to any output	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾				
	Output voltage range in the high or	-0.5	4.6	V		
I _{IK}	Input clamp current	V ₁ < 0	V _I < 0		±20	mA
I _{OK}	Output clamp current	V _O < 0			±20	mA
		P port, SDA	V Oto V		50	mA
OL	Continuous output Low current	INT	$v_0 = 0.10 v_{CC}$		25	
I _{OH}	Continuous output High current	P port	$V_{O} = 0$ to V_{CC}		50	
T _{stg}	Storage temperature range			-65	150	°C

(1) Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	YFP package	98.8	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
VIH	High-level input voltage	SCL, SDA, GPIO0-17, RESET	$0.7 \times V_{CC}$	3.6	V
VIL	Low-level input voltage	SCL, SDA, GPIO0-17, RESET	-0.5	$0.3 \times V_{CC}$	V
I _{OH}	High-level output current	GPIO0-17		10	mA
I _{OL}	Low-level output current	GPIO0-17		25	mA
T _A	Operating free-air temperature		-40	85	°C



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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 1.65 V to 3.6 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		V _{CCP}	MIN	TYP	MAX	UNIT
VIK	Input diode clamp voltage	I _I = -18 mA		1.65 V to 3.6 V	-1.2			V
V _{POR}	Power-on reset voltage	$V_{I} = V_{CCP}$ or GND, $I_{O} = 0$		1.65 V to 3.6 V		1	1.4	V
		$I_{OH} = -1 \text{ mA}$		1.65 V	1.25			
				1.65 V	1.2			
		$I_{OH} = -8 \text{ mA}$		2.3 V	1.8			
V _{OH}	GPIO0-17 high-level output			3 V	2.6			V
	voltage			1.65 V	1.1			
		$I_{OH} = -10 \text{ mA}$		2.3 V	1.7			
				3 V	2.5			
		I _{OL} = 1 mA		1.65 V			0.4	
	GPIO0-17 low-level output voltage			1.65 V			0.45	
		I _{OL} = 8 mA		2.3 V			0.25	V
V _{OL}				3 V			0.25	
		I _{OL} = 10 mA		1.65 V			0.6	
				2.3 V			0.3	
				3 V			0.25	
	SDA	V _{OL} = 0.4 V		1.65 V to 3.6 V	3			~
OL	INT	V _{OL} = 0.4 V		1.65 V to 3.6 V	3			mA
I _I	SCL, SDA, GPIO0-17, RESET	$V_{I} = V_{CCI}$ or GND; Pull-downs disable 17	ed for GPIO0-	1.65 V to 3.6 V			1	μA
r _{INT}	GPIO0-17					55		kΩ
			$f_{SCL} = 0 \text{ kHz}$				13	
I _{CC}		V _I on SDA, GPIO0–17, = V _{CC} or GND.	f _{SCL} = 400 kHz	1.65 V to 3.6 V			25	μA
		$I_{O} = 0$, I/O = inputs,	f _{SCL} = 1 MHz				35	
CI	SCL	V _I = V _{CCI} or GND		1.65 V to 3.6 V		6	8	pF
C	SDA			1.65 \/ to 2.6 \/		10	12.5	ъĘ
Uio	GPIO0-17		$V_{IO} = V_{CC}$ or GND			5	6	μr

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I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

		STANDARD MODE I ² C BUS		FAST MO I ² C BUS	DE S	FAST MODE PLUS (FM+) I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{scl}	I ² C clock frequency	0	100	0	400	0	1000	kHz
t _{sch}	I ² C clock high time	4		0.6		0.26		μs
t _{scl}	I ² C clock low time	4.7		1.3		0.5		μs
t _{sp}	I ² C spike time		50		50		50	ns
t _{sds}	I ² C serial data setup time	250		100		50		ns
t _{sdh}	I ² C serial data hold time	0		0		0		ns
t _{icr}	I ² C input rise time		1000	20 + 0.1C _b ⁽¹⁾	300		120	ns
t _{icf}	I ² C input fall time		300	20 + 0.1C _b ⁽¹⁾	300		120	ns
t _{ocf}	I ² C output fall time; 10 pF to 400 pF bus		300	20 + 0.1C _b ⁽¹⁾	300		120	μs
t _{buf}	I ² C bus free time between Stop and Start	4.7		1.3		0.5		μs
t _{sts}	I ² C Start or repeater Start condition setup time	4.7		0.6		0.26		μs
t _{sth}	I ² C Start or repeater Start condition hold time	4		0.6		0.26		μs
t _{sps}	I ² C Stop condition setup time	4		0.6		0.26		μs
t _{vd(data)}	Valid data time; SCL low to SDA output valid		1		0.9		0.45	μs
t _{vd(ack)}	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		0.9		0.45	μs

(1) C_b = total capacitance of one bus line in pF

RESET TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 15)

		STANDARD MODE, FAS MODE, FAST MODE PLU (FM+) I ² C BUS	IS IS	UNIT
		MIN	VAN	
t _W	Reset pulse duration	120 ⁽¹⁾		μs
t _{REC}	Reset recovery time	120 ⁽¹⁾		μs
t _{RESET}	Time to reset	120 ⁽¹⁾		μs

(1) The GPIO debounce circuit uses each GPIO input which passes through a two-stage register circuit. Both registers are clocked by the same clock signal, presumably free-running, with a nominal period of 50uS. When an input changes state, the new state is clocked into the first stage on one clock transition. On the next same-direction transition, if the input state is still the same as the previously clocked state, the signal is clocked into the second stage, and then on to the remaining circuits. Since the inputs are asynchronous to the clock, it will take anywhere from zero to 50 µsec after the input transition to clock the signal into the first stage. Therefore, the total debounce time may be as long as 100 µsec. Finally, to account for a slow clock, the spec further guard-banded at 120 µsec.



SWITCHING CHARACTERISTICS

PARAMETER		FROM	то	STANDARD FAST MODE MODE PLUS I ² C BU	UNIT			
					MIN	MAX		
t _{IV}	Interrupt valid time	GPI_INT with Debounce Enabled	CDI00 17	ĪNT		40	120	
		GPI_INT with Debounce Disabled	GPI00-17		0	1	μs	
t _{IR}	Interrupt reset delay time		SCL	INT		1	μs	
t _{PV}	Output data valid		SCL	GPIO0-17		400	ns	
t _{PS}	Input data setup time	Dehauman Dischlad	GPIO	SCL	0		ns	
t _{PH}	Input data hold time	Debounce Disabled	GPIO	SCL	300		ns	

LOGIC DIAGRAM (POSITIVE LOGIC)



At power on, the GPIOs are configured as inputs with internal 50-k Ω pulldown resistors enabled; however, the system master can enable the GPIOs to function as inputs or outputs.

The system master can reset the TCA6418E in the event of a timeout or other improper operation by asserting a low in the RESET input, while keeping the V_{CC} at its operating level.

A reset can be accomplished by holding the $\overrightarrow{\text{RESET}}$ pin low for a minimum of t_W. The TCA6418E registers and I²C/SMBus state machine are changed to their default state once $\overrightarrow{\text{RESET}}$ is low (0). When $\overrightarrow{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to VCC, if no active connection is used.

The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. The RESET pin causes the same reset/initialization to occur without de-powering the part.

The open-drain interrupt (INT) output is used to indicate to the system master that an input state has changed. INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote input can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the TCA6418E can remain a simple slave device.



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Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA6418E in a reset condition until V_{CC} reaches V_{POR}. At that time, the reset condition is released, and the TCA6418E registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered below 0.2 V and back up to the operating voltage for a power-reset cycle.

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6418E can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 1 and Figure 2.



Figure 1. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}



Figure 2. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 2 specifies the performance of the power-on reset feature for TCA6418E for both types of power-on reset.

Table 2. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES

	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC_FT}	Fall rate	See Figure 1	1		100	ms
V _{CC_RT}	Rise rate	See Figure 1	0.01		100	ms
V _{CC_TRR_GND}	Time to re-ramp (when V _{CC} drops to GND)	See Figure 1	0.001			ms
V _{CC_TRR_POR50}	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV)	See Figure 2	0.001			ms
V _{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See Figure 3			1.2	V
V _{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCx}$	See Figure 3				μs
V _{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V _{PORR}	Voltage trip point of POR on rising V _{CC}		1.033		1.428	V

(1) $T_A = -40^{\circ}C$ to 85°C (unless otherwise noted)



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Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 3 and Table 2 provide more information on how to measure these specifications.



Figure 3. Glitch Width and Glitch Height

 V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 4 and Table 2 provide more details on this specification.



For proper operation of the power-on reset feature, use as directed in the figures and table above.

Interrupt Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} , the signal INT is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as INT.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

The \overline{INT} output has an open-drain structure and requires a pullup resistor to V_{CC} depending on the application. For more information on the interrupt output feature, see Control Register and Command Byte and Typical Applications.



I²C Interface

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The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 5). After the <u>Start</u> condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 6).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 5).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.



Figure 5. Definition of Start and Stop Conditions



Figure 6. Bit Transfer





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Device Address

The address of the TCA6418E is shown in Table 3.

Table 3.

ВҮТЕ	BIT									
	7 (MSB)	6	5	4	3	2	1	0 (LSB)		
I ² C slave address	0	1	1	0	1	0	0	R/W		

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.



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Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA6418E. The command byte indicates the register that will be updated with information. All registers can be read and written to by the system master.

Table 4 shows all the registers within this device and their descriptions. The default value in all registers is 0.

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	7	6	5	4	3	2	1	0
0×00	Reserved	Reserved								
0×01	Reserved	Reserved								
0×02	INT_STAT	Interrupt status register	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPI_IN T	N/A 0
0×03	Reserved	Reserved								
0×04	Reserved	Reserved								
0×05	Reserved	Reserved								
0×06	Reserved	Reserved								
0×07	Reserved	Reserved								
0×08	Reserved	Reserved								
0×09	Reserved	Reserved								
0×0A	Reserved	Reserved								
0×0B	Reserved	Reserved								
0×0C	Reserved	Reserved								
0×0D	Reserved	Reserved								
0×0E	Reserved	Reserved								
0×0F	Reserved	Reserved								
0×10	Reserved	Reserved								
0×11	GPIO_INT_STAT1	GPIO interrupt status	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×12	GPIO_INT_STAT2	GPIO interrupt status	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×13	GPIO_INT_STAT3	GPIO interrupt status	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×14	GPIO_DAT_STAT1 (read twice to clear)	GPIO data status	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×15	GPIO_DAT_STAT2 (read twice to clear)	GPIO data status	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×16	GPIO_DAT_STAT3 (read twice to clear)	GPIO data status	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×17	GPIO_DAT_OUT1	GPIO data out	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×18	GPIO_DAT_OUT2	GPIO data out	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×19	GPIO_DAT_OUT3	GPIO data out	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×1A	GPIO_INT_EN1	GPIO interrupt enable	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0

Table 4. Register Descriptions



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TCA6418E

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	7	6	5	4	3	2	1	0
0×1B	GPIO_INT_EN2	GPIO interrupt enable	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×1C	GPIO_INT_EN3	GPIO interrupt enable	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×1D	Reserved	Reserved								
0×1E	Reserved	Reserved								
0×1F	Reserved	Reserved								
0×20	Reserved	Reserved								
0×21	Reserved	Reserved								
0×22	Reserved	Reserved								
0×23	GPIO_DIR1	GPIO data direction 0: input 1: output	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×24	GPIO_DIR2	GPIO data direction 0: input 1: output	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×25	GPIO_DIR3	GPIO data direction 0: input 1: output	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×26	GPIO_INT_LVL 1	GPIO edge/level detect 0: low 1: high	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×27	GPIO_INT_LVL 2	GPIO edge/level detect 0: low 1: high	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×28	GPIO_INT_LVL 3	GPIO edge/level detect 0: low 1: high	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×29	DEBOUNCE_DIS 1	Debounce disable 0: enabled 1: disabled	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×2A	DEBOUNCE_DIS 2	Debounce disable 0: enabled 1: disabled	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×2B	DEBOUNCE_DIS 3	Debounce disable 0: enabled 1: disabled	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×2C	GPIO_PULL1	GPIO pulldown 0: pulldown enabled 1: pulldown disabled	GPIO0 0	GPIO1 0	GPIO2 0	GPIO3 0	GPIO4 0	GPIO 5 0	GPIO6 0	GPIO7 0
0×2D	GPIO_PULL2	GPIO pulldown 0: pulldown enabled 1: pulldown disabled	GPIO15 0	GPIO14 0	GPIO13 0	GPIO12 0	GPIO11 0	GPIO 10 0	GPIO9 0	GPIO8 0
0×2E	GPIO_PULL3	GPIO pulldown 0: pulldown enabled 1: pulldown disabled	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	GPIO17 0	GPIO16 0
0×2F	Reserved									

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Interrupt Status Register, INT_STAT (Address 0×02)

GPI_INT (BIT1) reflects the status of the INT pin. If GPI_INT is 1, INT is asserted. Write 0x02 to INT_STAT register to clear interrupt.

GPIO Interrupt Status Registers, GPIO_INT_STAT1-3 (Address 0×11-0×13)

These registers are used to check GPIO interrupt status and are cleared on read.

GPIO Data Status Registers, GPIO_DAT_STAT1-3 (Address 0x14-0x16)

These registers show GPIO state when read for inputs and outputs.

GPIO Data Out Registers, GPIO_DAT_OUT1-3 (Address 0×17-0×19)

These registers contain GPIO data to be written to GPIO out driver; inputs are not affected. This is needed so that the value can be written prior to being set as an output.

GPIO Interrupt Enable Registers, GPIO_INT_EN1-3 (Address 0×1A-0×1C)

These registers enable interrupts for GP inputs only.

GPIO Data Direction Registers, GPIO_DIR1-3 (Address 0×23-0×25)

A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output.

GPIO Edge/Level Detect Registers, GPIO_INT_LVL1-3 (Address 0x26-0x28)

A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

Debounce Disable Registers, DEBOUNCE_DIS1-3 (Address 0×29-0×2B)

This is for pins configured as inputs. A bit value of '0' in any of the unreserved bits enables the debounce while a bit value of '1' disables the debounce.





The reset line always has a 50-µs debounce time.

The 50 µs debounce time for inputs is the time required for the input to be stable to be noticed.

GPIO Pull Disable Register, GPIO_PULL1-3 (Address 0×2C-0×2E)

This register enables or disables pulldown registers from inputs.



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Bus Transactions

Data is exchanged between the master and TCA6418E through write and read commands.

Writes

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Data is transmitted to the TCA6418E by sending the device address and setting the least significant bit (LSB) to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.



Figure 8. Write to Output Port Register





Reads

The bus master first must send the TCA6418E address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6418E (see Figure 10 and Figure 11). Data is clocked into the register on the rising edge of the ACK clock pulse.





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Figure 11. Read From Input Port Register



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$T_A = 25^{\circ}C$ (unless otherwise noted) SUPPLY CURRENT STANDBY SUPPLY CURRENT vs vs TEMPERATURE TEMPERATURE 12 1600 11 1400 10 V_{cc} = 3.6 V 9 1200 Supply Current, I $_{cc}$ (µA) V_{cc} = 3.3 V Supply Current, I cc (nA) 8 $V_{cc} = 3.6 V$ 1000 7 6 V_{cc} = 3.3 V 800 V_{cc} = 2.5 V V_{cc} = 2.5 V 5 600 4 V_{cc} = 1.8 V V_{cc} = 1.8 V 3 400 V_{cc} = 1.65 V 2 $V_{cc} = 1.65 V$ 200 1 0 0 85 -40 -15 10 35 60 -40 -15 10 35 60 85 Temperature, T_A (°C) Temperature, T_A (°C) SUPPLY CURRENT **I/O SINK CURRENT** vs vs OUTPUT LOW VOLTAGE SUPPLY VOLTAGE 60 11 V_{cc} = 1.65 V 10 50 9 T_A = -40°C 8 Supply Current, I cc (uA) Sink Current, I _{SINK} (mA) 00 00 00 00 - T_A = 25°C 7 T_A = 85°C 6 5 4 3 2 10 1 0 0 1.6 2.0 2.4 2.8 3.2 3.6 0.2 0.0 0.1 0.3 0.4 0.5 0.6 Supply Voltage, V_{cc} (V) Output Low Voltage, V_{OL} (V)

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS (continued)



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TYPICAL CHARACTERISTICS (continued)



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PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I ² C address
2	Input register port data

- A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r/t_f \leq 30 ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 12. I²C Interface Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)

INTERRUPT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r/t_f \leq 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 13. Interrupt Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION (continued)

A. C_L includes probe and jig capacitance.

- B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
- C. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r/t_f \leq$ 30 ns.

READ MODE (R/W = 1)

- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 14. P Port Load Circuit and Timing Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r/t_f \leq 30 ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. I/Os are configured as inputs.
- E. All parameters and waveforms are not applicable to all devices.

Figure 15. Reset Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	. ,	.,				(4)	(5)		.,
TCA6418EYFPR	Active	Production	DSBGA (YFP) 25	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(AZ2, AZN)
TCA6418EYFPR.B	Active	Production	DSBGA (YFP) 25	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(AZ2, AZN)

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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YFP0025



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.



YFP0025

EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

 Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



YFP0025

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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