TCA4311A 热插拔 2 线制总线缓冲器

1 特性

- 2.7V 至 5.5V 工作电源电压范围
- 支持 I^2C 总线信号的双向数据传输
- SDA 和 SCL 线路经过缓冲，因而增加了扇出
- 对所有 SDA 和 SCL 线路的 1V 预充电防止了带电板插入和从背板上移除过程中的损坏
- SDA 和 SCL 输入线路与输出隔离
- 可适应标准模式及快速模式 I^2C 器件
- 抗噪声性能有所改善
- 应用 包括热板插入和总线扩展
- 低 I_{CC} 芯片停用模式：<1μA
- READY 开漏输出
- 支持时钟展宽、仲裁及同步
- 断电高阻抗 I^2C 引脚
- 开漏 I^2C 引脚
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 8000V 人体放电模型 (A114-A)
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 基站
- 工业自动化

3 说明

TCA4311A 是一款热插拔 I^2C 总线缓冲器，支持将 I/O 卡插入带电背板中而不会损坏数据和破坏时钟总线。控制电路可防止背板与板卡相连接（直到背板上出现停止命令或总线空闲为止），而不会在板卡上发生总线争用的情况。当建立连接时，该器件可提供双向缓冲，从而使背板及板卡电容保持隔离。在插入过程中，会对 SDA 和 SCL 线路预充电至 1V，从而最大程度地减小对芯片的寄生电容充电所需的电流。

当 I^2C 总线空闲时，可通过将 EN 引脚设定为低电平将 TCA4311A 置于停机模式下。当 EN 引脚为高电平时，TCA4311A 将恢复正常运作。该器件还包括一个开漏 READY 输出引脚，该引脚负责在背板与板卡侧相连时发出指示信号。当 READY 引脚为高电平时，SDAIN 和 SCLIN 被连接至 SDAOUT 和 SCLOUT。当两侧断开时，READY 引脚为低电平。

背板及板卡均可采用 2.7V 至 5.5V 的电源电压来供电，而对于它们哪一个的电源电压较高则未做限制。

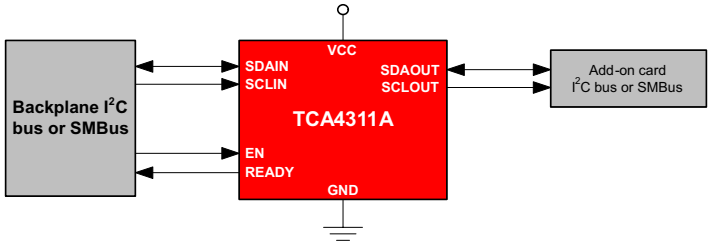
TCA4311A 具有标准的开漏 I/O。I/O 的上拉电阻器的尺寸由系统决定，不过此缓冲器的每一侧都必须有一个上拉电阻器。除了 SMBus 器件，此器件专门用于与标准模式和快速模式的 I^2C 器件一同工作。在可以接受标准模式器件和多个主控器的通用型 I^2C 系统中，标准模式 I^2C 器件只规定了 3mA。在某些条件下，可以采用高结束电流。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA4311A	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

Changes from Revision B (October 2014) to Revision C **Page**

- Moved T_{stg} to the *Absolute Maximum Rating* table ... 4
- Changed the *Handling Rating* table To: *ESD Ratings* ... 4
- Added *Missing ACK Event* section ... 10

Changes from Revision A (July 2012) to Revision B **Page**

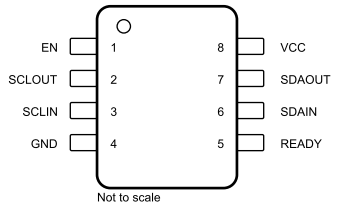
- *处理额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 已更改 更改了 TCA4311A RTA 规格。 ... 1

Changes from Original (January 2011) to Revision A **Page**

- Updated Input-output Offset Voltage vs Pullup Resistor graphic. ... 6

5 Pin Configuration and Functions

D OR DGK Packages
(Top View)



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
EN	1	Active-high chip enable pin. If EN is low, the TCA4311A is in a low current (<1 μA) mode. It also disables the rise-time accelerators, disables the bus pre-charge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. EN should be high (at V_{CC}) for normal operation. Connect EN to V_{CC} if this feature is not being used.
SCLOUT	2	Serial clock output. Connect this pin to the SCL bus on the card.
SCLIN	3	Serial clock input. Connect this pin to the SCL bus on the backplane.
GND	4	Supply ground
READY	5	Connection flag/rise-time accelerator control. READY is low when either EN is low or the start-up sequence described in the operation section has not been completed. READY goes high when EN is high and start-up is complete. Connect a 10-kΩ resistor from this pin to V_{CC} to provide the pull up.
SDAIN	6	Serial data input. Connect this pin to the SDA bus on the backplane.
SDAOUT	7	Serial data output. Connect this pin to the SDA bus on the card.
VCC	8	Supply power. Main input power supply from backplane. This is the supply voltage for the devices on the backplane I^2C busses. Connect pull-up resistors from SDAIN and SCLIN (and also from SDAOUT and SCLOUT) to this pin. Place a bypass capacitor of at least 0.01 μF close to this pin for best results.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)	SDAIN, SCLIN, SDAOUT, SCLOUT	–0.5	7	V
V_I	Input voltage range(2)	EN	–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
I_{CC}	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	5.5	V
V_{IH}	High-level input voltage	EN input	2	5.5	V
V_{IL}	Low-level input voltage	SDA and SCL inputs(1)	–0.5	0.4	V
		EN input	–0.5	0.8	
I_{OL}	Low-level output current	V_{CC} = 3 V		3	mA
		V_{CC} = 4.5 V		3	
T_A	Operating free-air temperature		–40	85	°C

(1) In certain circumstances, devices must be able to drive the input voltage low while sinking current from the rise time accelerators of the TCA4311A (see $I_{PULLUPAC}$ in *Electrical Characteristics*).

6.4 Thermal Information

THERMAL METRIC(1)		TCA4311A		UNIT
		D	DGK	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.2	158.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.5	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	78.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.2	76.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{CC}	Positive supply voltage		2.7		5.5	V
I_{CC}	Supply current	V_{CC} = 5.5 V, V_{SDAIN} = V_{SCLIN} = 0 V		5.1	7	mA
I_{SD}	Supply current in shutdown mode	V_{EN} = 0 V		0.1		µA
Start-Up Circuitry						
V_{PRE}	Pre-charge voltage	SDA, SCL floating	0.8	1	1.2	V
t_{IDLE}	Bus idle time		50	95	150	µs
V_{EN}	EN threshold voltage			0.5 × V_{CC}	0.9 × V_{CC}	V
V_{DIS}	Disable threshold voltage	EN Pin	0.1 × V_{CC}	0.5 × V_{CC}		V
I_{EN}	EN input current	EN from 0 V to V_{CC}		±0.1	±1	µA
t_{EN}	Enable time			95		µs
t_{DIS}	Disable time (EN to READY)			30		ns
t_{STOP}	SDAIN to READY delay after STOP			1.2		µs
t_{READY}	SCLOUT/SDAOUT to READY			0.8		µs
I_{OFF}	READY OFF state leakage current			±0.1		µA
V_{OL}	READY output low voltage	I_{PULLUP} = 3 mA			0.4	V
Rise-Time Accelerators						
$I_{PULLUPAC}$	Transient boosted pull-up current	Positive transition on SDA, SCL, V_{CC} = 2.7 V,	1	8		mA
Input-Output Connection						
V_{OS}	Input-output offset voltage	10 kΩ to V_{CC} on SDA, SCL, V_{CC} = 3.3 V,(1)	0	100	175	mV
C_{IN}	Digital input capacitance				10	pF
V_{OL}	Output low voltage, input = 0 V	SDA, SCL pins, I_{SINK} = 3 mA,	0		0.4	V
I_I	Input leakage current	SDA, SCL pins = V_{CC} = 5.5 V			±5	µA

(1) The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the *Typical Characteristics* section.

6.6 Typical Characteristics

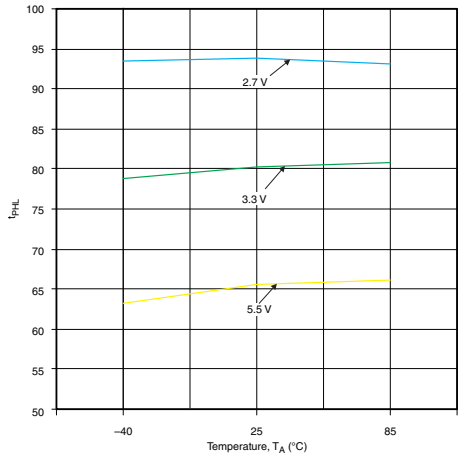


Figure 1. Input-Output t_{PLH} vs Temperature

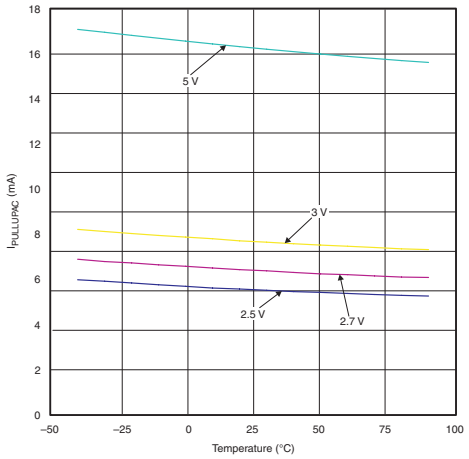


Figure 2. $I_{PULLUPAC}$ vs Temperature

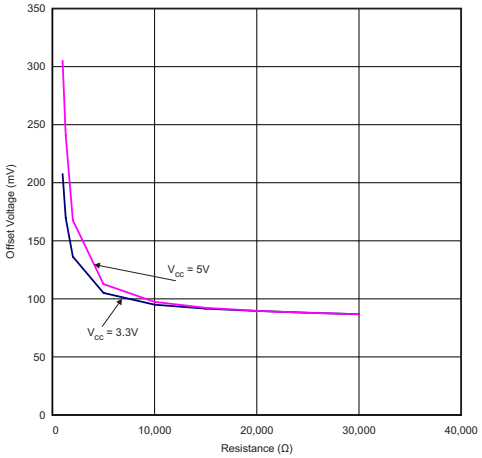
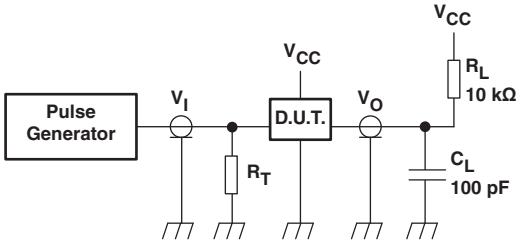


Figure 3. Input-output Offset Voltage vs Pull-Up Resistor

7 Parameter Measurement Information



R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generators.

Figure 4. Test Circuitry for Switching Times

Parameter Measurement Information (continued)

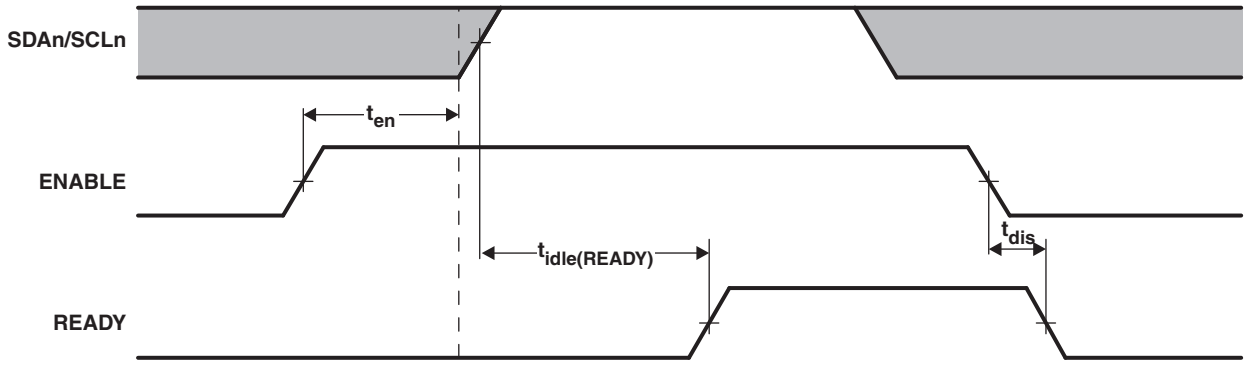


Figure 5. Timing for t_{en}, $t_{idle(READY)}$, and t_{dis}

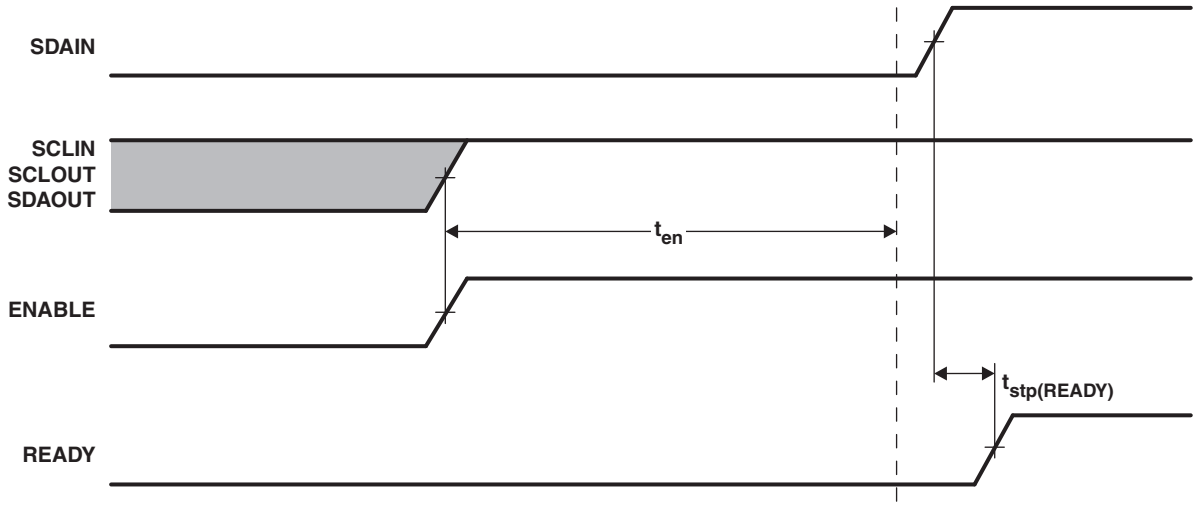


Figure 6. $t_{stp(READY)}$ That Can Occur After t_{en}

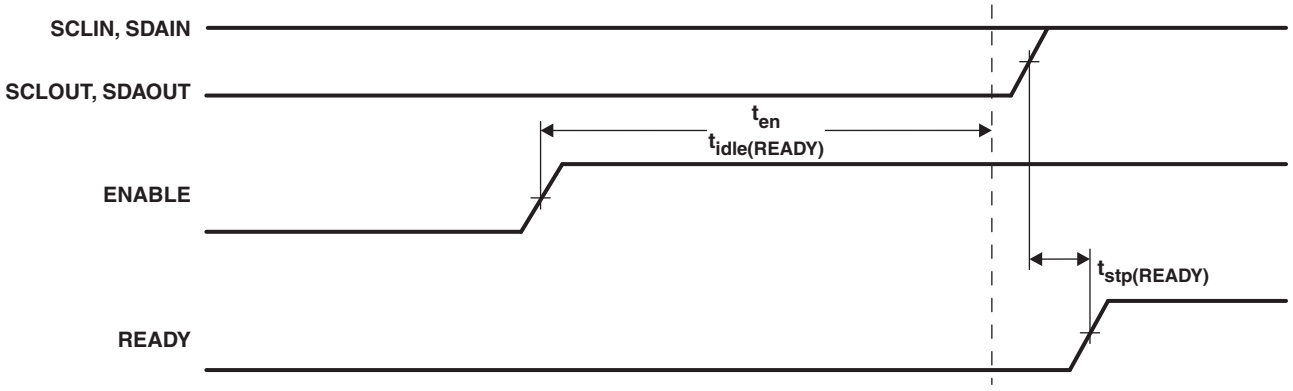


Figure 7. $t_{stp(READY)}$ That Can Occur After t_{en} and $t_{idle(READY)}$

8 Detailed Description

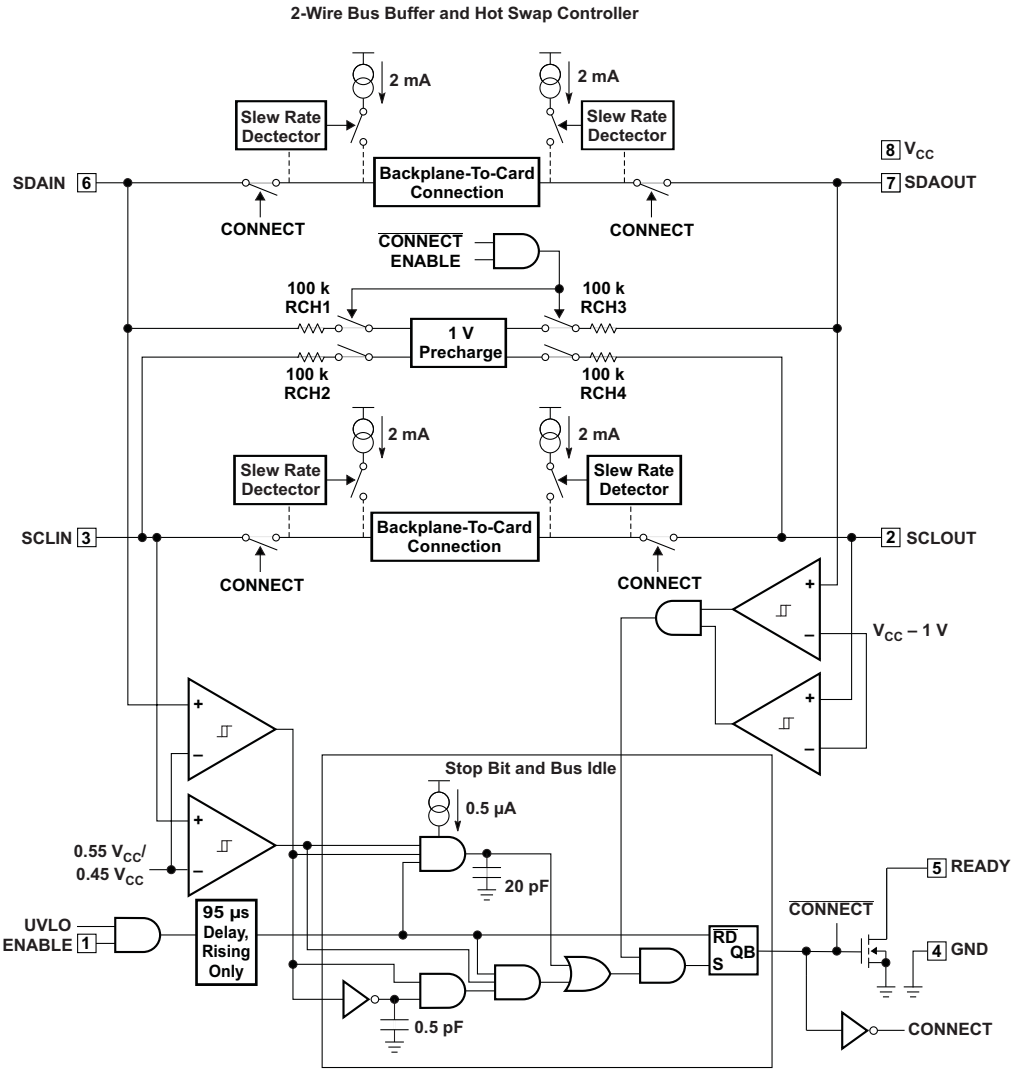
8.1 Overview

The TCA4311A is a bidirectional I^2C buffer optimized for hot-swap applications. The device supports I/O card insertion into a live backplane operating in Standard-Mode (100 kHz) or Fast-Mode (400 kHz). Initially, there is no connection between SCLIN and SCLOUT or between SDAIN and SDAOUT. Upon connection, the TCA4311A provides bidirectional buffering, keeping the card and backplane capacitances isolated from each other.

A pre-charge voltage on all SCL and SDA pins prevents the TCA4311A from disrupting I^2C bus communication during insertion. Bus idle detection determines that there is no communication on the I^2C line when the connection from –IN to –OUT is made. Once the connection is made, the READY pin will output a logic high signal. If the I^2C bus will be inactive for extended periods of time, the TCA4311A can be put in shutdown mode by setting the EN pin to a logic low state. The TCA4311A resumes normal operation when EN is in a logic high state.

As with all I^2C buffers, the TCA4311A requires pull-up resistors on all SCL and SDA pins due to the open-drain output circuitry. However, the integration of rise time accelerators allowed the use of weaker pull-up resistors than would normally be required.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rise-Time Accelerators

Once connection has been established, rise-time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise-time requirements. During positive bus transitions, the TCA4311A switches in 2 mA (typical) of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6 V. Using a general rule of 20 pF of capacitance for every device on the bus (10 pF for the device and 10 pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25 V/μs to specify activation of the accelerators.

For example, assume an SMBus system with V_{CC} = 3 V, a 10-kΩ pull-up resistor and equivalent bus capacitance of 200 pF. The rise-time of an SMBus system is calculated from ($V_{IL(MAX)}$ – 0.15 V) to ($V_{IH(MIN)}$ + 0.15 V), or 0.65 V to 2.25 V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3 V supply; in this case, 0.92 × (10 kΩ × 200 pF) = 1.84 μs. Thus, the system exceeds the maximum allowed rise-time of 1 μs by 84%. However, using the rise-time accelerators, which are activated at a DC threshold of below 0.65 V, the worst-case rise-time is: (2.25 V – 0.65 V) × 200 pF/1 mA = 320 ns, which meets the 1 μs rise-time requirement.

8.3.2 READY Digital Output

This pin provides a digital flag which is low when either EN is low or the start-up sequence described earlier in this section has not been completed. READY goes high when EN is high and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to V_{CC} to provide the pull-up.

8.3.3 EN Low Current Disable

Grounding the EN pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY low, disables the bus pre-charge circuitry and puts the part in a near-zero current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides.

8.4 Device Functional Modes

8.4.1 Start-Up

When the TCA4311A first receives power on its V_{CC} pin, either during power-up or during live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5 V.

During this time, the 1 V pre-charge circuitry is also active and forces 1 V through 100-kΩ nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0 V and V_{CC}. Pre-charging the SCL and SDA pins to 1 V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the TCA4311A comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane, and the rise time accelerators are enabled.

Device Functional Modes (continued)

8.4.2 Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. For proper operation, logic low input voltages should be no higher than 0.4 V with respect to the ground pin voltage of the TCA4311A. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the TCA4311A.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

8.4.3 Missing ACK Event

Description

When the slave (or master) device sends an ACK bit, a logic low on SDA during the 9th clock cycle, the slave (or master) may pull the SDA line low while the rise time accelerators are engaged and the master (or slave) side stays high. The rise time accelerators are engaged when the voltage is above 0.6 V (typical) and the slew rate is above 1.25 V/us. In Figure 8, SDAOUT is a slave attempting to send an ACK bit. SDAOUT pulls to a logic low, but the ACK is not transferred to the other side and SDAIN remains high unexpectedly. The timing window in which this occurs has been approximated to 1 nanosecond and can vary with the loading on the bus.

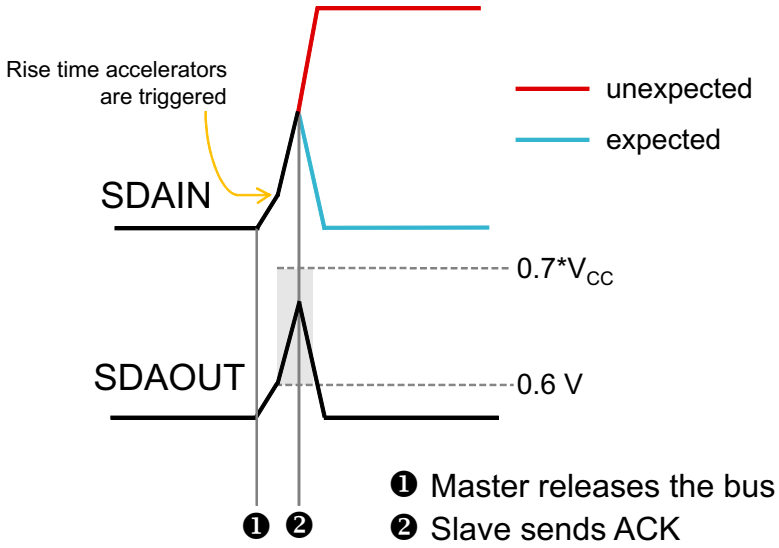


Figure 8. Missing ACK

8.4.3.1 System Impact

The ACK bit is not transferred through the TCA4311A, and the slave or master device interprets the result as a NACK.

8.4.3.2 System Workaround

Changing the bus load on the master or slave side to either a larger value pull up resistor or adding bus capacitance can help to slow down the rise time accelerators from engaging. If adding capacitance, care should be taken to not overload the capacitance above the allowed limit specified by I2C standard.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TCA4311A was designed for applications in which a portion of a communication bus contained on an I/O card or add-on card, is inserted into a live backplane where the main communication bus is already active, which is known as hot-swapping. The two types of communication buses supported by the TCA4311A are I^2C and SMBus. System management for PCI cards is an application of the SMBus protocol, which adds on to the electrical specifications and hardware addressing protocol of I^2C with second-level software for building special systems that may include dynamic addressing. The following application schematics and descriptions give examples of a typical application of the TCA4311A (Figure 9), a CompactPCI™ system configuration (Figure 12), a PCI system configuration (Figure 13), repeater or bus-extender application (Figure 14), and a system with disparate voltage supplies (Figure 15).

9.2 Typical Application

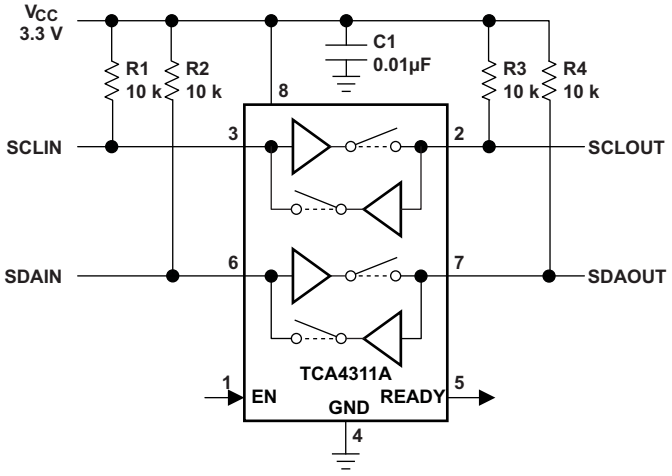


Figure 9. Application Schematic

9.2.1 Design Requirements

9.2.1.1 Input to Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the TCA4311A's data or clock pins, the TCA4311A regulates the voltage on the other side of the chip (call it V_{LOW2}) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 75\ mV + (V_{CC}/R) \times 100 \quad (1)$$

where R is the bus pull-up resistance in ohms (Ω). For example, if a device is forcing SDAOUT to 10 mV where V_{CC} = 3.3 V and the pull-up resistor R on SDAIN is 10 kΩ, then the voltage on SDAIN = 10 + 75 + (3.3/10000) × 100 = 118 mV. See the *Typical Characteristics* section for curves showing the offset voltage as a function of V_{CC} and R.

Typical Application (continued)

9.2.1.2 Propagation Delays

During a rising edge, the rise-time on each side is determined by the combined pull-up current of the TCA4311A boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 10 for V_{CC} = 3.3 V and a 10-kΩ pull-up resistor on each side (50 pF on one side and 150 pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative.

There is a finite propagation delay, t_{PHL}, through the connection circuitry for falling waveforms. Figure 11 shows the falling edge waveforms for the same V_{CC}, pull-up resistors and equivalent capacitance conditions as used in Figure 10. An external NMOS device pulls down the voltage on the side with 150 pF capacitance; the TCA4311A pulls down the voltage on the opposite side, with a delay of 55 ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The *Typical Characteristics* section shows t_{PHL} as a function of temperature and voltage for 10-kΩ pull-up resistors and 100 pF equivalent capacitance on both sides of the part. By comparison with Figure 11, the V_{CC} = 3.3 V curve shows that increasing the capacitance from 50 pF to 100 pF results in a t_{PHL} increase from 55 ns to 75 ns. Larger output capacitances translate to longer delays (up to 150 ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Pull-Up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value R using the formula:

$$R \leq (V_{CC(MIN)} - 0.6)\ (800{,}000) / C \quad (2)$$

where R is the pull-up resistor value in ohms, $V_{CC(MIN)}$ is the minimum V_{CC} voltage and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R ≤ 16 kΩ for V_{CC} = 5.5 V maximum, R ≤ 24 kΩ for V_{CC} = 3.6 V maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the pre-charge voltage.

9.2.3 Application Curves

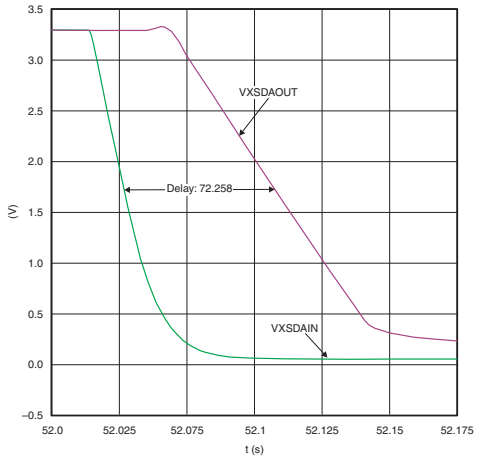


Figure 10. Input-Output Connection t_{PLH}

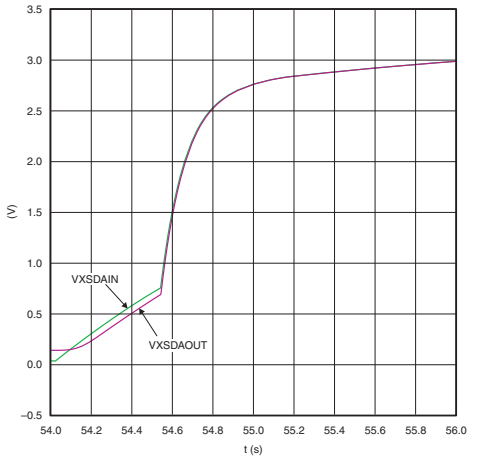


Figure 11. Input-Output Connection t_{PHL}

Typical Application (continued)

9.2.4 Live Insertion and Capacitance Buffering CompactPCI™ Application

Figure 12 through Figure 13 illustrate the usage of the TCA4311A in applications that take advantage of both its hot swap controlling and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a TCA4311A on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the TCA4311A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the TCA4311A, which is less than 10 pF.

Figure 12 shows the TCA4311A in a CompactPCI™ configuration. Connect V_{CC} and EN to the output of one of the CompactPCI™ power supply Hot Swap circuits. Use a pull-up resistor to EN for a card side enable/disable.

V_{CC} is monitored by a filtered UVLO circuit. With the V_{CC} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with live insertion have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

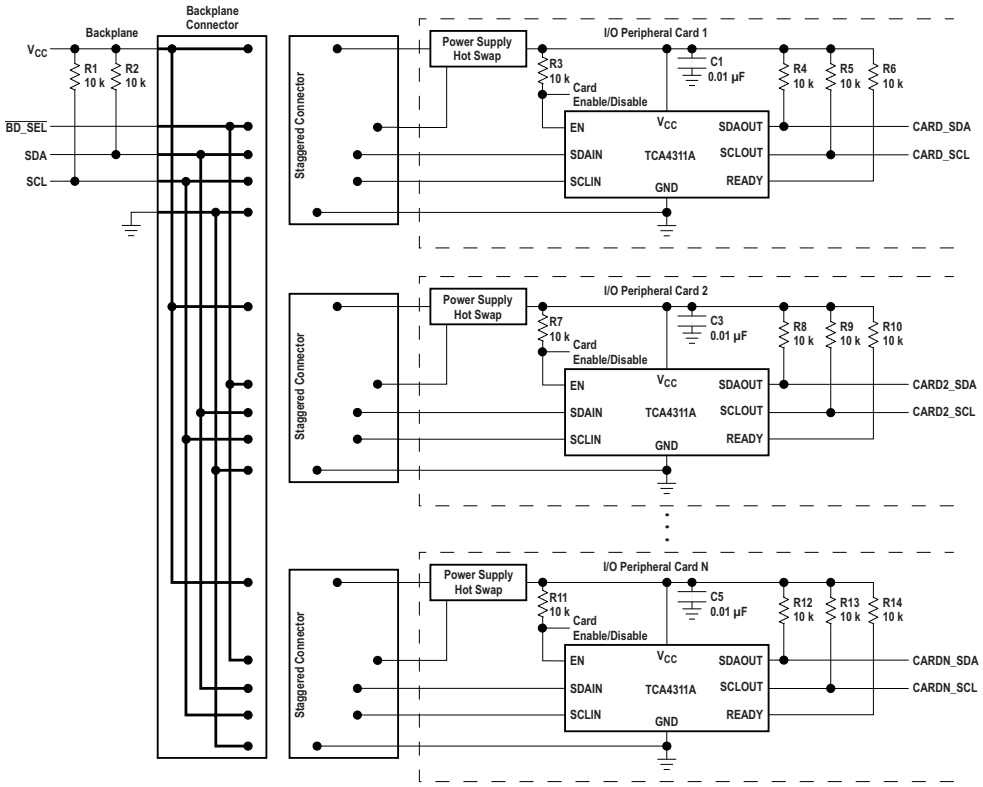


Figure 12. Inserting Multiple I/O Cards into a Live Backplane Using the TCA4311A in a CompactPCI System

9.2.4.1 Design Requirements

Refer to *Design Requirements*.

9.2.4.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.4.3 Application Curves

Refer to *Application Curves*.

Typical Application (continued)

9.2.5 Live Insertion and Capacitance Buffering PCI Application

Figure 13 shows the TCA4311A in a PCI application, where all of the pins have the same length. In this case, connect an RC series circuit on the I/O card between V_{CC} and EN. An RC product of 10 ms provides a filter to prevent the TCA4311A from becoming activated until the transients associated with live insertion have settled.

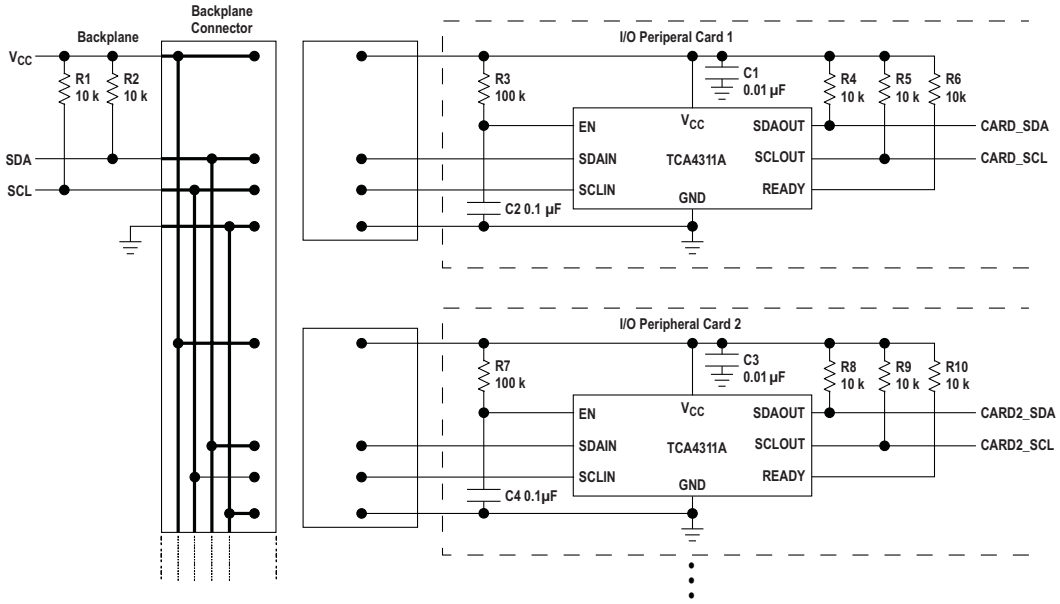


Figure 13. Inserting Multiple I/O Cards into a Live Backplane Using the TCA4311A in a PCI System Schematic

9.2.5.1 Design Requirements

Refer to *Design Requirements*.

9.2.5.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.5.3 Application Curves

Refer to *Application Curves*.

Typical Application (continued)

9.2.6 Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two TCA4311A back-to-back, as shown in Figure 14. The I^2C specification allows for 400 pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise- and fall-time specifications are to be met. The strong pull-up and pull-down impedances of the TCA4311A are capable of meeting rise- and fall-time specifications for one nano-Farad of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back TCA4311A add together, directly contributing to the same problem.

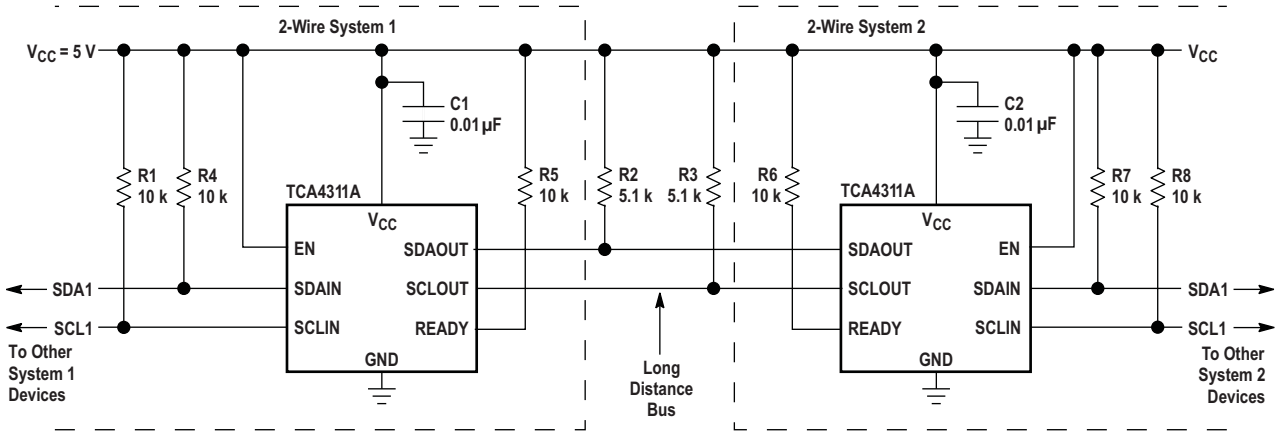


Figure 14. Repeater/Bus Extender Schematic

9.2.6.1 Design Requirements

Refer to *Design Requirements*.

9.2.6.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.6.3 Application Curves

Refer to *Application Curves*.

Typical Application (continued)

9.2.7 Systems With Disparate Supply Voltages

In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is well modeled by a series resistor in the V_{CC} line, as shown in Figure 15. For proper operation of the TCA4311A, make sure that $V_{CC(BUS)} \geq V_{CC(TCA4311A)} - 0.5$ V.

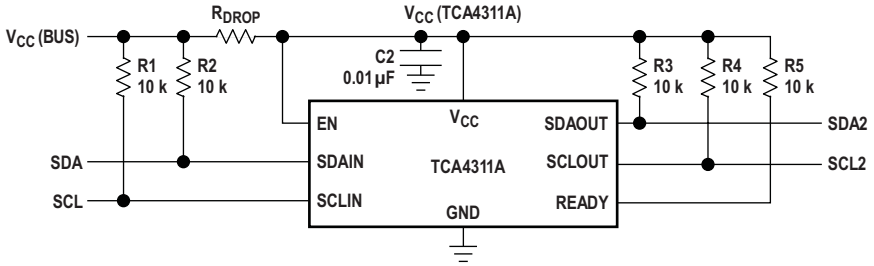


Figure 15. System With Disparate V_{CC} Voltages Schematic

9.2.7.1 Design Requirements

Refer to *Design Requirements*.

9.2.7.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.7.3 Application Curves

Refer to *Application Curves*.

10 Power Supply Recommendations

In order for the pre-charge circuitry to dampen the effect of hot-swap insertion of the TCA4311A into an active I^2C bus, V_{CC} must be applied before the SCL and SDA pins make contact to the main I^2C bus. This is essential when the TCA4311A is placed on the add-on card circuit board, as in Figure 12. Although the pre-charge circuitry exists on both the -IN and -OUT side, the example in Figure 12 shows SCLIN and SDAIN connecting to the main bus. The supply voltage to V_{CC} can be applied early by ensuring that the VCC and GND pin contacts are physically longer than the contacts for the SCLIN and SDAIN pins. If a voltage supervisor will also be used to control the voltage supply on the add-on card, additional delay will exist before the 1 V pre-charge voltage is present on the SCL and SDA pins.

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA4311A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCA4311A as possible. These best practices are shown in Figure 16.

The layout example provided in Figure 16 shows a 4 layer board, which is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, shown in Figure 16 for the V_{CC} side of the resistor connected to the EN pin; however, this routing and via is not necessary if V_{CC} and GND are both full planes as opposed to the partial planes depicted.

11.2 Layout Example

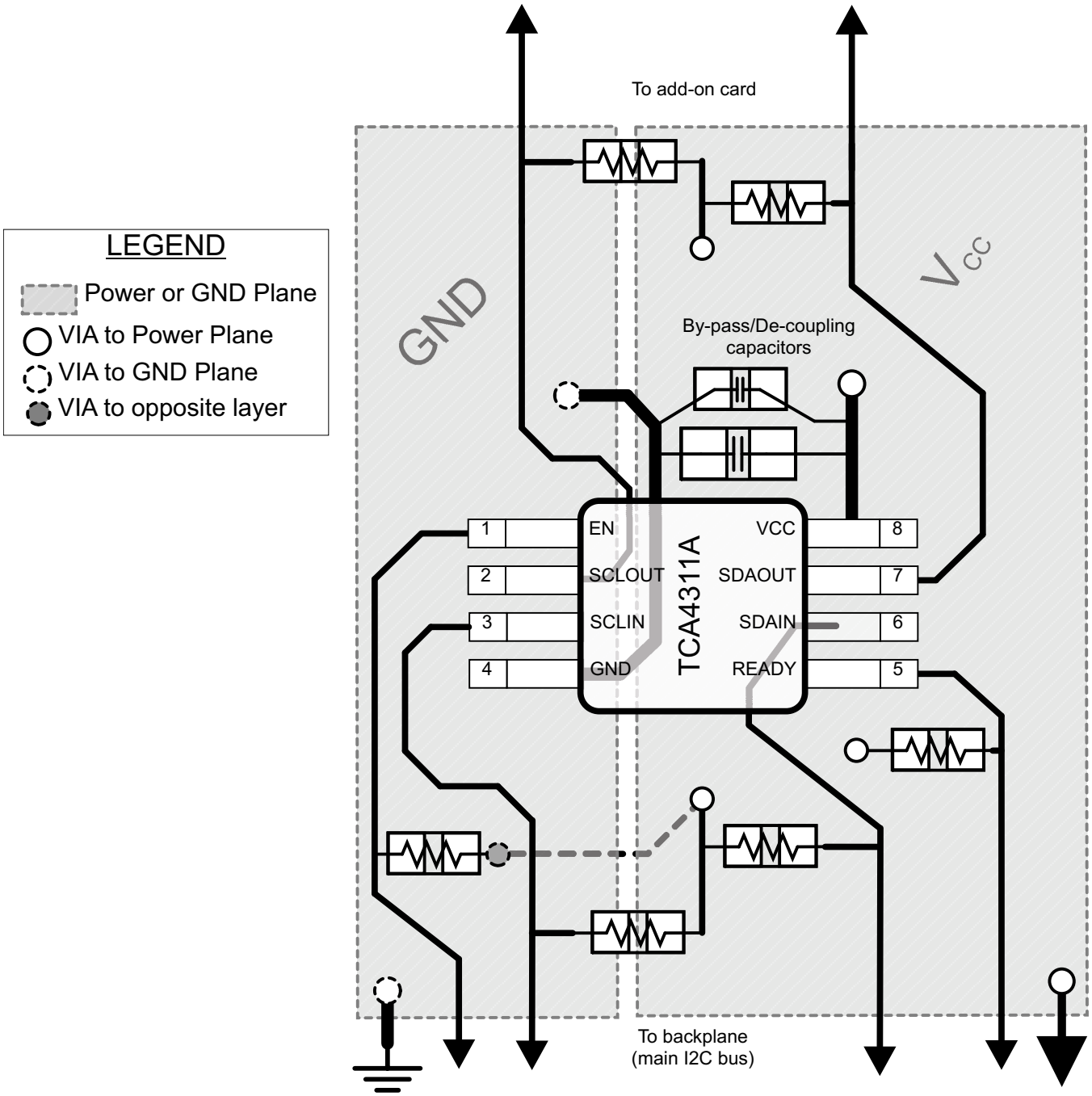


Figure 16. Package Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.3 商标

E2E is a trademark of Texas Instruments.
CompactPCI is a trademark of PCI Industrial Computer Manufacturers Group.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA4311ADGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6KA, 6KF, 6KS, 6KU) (6K6, 6KE)
TCA4311ADGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6KA, 6KF, 6KS, 6KU) (6K6, 6KE)
TCA4311ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PR311A
TCA4311ADR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PR311A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

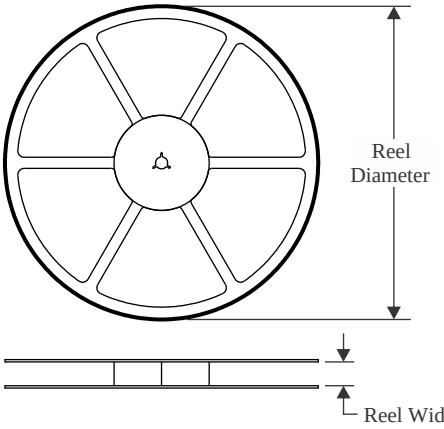
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

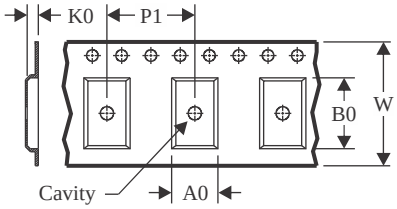
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

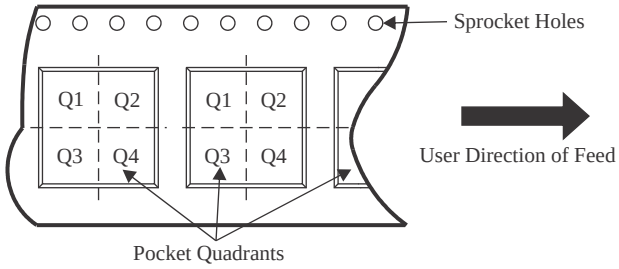


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

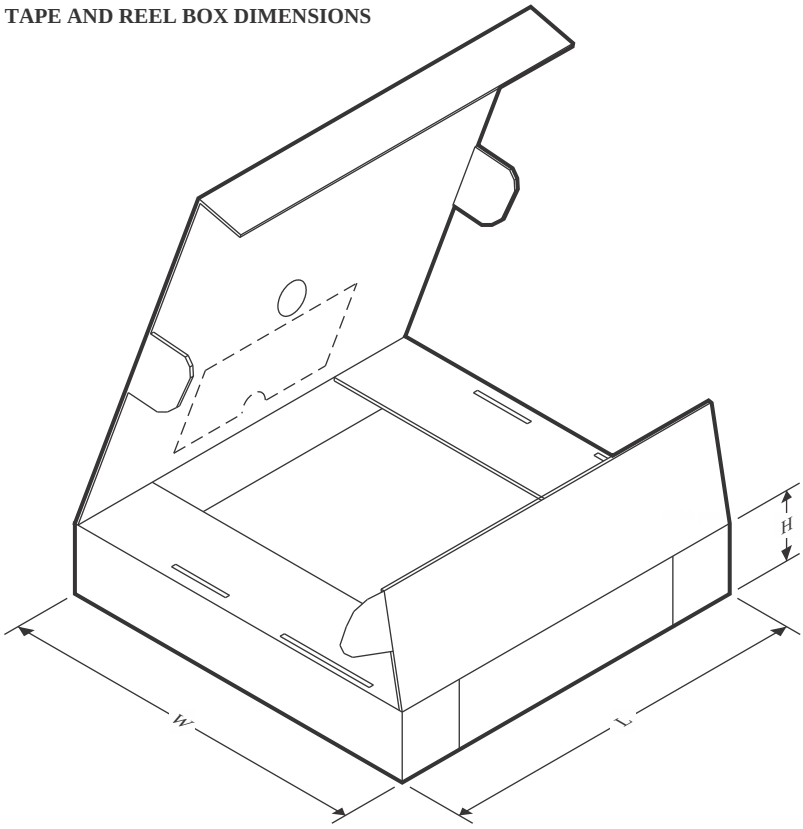
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA4311ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA4311ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

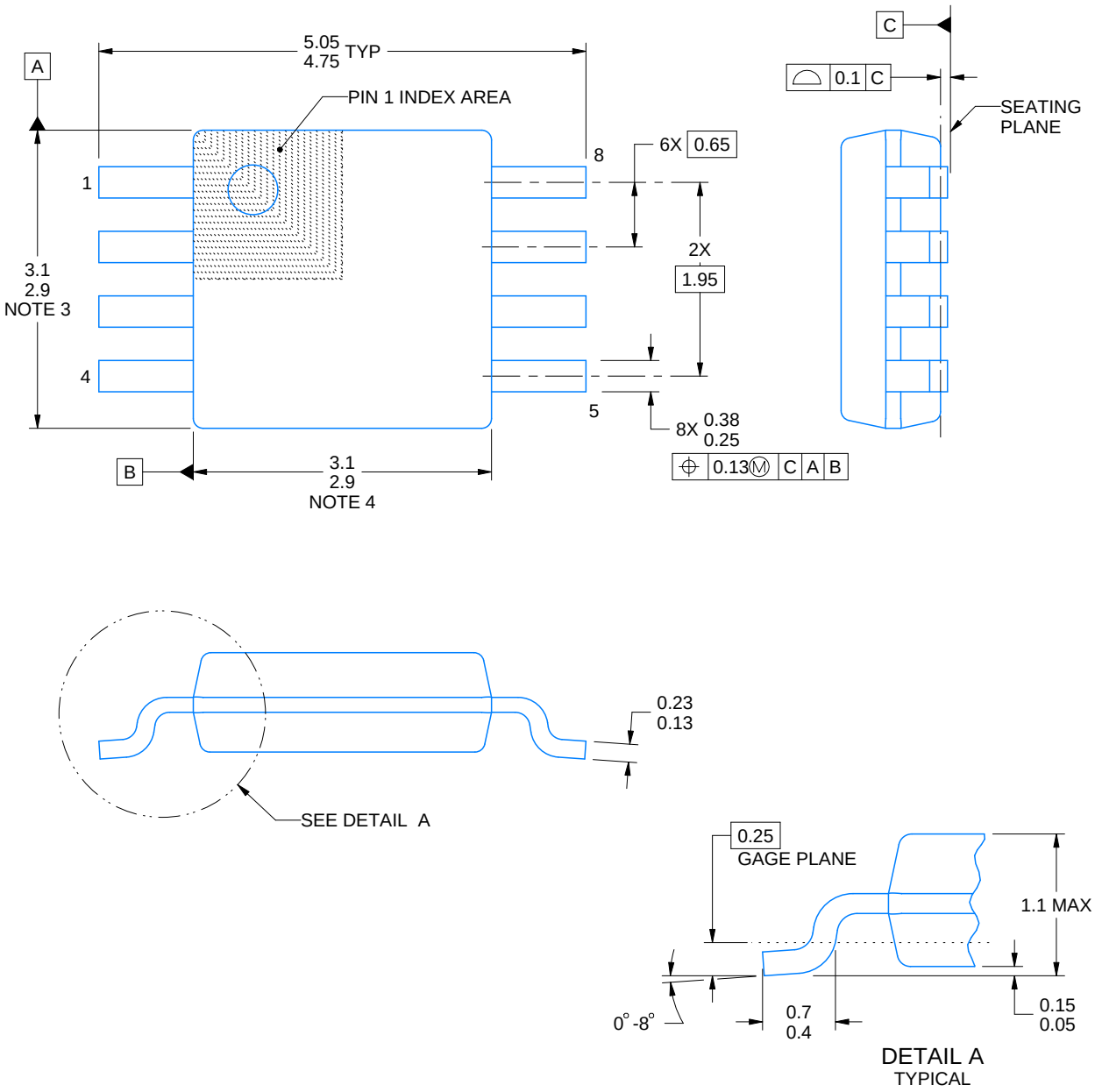
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA4311ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TCA4311ADR	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

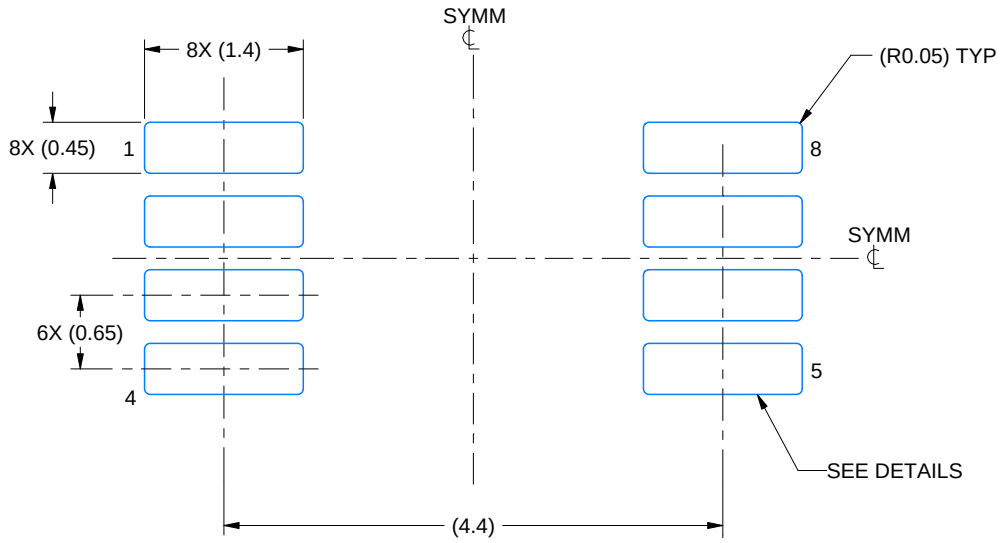
SMALL OUTLINE PACKAGE



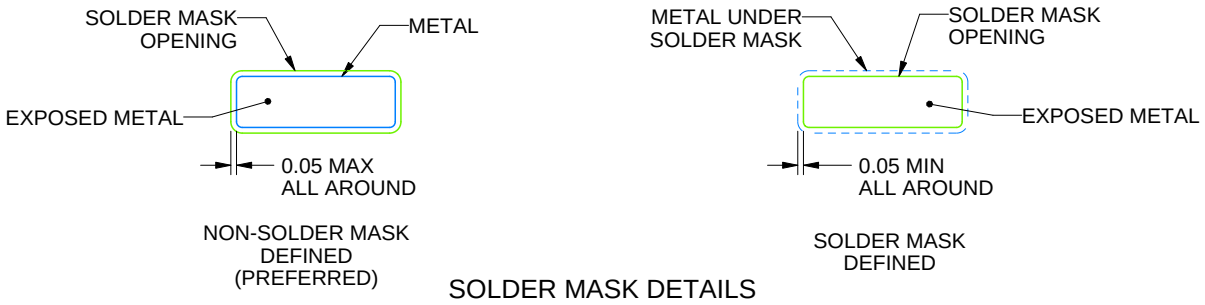
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

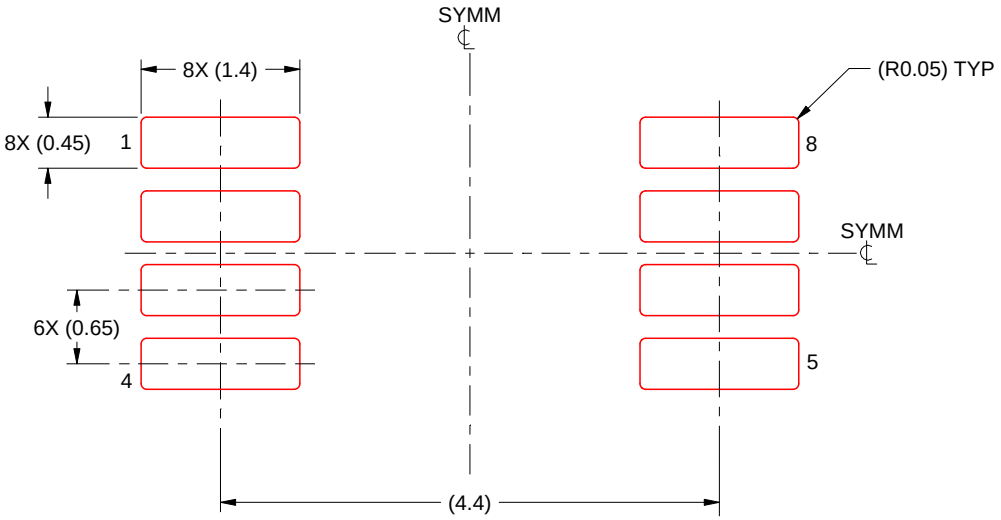


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

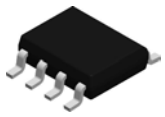


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

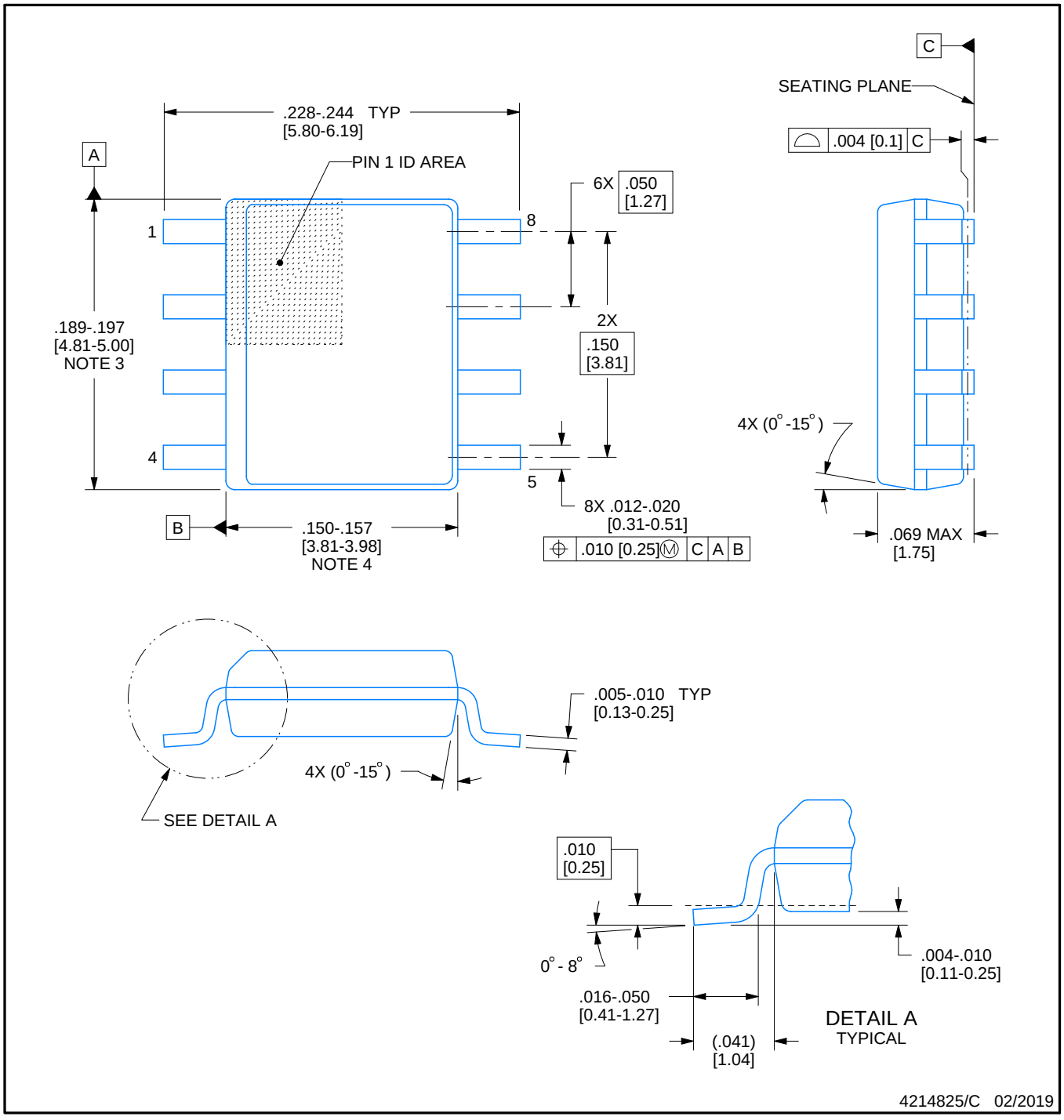


PACKAGE OUTLINE

D0008A

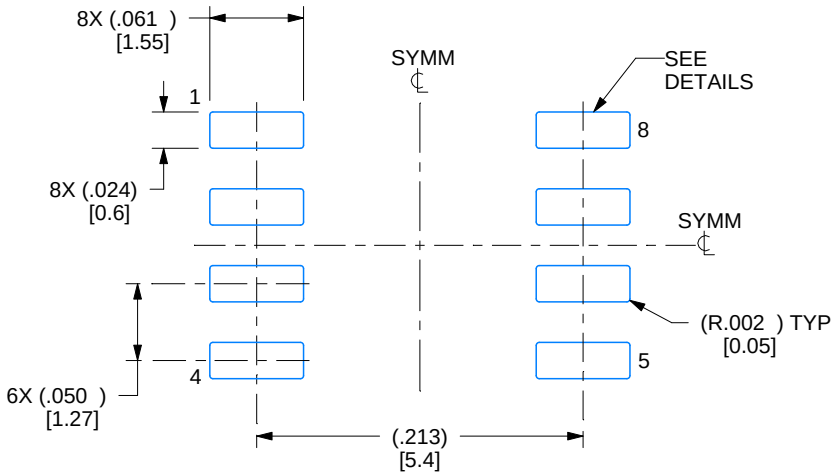
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

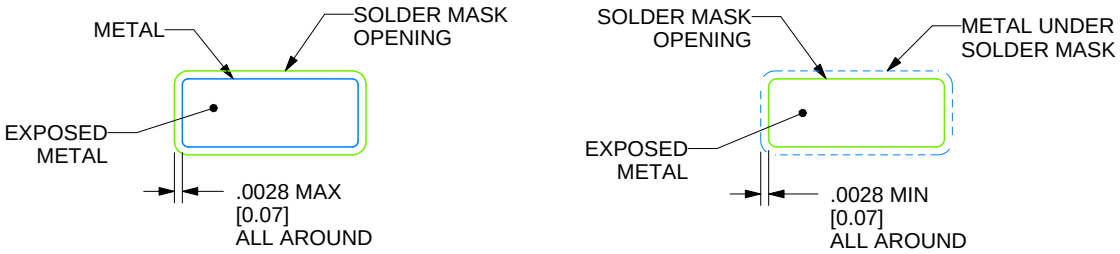


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

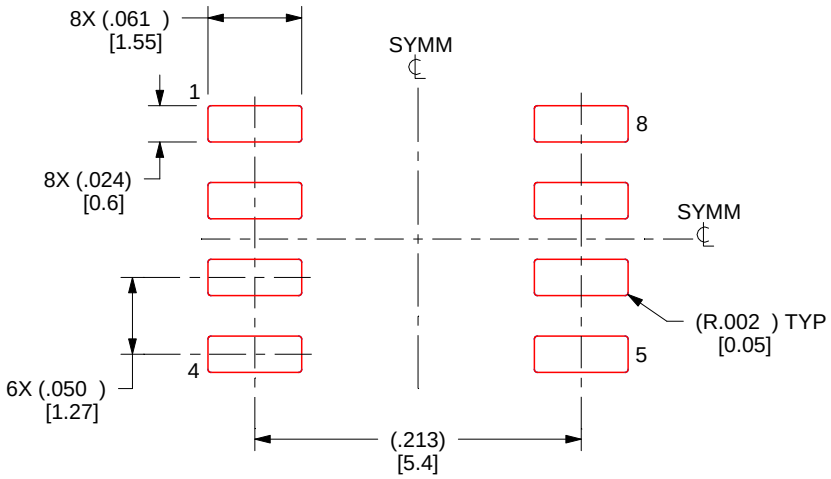
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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