TAS2572 6.6 W Digital Input smart amp with I/V sense and integrated 13 V Class-H Boost

1 Features

- Powerful class-D amplifier
  - 6.6 W 1% THD+N
  - 13V boost with 4.0A max current limit
- Best in class efficiency
  - Upto 90% efficiency at system level
  - 4.8mW idle channel power
  - Integrated Y-bridge
  - Advanced 33mV step size class-H boost
- High performance audio channel
  - 7µV A-wt. idle channel noise
  - 109dB Dynamic Range
  - -90dB THDN
  - Low EMI performance
- Advanced integrated features
  - Integrated Speaker IV sense
  - Signal detection high efficiency modes
  - High accuracy voltage monitor & temp sensor
  - Programmable battery input current limit
- Ease of use features
  - 1cell, 2cell and 3cell Li-ion battery support
  - Clock based power up/down
  - Auto clock rate detection: 16kHz to 192kHz
  - Integrated ultrasonic tone generator
  - External 14V PVDD supply support
  - MCLK free operation
  - Thermal and over current protection
  - Programmable drive strength IO buffers
- Power Supplies and user interface
  - VBAT: 2.5 V to 5.5 V
  - VDD: 1.65 V to 1.95 V
  - IOVDD: 1.2V or 1.8V
  - I^2S/TDM: 8 channels
  - I^2C: 4 selectable addresses
- WCSP package

2 Applications

- Mobile phone, Tablets & Wearables
- Smart Speakers with Voice Assistance
- Bluetooth and Wireless speakers

3 Description

The TAS2572 is a digital input Class-D audio amplifier with an integrated Boost for higher power delivery in battery-operated systems. The device has integrated speaker voltage and current sense (IV-Sense) for real-time monitoring of the loudspeakers. IV-sense data can be used to run speaker protection algorithms on a host DSP to enable high output SPL while keeping speakers in a safe operating region.

The device is optimized for delivering the best battery life for real use cases of Music playback and Voice calls. Advanced efficiency optimization features like Class-H, Y-bridge and algorithms enable the device to produce best-in-class efficiency across all power regions of operation. The Class-D amplifier is capable of delivering 6.6 W output power using the integrated Class-H 13 V Boost.

A battery tracking peak voltage limiter and a battery voltage monitor ADC enables advanced battery monitoring algorithms on the host processor to manage peak output power delivery while avoiding any audio distortion when battery capacity is depleting.

Up to four devices can share a common bus via I^2S/TDM + I^2C interfaces.

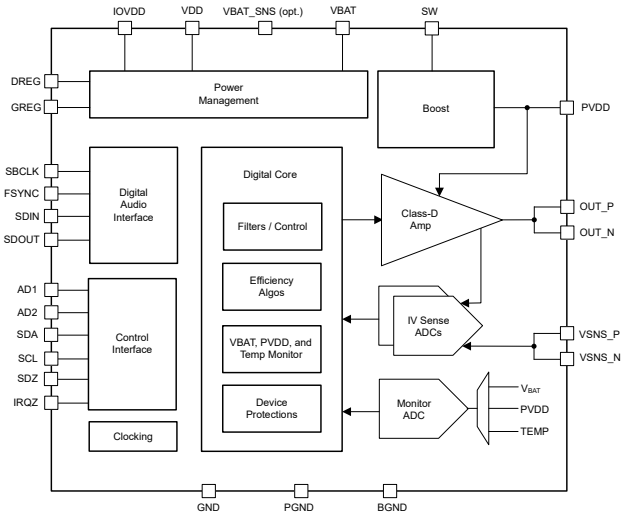


Figure 3-1. Functional block diagram

Table of Contents

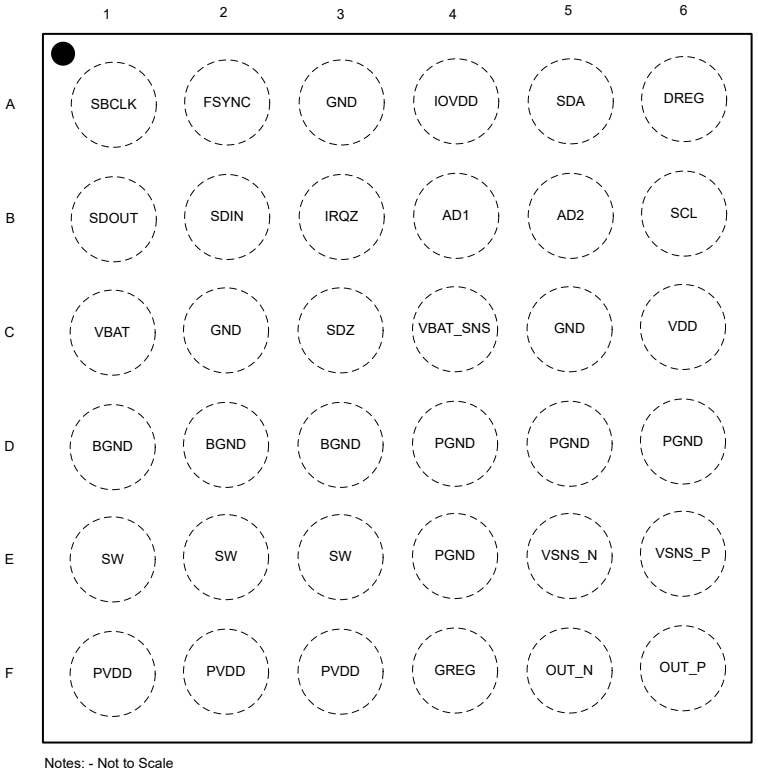
1 Features.....1
2 Applications.....1
3 Description.....1
4 Revision History.....2
5 Pin Configuration and Functions.....2

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
Nov, 2022	v0.1	Initial Release

5 Pin Configuration and Functions



Notes: - Not to Scale

Figure 5-1. Package Top Level View Pinout

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
AD1	B4	I	I²C address pin LSB.
AD2	B5	I	I²C address pin LSB+1.
BGND	D1	P	Boost ground. Connect to PCB GND plane strongly with multiple vias.
	D2		
	D3		
DREG	A6	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.
FSYNC	A2	I	I²S word clock or TDM frame sync.
GREG	F4	P	High-side gate CP regulator output. Do not connect to external load.
GND	A3	P	Digital ground. Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.
	C2		
	C5		
IOVDD	A4	P	1.2-V or 1.8-V Digital IO supply. Decouple to GND with capacitor.
IRQZ	B3	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.
OUT_N	F5	O	Class-D negative output.
OUT_P	F6	O	Class-D positive output.
PGND	D4	P	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
	D5		
	D6		
	E4		
PVDD	F1	P	Integrated boost output and Class-D power stage supply.
	F2		
	F3		
SBCLK	A1	I	I²S/TDM serial bit clock.
SCL	B6	I	I²C Clock Pin. Pull up to IOVDD with a resistor.
SDA	A5	IO	I²C Data Pin. Pull up to IOVDD with a resistor.
SDIN	B2	I	I²S or TDM serial data input.
SDOUT	B1	IO	I²S or TDM serial data output.
SDZ	C3	I	Active low hardware shutdown.
SW	E1	P	Boost converter switch input.
	E2		
	E3		
VBAT	C1	P	Battery power supply input. Connect to 2.5-V to 5.5-V supply and decouple with a cap.
VBAT_SNS	C4	I	Battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.
VDD	C6	P	Analog, digital power supply. Connect to 1.8-V supply and decouple to GND with cap.
VSNS_N	E5	I	Voltage sense negative input. Connect to speaker negative terminal as close to speaker as possible. Add series resistor if EMI filter is used.
VSNS_P	E6	I	Voltage sense positive input. Connect to speaker positive terminal as close to speaker as possible. Add series resistor if EMI filter is used.

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS2572YCGR	Active	Production	DSBGA (YCG) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS257X
TAS2572YCGR.A	Active	Production	DSBGA (YCG) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS257X

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

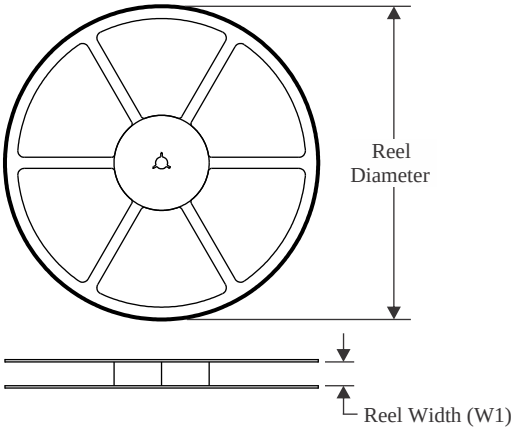
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

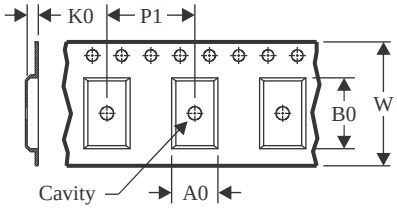
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

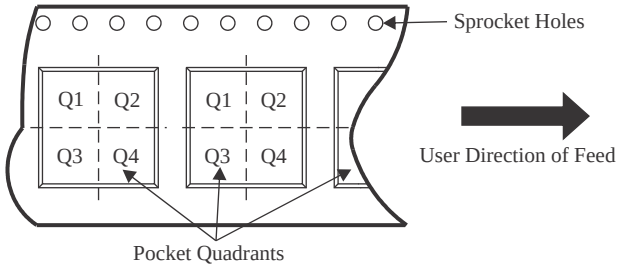


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

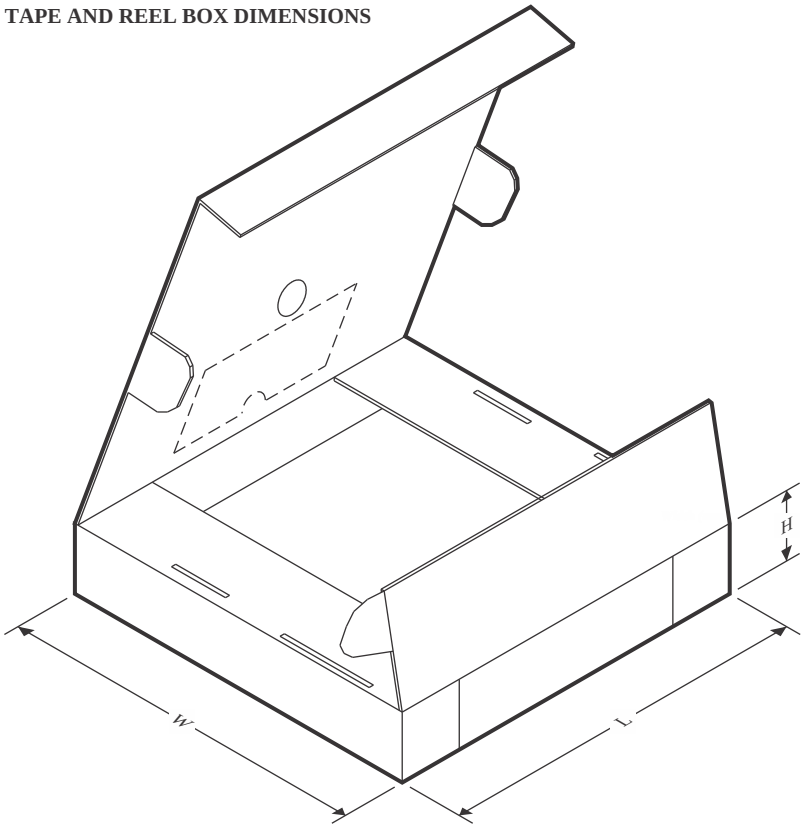
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2572YCGR	DSBGA	YCG	36	3000	180.0	8.4	2.4	2.4	0.62	4.0	8.0	Q1
TAS2572YCGR	DSBGA	YCG	36	3000	180.0	8.4	2.4	2.4	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2572YCGR	DSBGA	YCG	36	3000	182.0	182.0	20.0
TAS2572YCGR	DSBGA	YCG	36	3000	182.0	182.0	20.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265