

# SN54LVTH126, SN74LVTH126 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS746B – JULY 2000 - REVISED OCTOBER 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

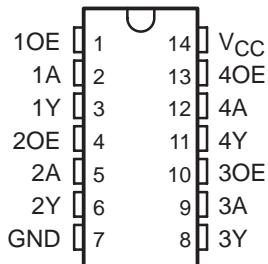
## description/ordering information

These bus buffers are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

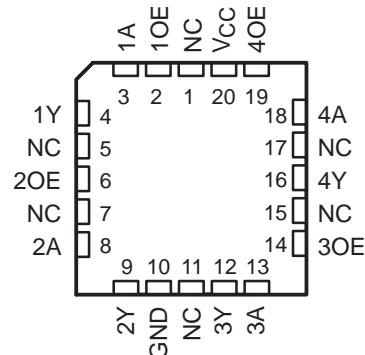
The 'LVTH126 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (OE) input is low.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**SN54LVTH126 . . . J OR W PACKAGE  
SN74LVTH126 . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)**



**SN54LVTH126 . . . FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube	SN74LVTH126D	LVTH126
		Tape and reel	SN74LVTH126DR	
	SOP – NS	Tape and reel	SN74LVTH126NSR	LVTH126
	SSOP – DB	Tape and reel	SN74LVTH126DBR	LXH126
	TSSOP – PW	Tube	SN74LVTH126PW	LXH126
		Tape and reel	SN74LVTH126PWR	
	TVSOP – DGV	Tape and reel	SN74LVTH126DGVR	LXH126
-55°C to 125°C	CDIP – J	Tube	SNJ54LVTH126J	SNJ54LVTH126J
	CFP – W	Tube	SNJ54LVTH126W	SNJ54LVTH126W
	LCCC – FK	Tube	SNJ54LVTH126FK	SNJ54LVTH126FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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SCBS746B – JULY 2000 - REVISED OCTOBER 2003

**description/ordering information (continued)**

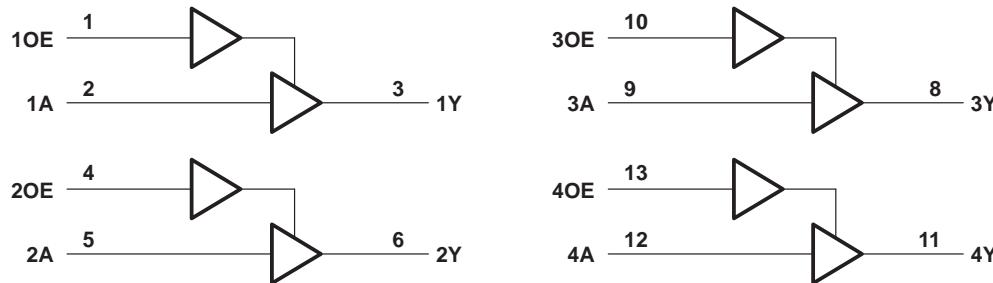
When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**FUNCTION TABLE  
(each buffer)**

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

**logic diagram (positive logic)**



# **SN54LVTH126, SN74LVTH126 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

SCBS746B – JULY 2000 - REVISED OCTOBER 2003

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	.....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	.....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH126	.....	96 mA
	SN74LVTH126	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH126	.....	48 mA
	SN74LVTH126	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	.....	86°C/W
	DB package	96°C/W
	DGV package	127°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

**recommended operating conditions (see Note 4)**

		SN54LVTH126		SN74LVTH126		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200	200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

**NOTE 4:** All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**PRODUCT PREVIEW** information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SCBS746B – JULY 2000 - REVISED OCTOBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVTH126			SN74LVTH126			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA		-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 µA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2				V
	V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA	2.4		2.4				
	V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -24 mA	2					
		I <sub>OH</sub> = -32 mA			2			
V <sub>OL</sub>	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 µA		0.2	0.2			V
		I <sub>OL</sub> = 24 mA		0.5	0.5			
	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA		0.4	0.4			
		I <sub>OL</sub> = 32 mA		0.5	0.5			
		I <sub>OL</sub> = 48 mA		0.55				
		I <sub>OL</sub> = 64 mA			0.55			
I <sub>I</sub>	V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		10		10			µA
	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		
	Data inputs	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = V <sub>CC</sub>	1		1		
			V <sub>I</sub> = 0	-5		-5		
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V				±100			µA
I <sub>I(hold)</sub>	Data inputs	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75		75		µA
			V <sub>I</sub> = 2 V	-75		-75		
		V <sub>CC</sub> = 3.6 V‡	V <sub>I</sub> = 0 to 3.6 V			±500		
I <sub>OZH</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V			5		5		µA
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V			-5		-5		µA
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care			±50*		±50		µA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care			±50*		±50		µA
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high	0.12	0.19	0.12	0.19		mA
		Outputs low	4.5	7	4.5	7		
		Outputs disabled	0.12	0.19	0.12	0.19		
ΔI <sub>CC</sub> §	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.3		0.2			mA
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0		4		4			pF
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0		6.5		6.5			pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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WITH 3-STATE OUTPUTS**

SCBS746B – JULY 2000 - REVISED OCTOBER 2003

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH126				SN74LVTH126				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	4.8		5.5	1	2.3	3.8		4.5	ns
$t_{PHL}$			1	4.9		5.4	1	2.4	3.9		4.4	
$t_{PZH}$	OE	Y	1	6.4		7.1	1	3.6	5.4		6.1	ns
$t_{PZL}$			1.1	6.2		6.8	1.1	3.6	5.2		5.8	
$t_{PHZ}$	OE	Y	1	4.8		5.3	1	2.2	3.8		4.3	ns
$t_{PLZ}$			1.3	6.5		7.1	1.3	3.6	5.5		6.1	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

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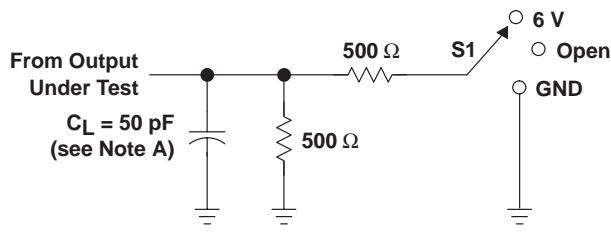


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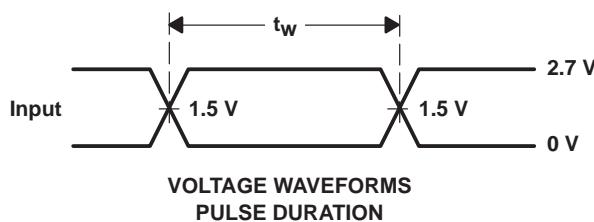
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**PARAMETER MEASUREMENT INFORMATION**

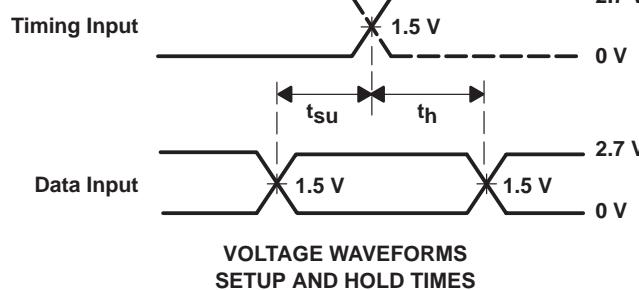


LOAD CIRCUIT

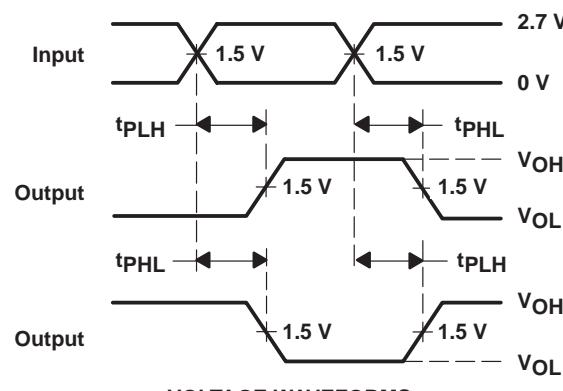


VOLTAGE WAVEFORMS  
PULSE DURATION

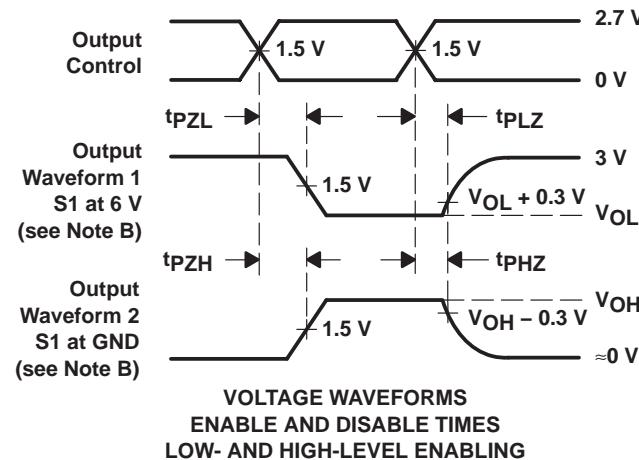
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<b>SN74LVTH126D</b>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126D.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
<b>SN74LVTH126DBR</b>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DBR.B	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
<b>SN74LVTH126DGVR</b>	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVR.B	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVRG4	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVRG4.B	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
<b>SN74LVTH126DR</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DRG4.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
<b>SN74LVTH126NSR</b>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSR.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSRG4	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSRG4.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
<b>SN74LVTH126PW</b>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
<b>SN74LVTH126PWR</b>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

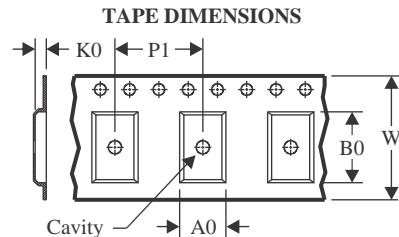
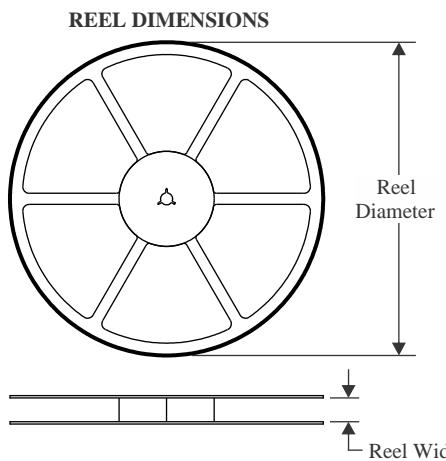
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

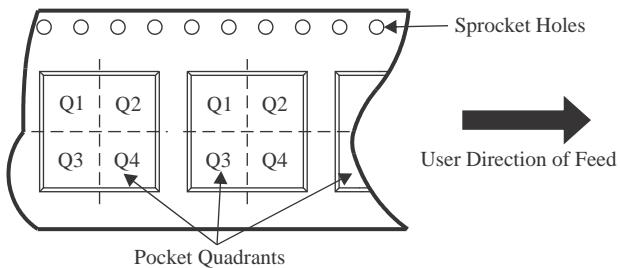
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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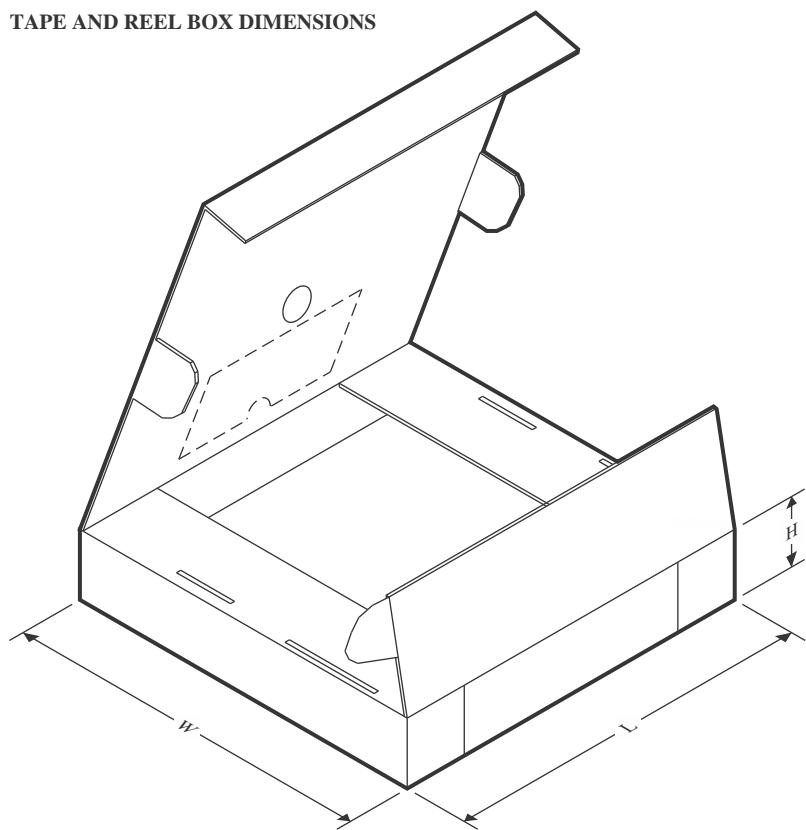
**TAPE AND REEL INFORMATION**

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

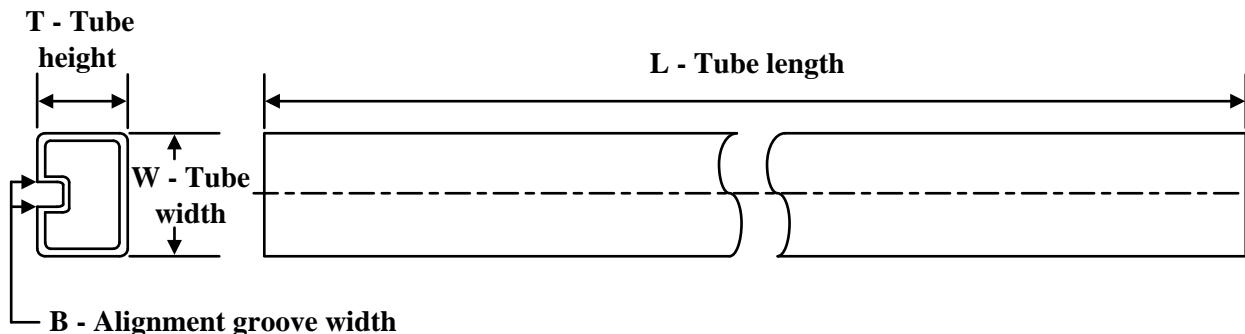
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVTH126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH126DGVRG4	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVTH126DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVTH126NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVTH126NSRG4	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVTH126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH126DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVTH126DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH126DGVRG4	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH126DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVTH126DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVTH126NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVTH126NSRG4	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVTH126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

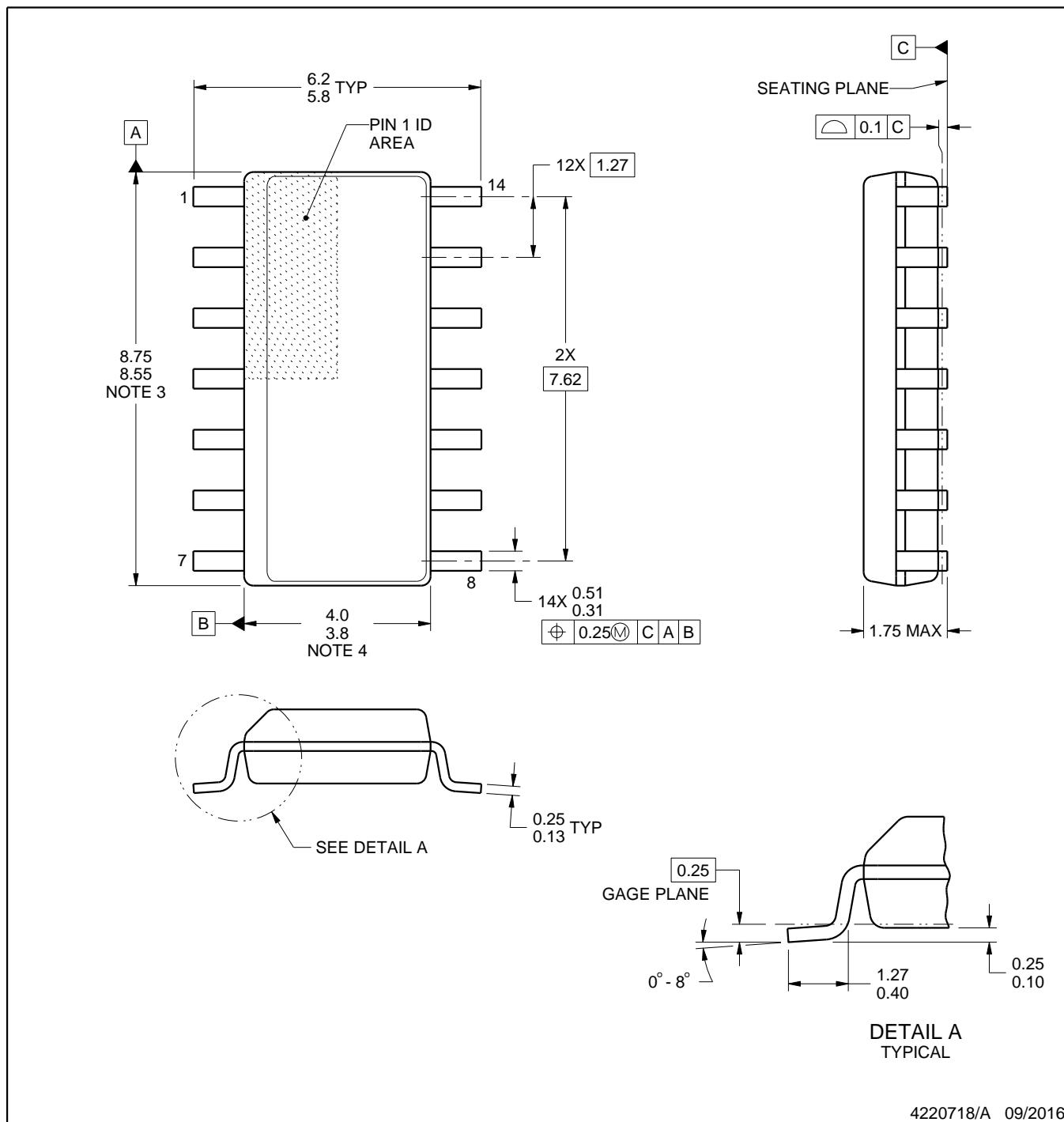
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
SN74LVTH126D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH126D.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH126PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVTH126PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

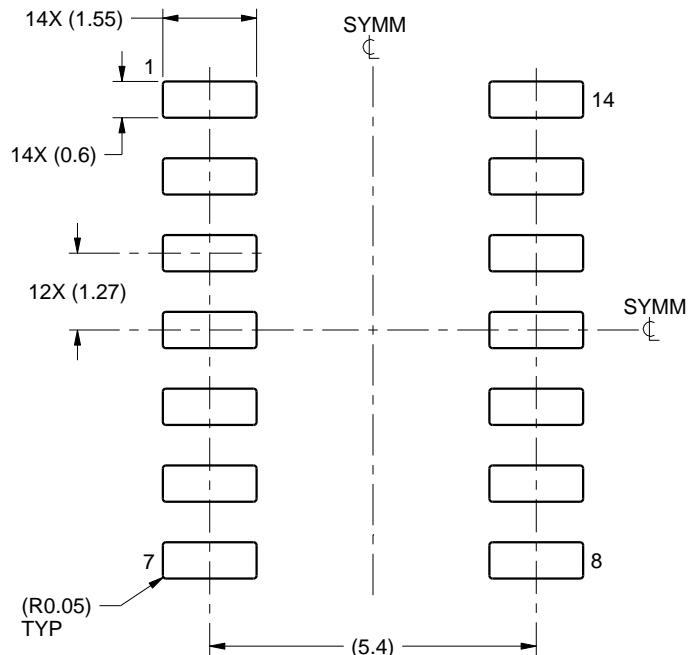
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

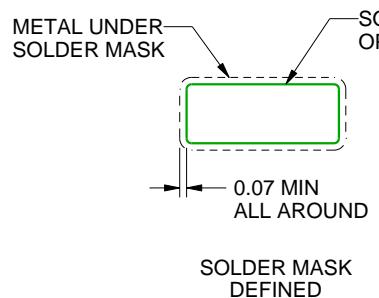
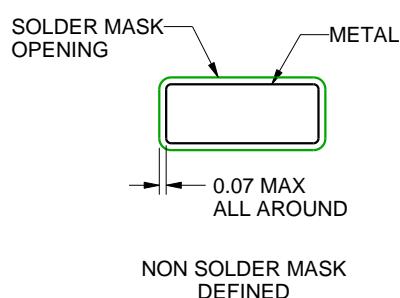
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

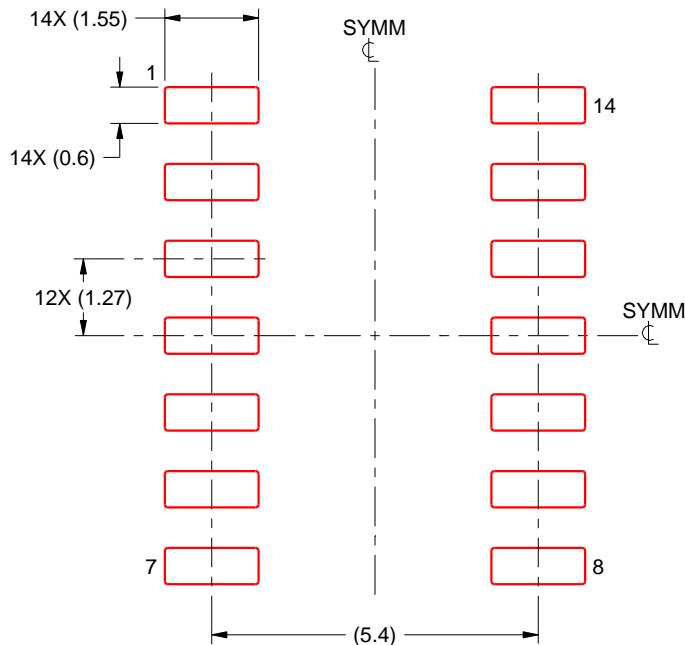
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

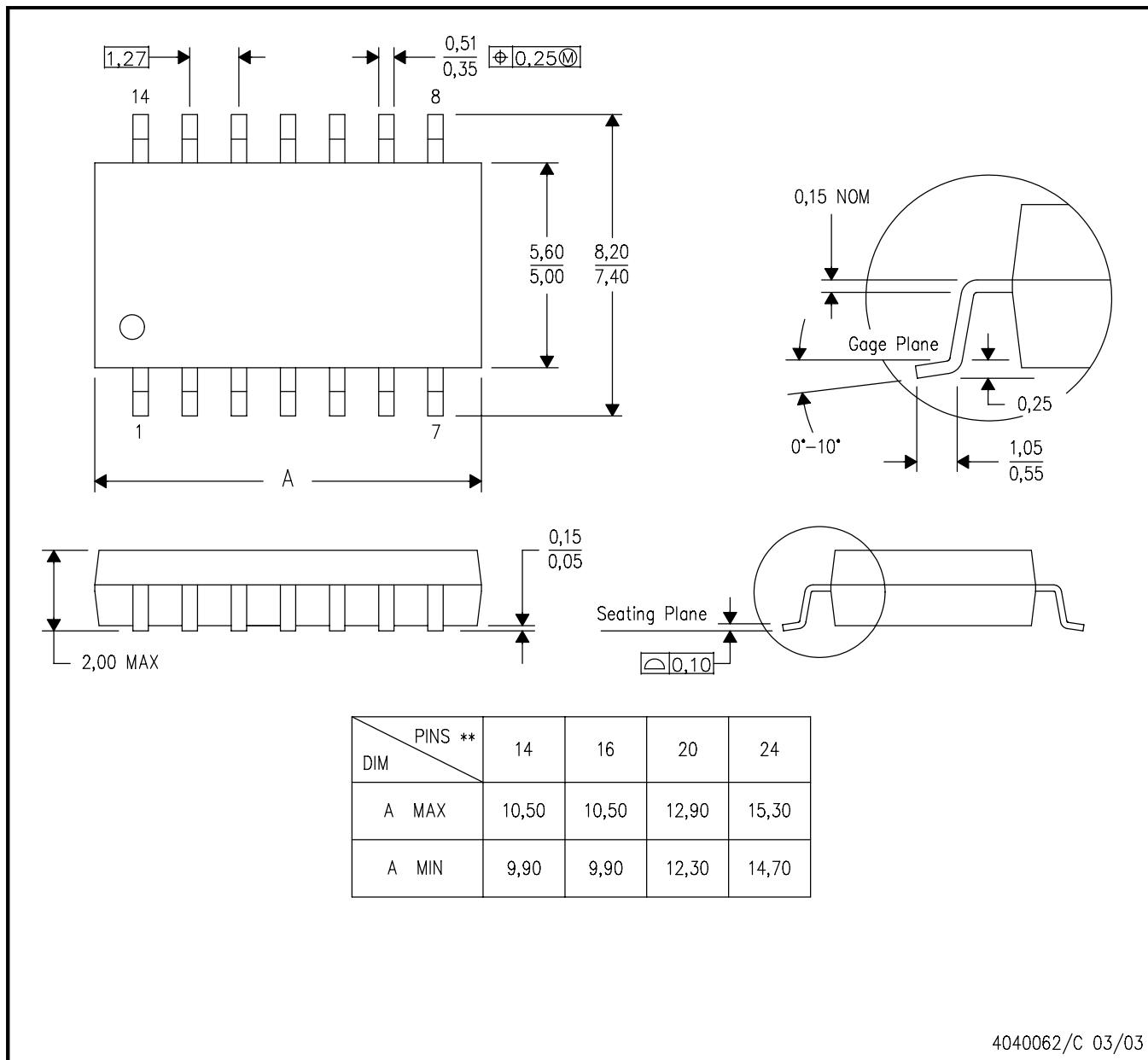
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

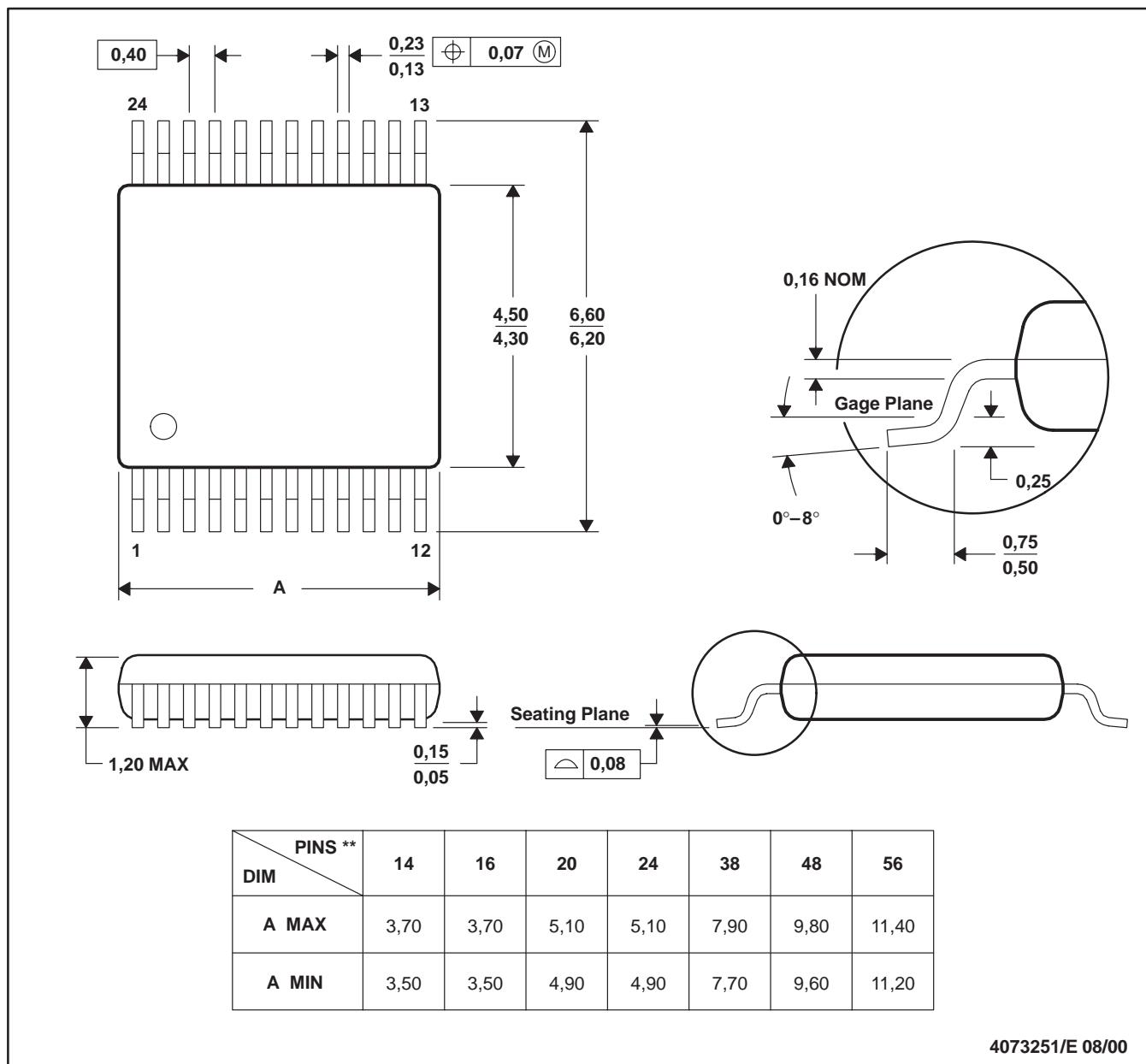


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

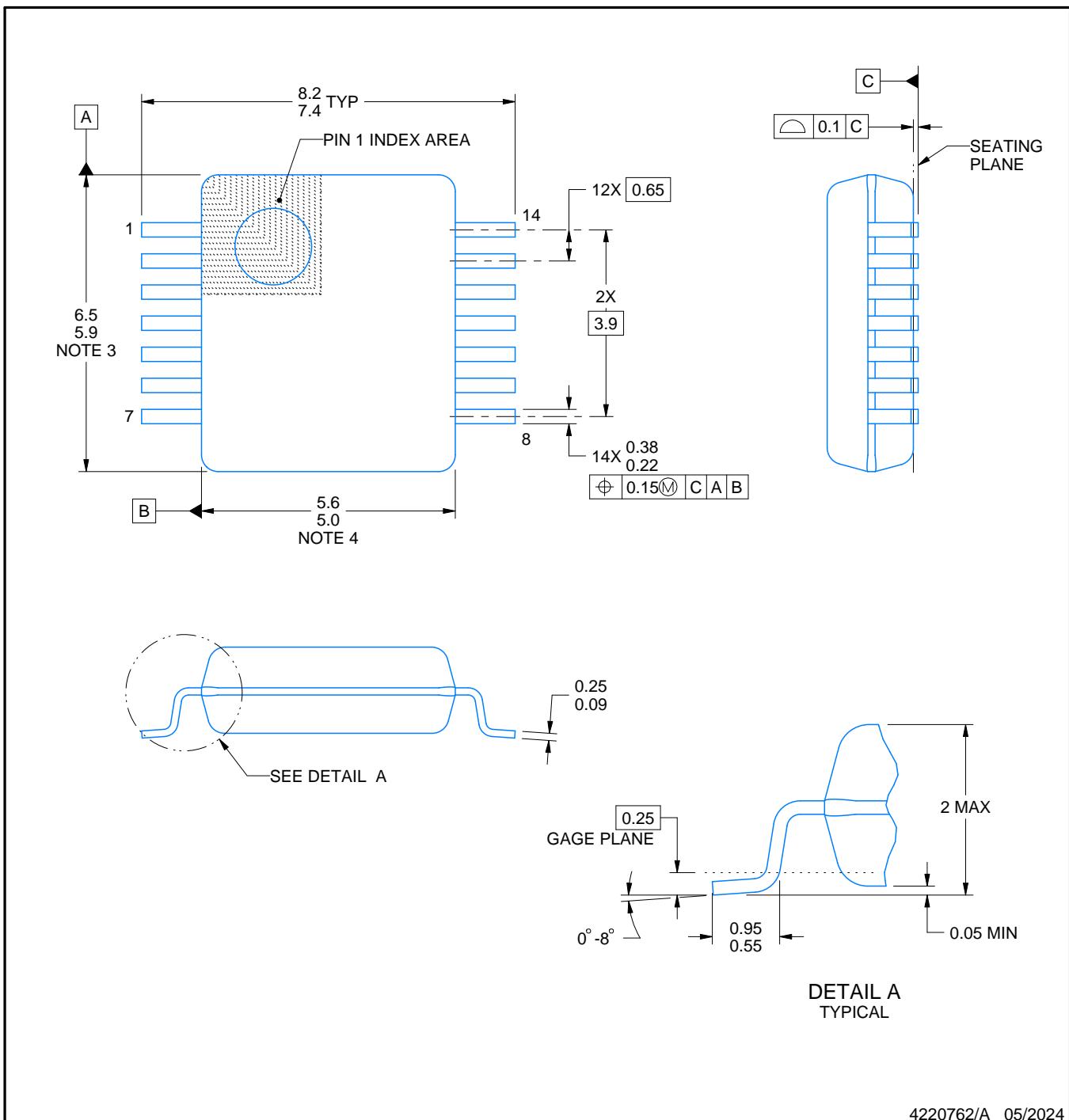


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
  - D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

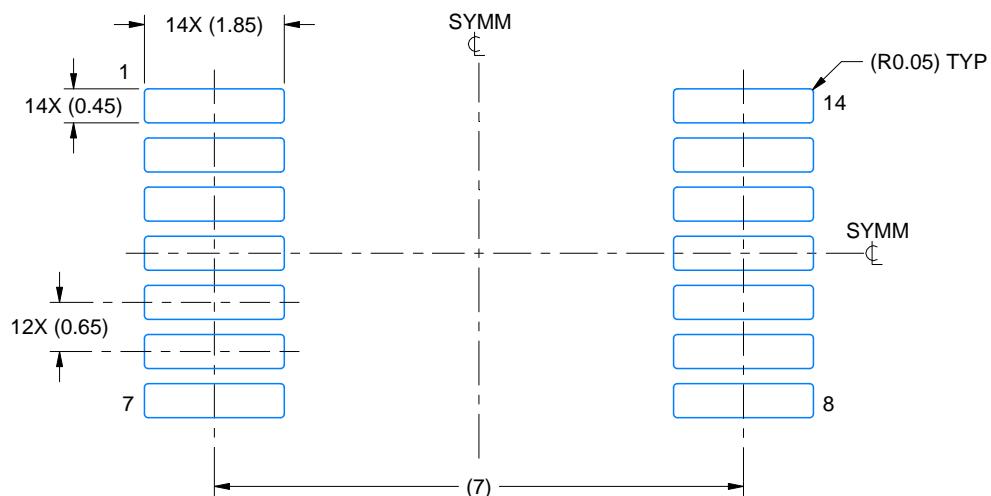
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

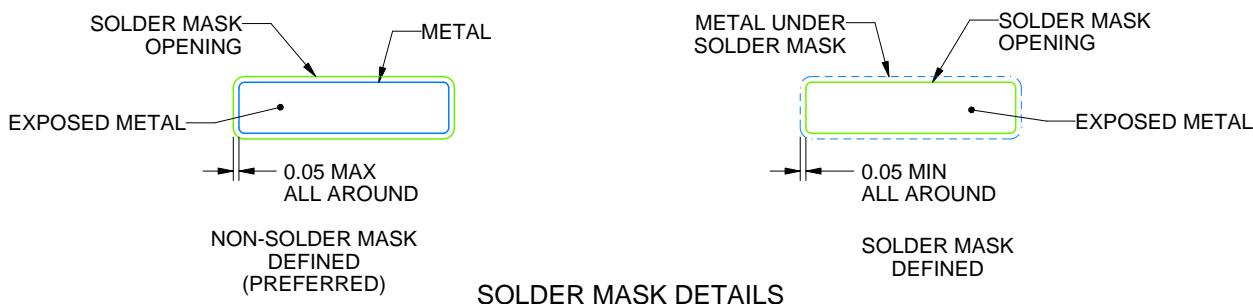
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

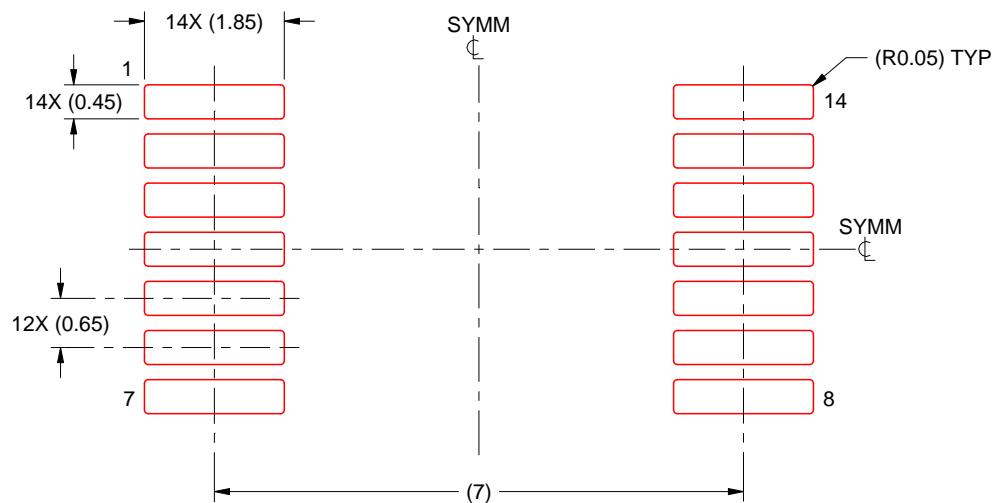
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

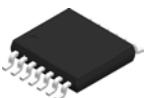
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

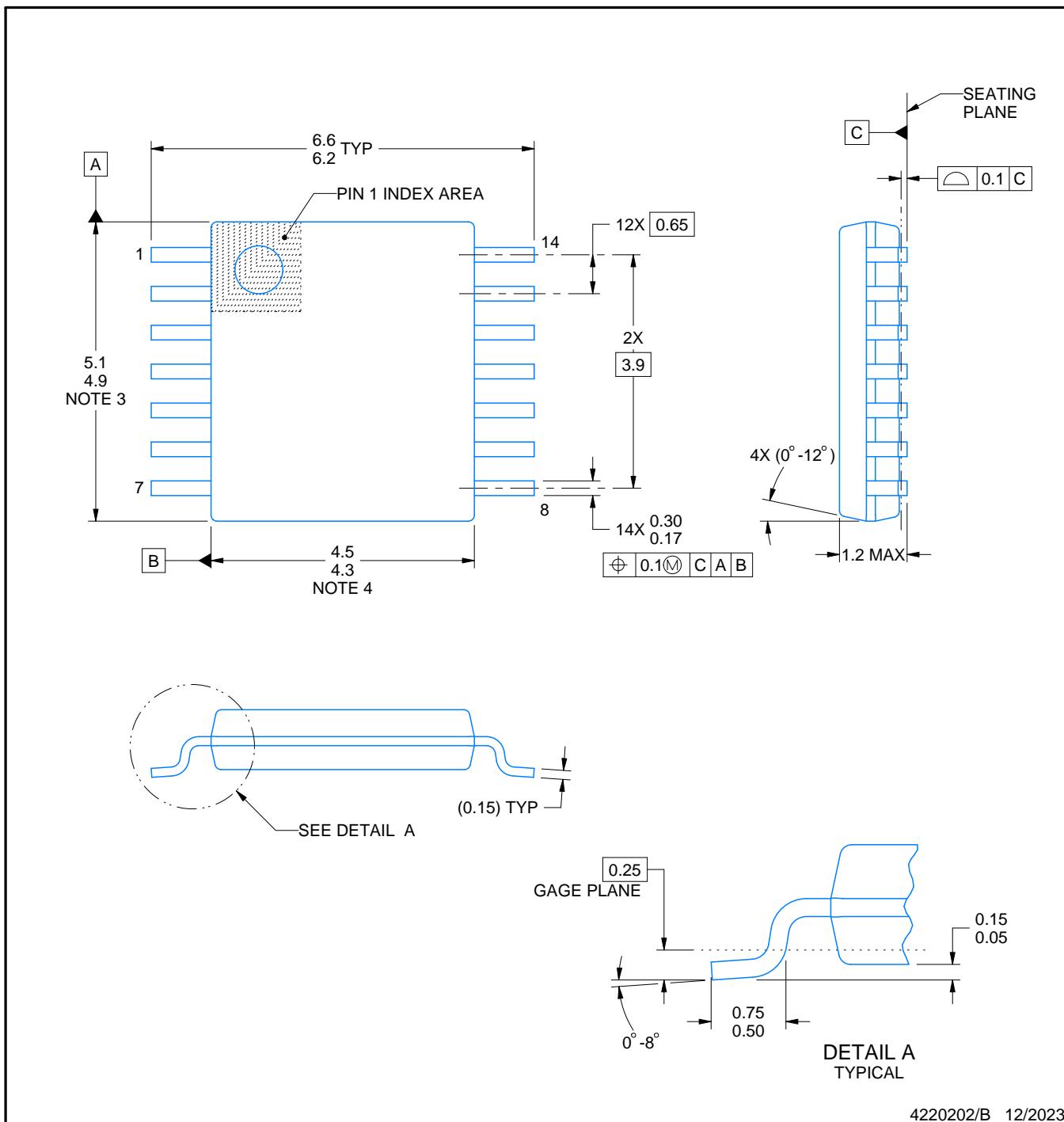
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

## NOTES:

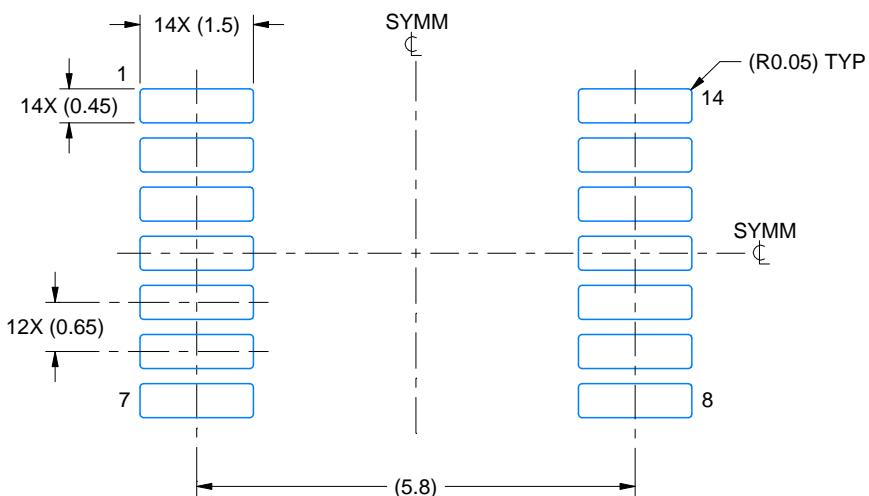
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

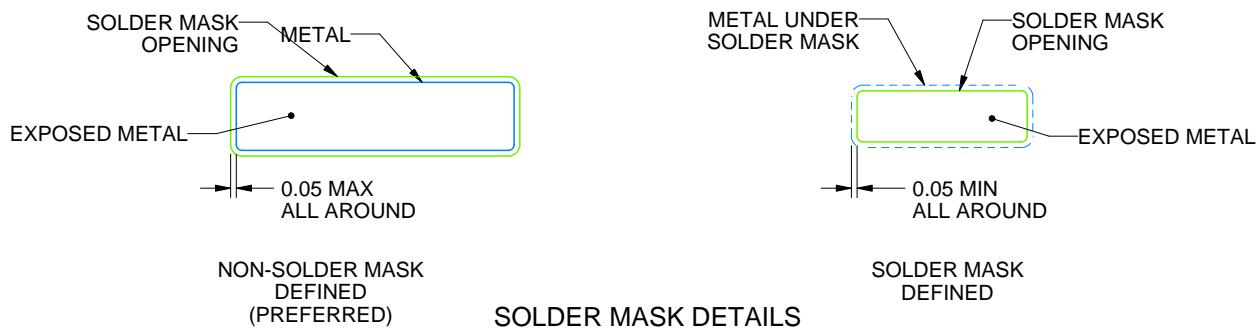
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

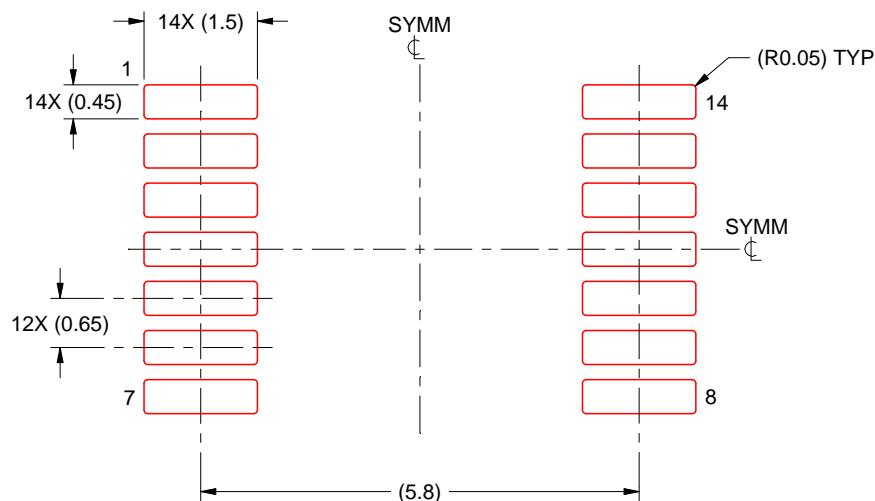
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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