具有三态输出的 SN74LVCH32373A 32 位透明 D 型锁存器

1 特性

- 德州仪器 (TI) Widebus+™ 系列产品
- 工作电压范围为 1.65V 至 3.6V
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4.2ns
- V_{OLP}（输出接地反弹）典型值小于 0.8V（V_{CC} = 3.3V、T_A = 25°C 时）
- V_{OHV}（输出 V_{OH} 下冲）典型值大于 2V（V_{CC} = 3.3V、T_A = 25°C 时）
- I_{off} 支持局部断电模式运行
- 支持混合模式信号运行（5V 输入或输出电压，具有 3.3V V_{CC}）
- 总线保持数据输入消除了对外部上拉/下拉电阻的需求
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)

2 应用

- 缓冲寄存器
- I/O 端口
- 双向总线驱动器
- 工作寄存器

3 说明

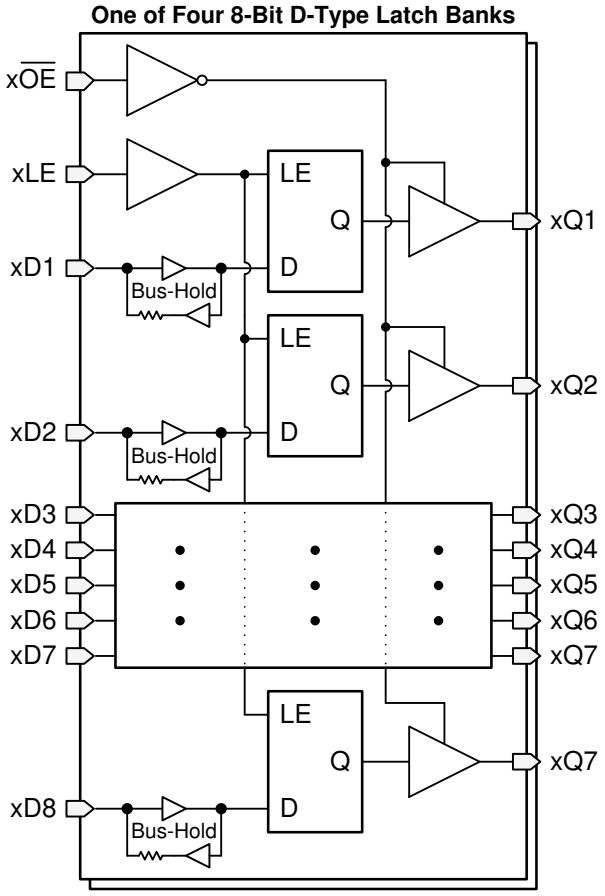
这款 32 位透明 D 型锁存器旨在 1.65V 至 3.6V V_{CC} 下运行。

SN74LVCH32373A 特别适合于实现缓冲寄存器、I/O 端口、双向总线驱动器和工作寄存器。它可以用作四个 8 位锁存器、两个 16 位锁存器或一个 32 位锁存器。在锁存器使能 (LE) 输入为高电平时，Q 输出将跟随数据 (D) 输入。当 LE 为低电平时，Q 输出被锁存在 D 输入端设置的电平。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN74LVCH32373AGKER	LFBGA-GKE	13.50mm × 5.00mm
SN74LVCH32373ANMJR	LFBGA-NMJ	13.50mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图

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• 全局更改为新的 TI 数据表格式	1
• 添加了“应用”列表、“器件信息”表和重要图形	1
• Added maximum junction temperature	7
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• Added Thermal Information section	8
• Added Typical Characteristics section	10
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5 Pin Configuration and Functions

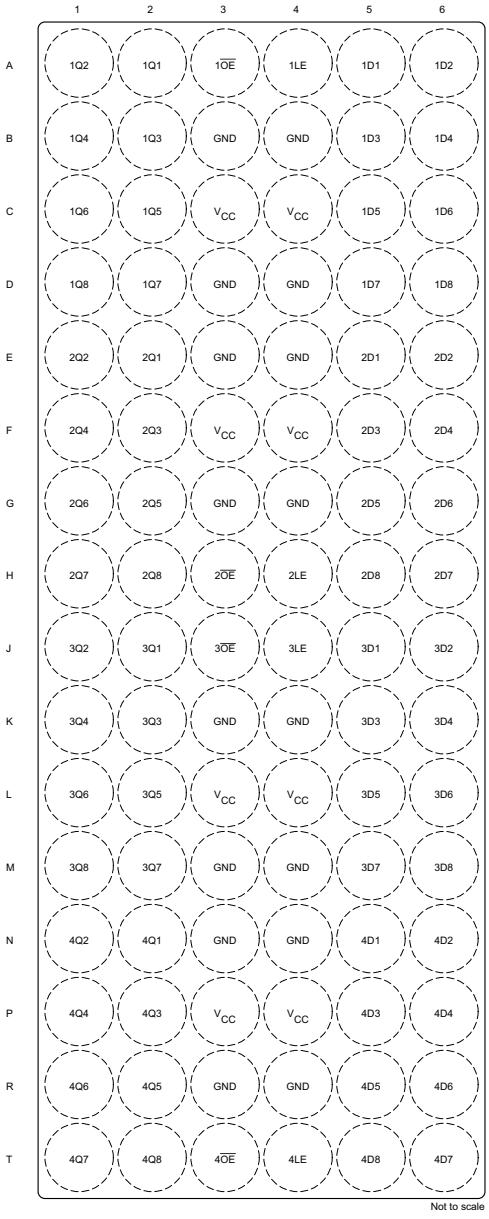


图 5-1. GKE 96-Pin LFBGA Transparent Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1Q2	A1	Output	Bank 1, Channel 2, Q Output
1Q4	B1	Output	Bank 1, Channel 4, Q Output
1Q6	C1	Output	Bank 1, Channel 6, Q Output
1Q8	D1	Output	Bank 1, Channel 8, Q Output
2Q2	E1	Output	Bank 2, Channel 2, Q Output
2Q4	F1	Output	Bank 2, Channel 4, Q Output
2Q6	G1	Output	Bank 2, Channel 6, Q Output

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
2Q7	H1	Output	Bank 2, Channel 8, Q Output
3Q2	J1	Output	Bank 3, Channel 2, Q Output
3Q4	K1	Output	Bank 3, Channel 4, Q Output
3Q6	L1	Output	Bank 3, Channel 6, Q Output
3Q8	M1	Output	Bank 3, Channel 8, Q Output
4Q2	N1	Output	Bank 4, Channel 2, Q Output
4Q4	P1	Output	Bank 4, Channel 4, Q Output
4Q6	R1	Output	Bank 4, Channel 6, Q Output
4Q7	T1	Output	Bank 4, Channel 8, Q Output
1Q1	A2	Output	Bank 1, Channel 1, Q Output
1Q3	B2	Output	Bank 1, Channel 3, Q Output
1Q5	C2	Output	Bank 1, Channel 5, Q Output
1Q7	D2	Output	Bank 1, Channel 7, Q Output
2Q1	E2	Output	Bank 2, Channel 1, Q Output
2Q3	F2	Output	Bank 2, Channel 3, Q Output
2Q5	G2	Output	Bank 2, Channel 5, Q Output
2Q8	H2	Output	Bank 2, Channel 7, Q Output
3Q1	J2	Output	Bank 3, Channel 1, Q Output
3Q3	K2	Output	Bank 3, Channel 3, Q Output
3Q5	L2	Output	Bank 3, Channel 5, Q Output
3Q7	M2	Output	Bank 3, Channel 7, Q Output
4Q1	N2	Output	Bank 4, Channel 1, Q Output
4Q3	P2	Output	Bank 4, Channel 3, Q Output
4Q5	R2	Output	Bank 4, Channel 5, Q Output
4Q8	T2	Output	Bank 4, Channel 7, Q Output
1 $\overline{OE}$	A3	Input	Bank 1, Output Enable, Active Low
GND	B3	—	Ground
V_{CC}	C3	—	Positive Supply
GND	D3	—	Ground
GND	E3	—	Ground
V_{CC}	F3	—	Positive Supply
GND	G3	—	Ground
2 $\overline{OE}$	H3	Input	Bank 2, Output Enable, Active Low
3 $\overline{OE}$	J3	Input	Bank 3, Output Enable, Active Low
GND	K3	—	Ground
V_{CC}	L3	—	Positive Supply
GND	M3	—	Ground
GND	N3	—	Ground
V_{CC}	P3	Input	Positive Supply
GND	R3	—	Ground
4 $\overline{OE}$	T3	Input	Bank 4, Output Enable, Active Low
1LE	A4	Input	Bank 1, Latch Enable, Active Low
GND	B4	—	Ground
V_{CC}	C4	—	Positive Supply

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D4	—	Ground
GND	E4	—	Ground
V_{CC}	F4	—	Positive Supply
GND	G4	—	Ground
2LE	H4	Input	Bank 2, Latch Enable, Active Low
3LE	J4	Input	Bank 3, Latch Enable, Active Low
GND	K4	—	Ground
V_{CC}	L4	—	Positive Supply
GND	M4	—	Ground
GND	N4	—	Ground
V_{CC}	P4	—	Positive Supply
GND	R4	—	Ground
4LE	T4	Input	Bank 4, Latch Enable, Active Low
1D1	A5	Input	Bank 1, Channel 1, Data Input
1D3	B5	Input	Bank 1, Channel 3, Data Input
1D5	C5	Input	Bank 1, Channel 5, Data Input
1D7	D5	Input	Bank 1, Channel 7, Data Input
2D1	E5	Input	Bank 2, Channel 1, Data Input
2D3	F5	Input	Bank 2, Channel 3, Data Input
2D5	G5	Input	Bank 2, Channel 5, Data Input
2D8	H5	Input	Bank 2, Channel 8, Data Input
3D1	J5	Input	Bank 3, Channel 1, Data Input
3D3	K5	Input	Bank 3, Channel 3, Data Input
3D5	L5	Input	Bank 3, Channel 5, Data Input
3D7	M5	Input	Bank 3, Channel 7, Data Input
4D1	N5	Input	Bank 4, Channel 1, Data Input
4D3	P5	Input	Bank 4, Channel 3, Data Input
4D5	R5	Input	Bank 4, Channel 5, Data Input
4D8	T5	Input	Bank 4, Channel 8, Data Input
1D2	A6	Input	Bank 1, Channel 2, Data Input
1D4	B6	Input	Bank 1, Channel 4, Data Input
1D6	C6	Input	Bank 1, Channel 6, Data Input
1D8	D6	Input	Bank 1, Channel 8, Data Input
2D2	E6	Input	Bank 2, Channel 2, Data Input
2D4	F6	Input	Bank 2, Channel 4, Data Input
2D6	G6	Input	Bank 2, Channel 6, Data Input
2D7	H6	Input	Bank 2, Channel 7, Data Input
3D2	J6	Input	Bank 3, Channel 2, Data Input
3D4	K6	Input	Bank 3, Channel 4, Data Input
3D6	L6	Input	Bank 3, Channel 6, Data Input
3D8	M6	Input	Bank 3, Channel 8, Data Input
4D2	N6	Input	Bank 4, Channel 2, Data Input
4D4	P6	Input	Bank 4, Channel 4, Data Input
4D6	R6	Input	Bank 4, Channel 6, Data Input

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
4D7	T6	Input	Bank 4, Channel 7, Data Input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	6.5	V
V_I	Input voltage range(2)		– 0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		– 0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 50	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVCH32373A		UNIT
		GKE	NMJ	
		96 PINS	96 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	26.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	14.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.9	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.8	10.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		1.65 V to 3.6 V	V_{CC} – 0.2			V
	I_{OH} = –4 mA		1.65 V	1.2			
	I_{OH} = –8 mA		2.3 V	1.7			
	I_{OH} = –12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = –24 mA		3 V	2.2			
V_{OL}	I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
	I_{OL} = 4 mA		1.65 V			0.45	
	I_{OL} = 8 mA		2.3 V			0.7	
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5	μA
$I_{I(hold)}$	V_I = 0.58 V		1.65 V	25			μA
	V_I = 1.07 V			–25			
	V_I = 0.7 V		2.3 V	45			
	V_I = 1.7 V			–45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			–75			
	V_I = 0 to 3.6 V(2)		3.6 V			±500	
I_{off}	V_I or V_O = 5.5 V		0			±10	μA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			40	μA
	3.6 V ≤ V_I ≤ 5.5 V(3)					40	
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		5		pF
C_o	V_O = V_{CC} or GND		3.3 V		6.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) This applies in the disabled state only.

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	(1)		(1)		3.3		3.3		ns
t_{su}	Setup time, data before LE ↓	(1)		(1)		1.7		1.7		ns
t_h	Hold time, data after LE ↓	(1)		(1)		1.2		1.2		ns

(1) This information was not available at the time of publication.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	(1)	(1)	(1)	(1)		4.9	1.6	4.2	ns
	LE		(1)	(1)	(1)	(1)		5.3	2.1	4.6	
t_{en}	$\overline{OE}$	Q	(1)	(1)	(1)	(1)		5.7	1.3	4.7	ns
t_{dis}	$\overline{OE}$	Q	(1)	(1)	(1)	(1)		6.3	2.5	5.9	ns

(1) This information was not available at the time of publication.

6.8 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	f = 10 MHz	(1)	(1)	39	pF
		Outputs disabled		(1)	(1)	6	

(1) This information was not available at the time of publication.

6.9 Typical Characteristics

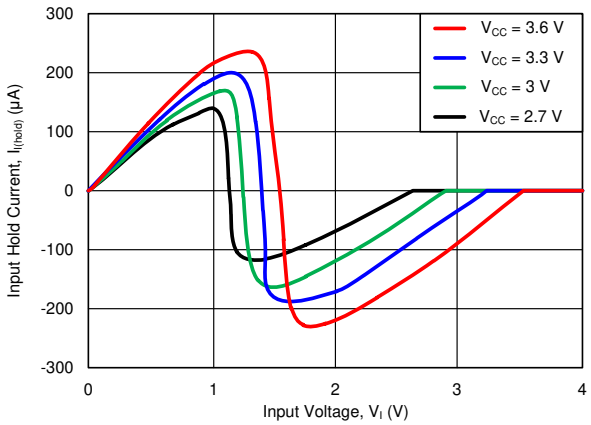
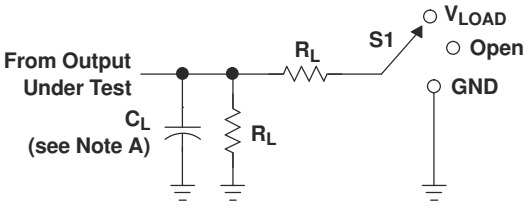


图 6-1. Typical input current for LVC family bus-hold inputs

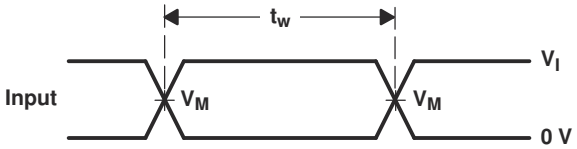
Parameter Measurement Information



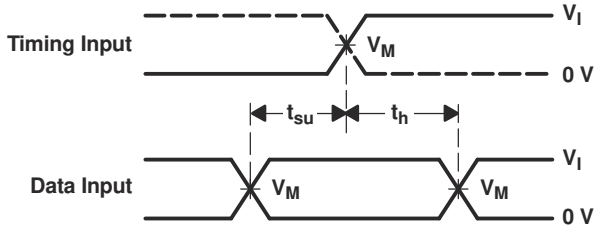
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

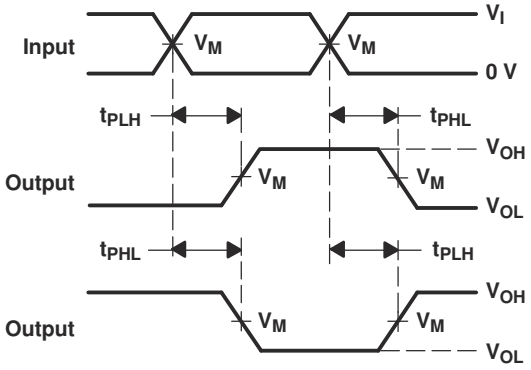
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



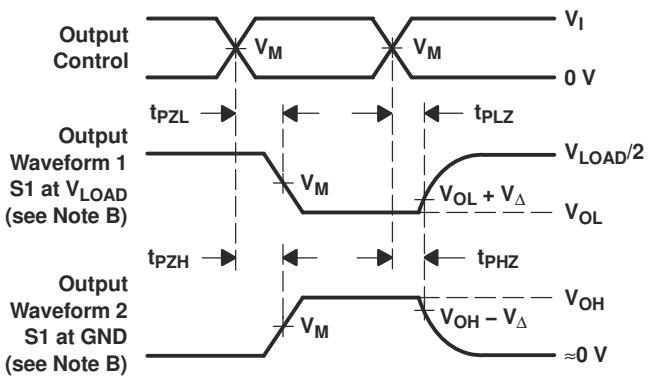
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVCH32373A is a 32-bit transparent D-type latch that is designed for 1.65-V to 3.6-V V_{CC} operation.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended.

Latches are arranged in banks of 8, with each bank having a separate latch enable (LE) and output enable ($\overline{OE}$) associated with it, as shown in the functional block diagram below.

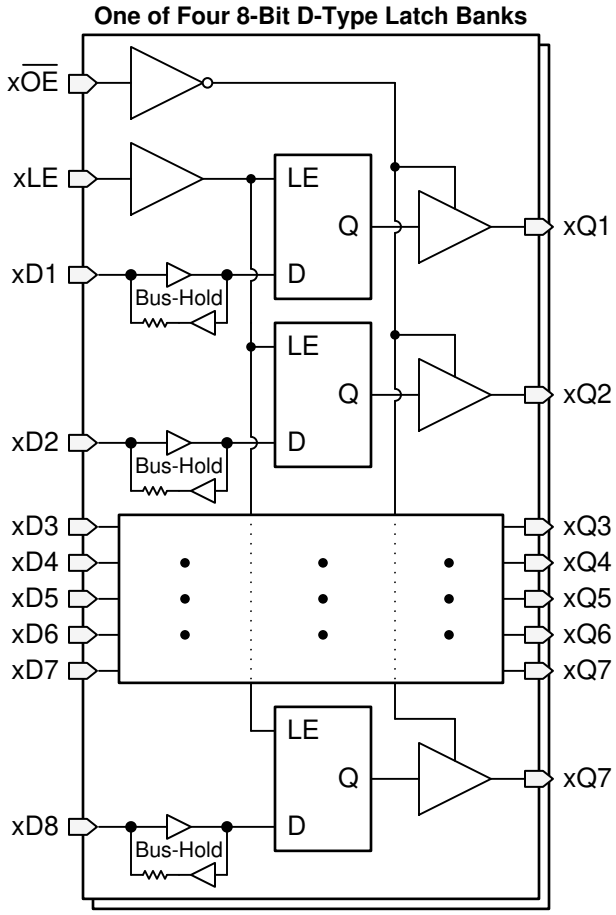
When the latch enable pin for a bank is asserted (HIGH), the outputs will follow the data inputs.

When the latch enable pin for a bank is de-asserted (LOW), the outputs will continue to hold the valid input value at the time of switching.

When the output enable pin is asserted (LOW), the output is active.

When the output enable pin is de-asserted (HIGH), the output is disabled (high impedance). This does not affect the latch operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance to ground given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings,* and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the *Recommended Oeprating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

7.3.5 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in 图 7-1.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

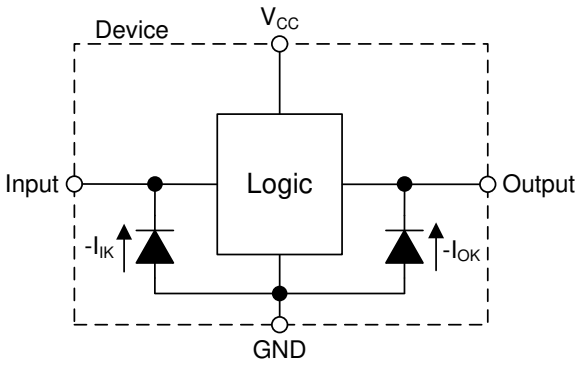


图 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.6 Bus-Hold Data Inputs

Each data input (D) on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data has been sent through a channel, the latch then maintains the previous state on the input if the line is left floating. It is not recommended to use pull-up or pull-down resistors together with a bus-hold input, as it may cause undefined inputs to occur which can lead to excessive current consumption.

Bus-hold data inputs prevent floating inputs on this device. The Implications of Slow or Floating CMOS Inputs application report explains the problems associated with leaving CMOS inputs floating. These latches remain active at all times, independent of all control signals such as direction control or output enable. The Bus-Hold Circuit application report has additional details regarding bus-hold inputs.

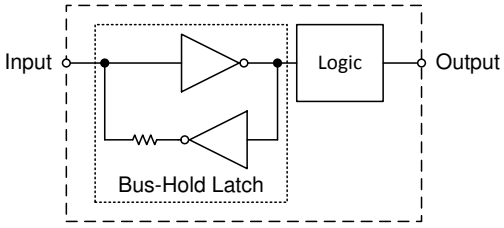


图 7-2. Bus-Hold circuit block diagram representation

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

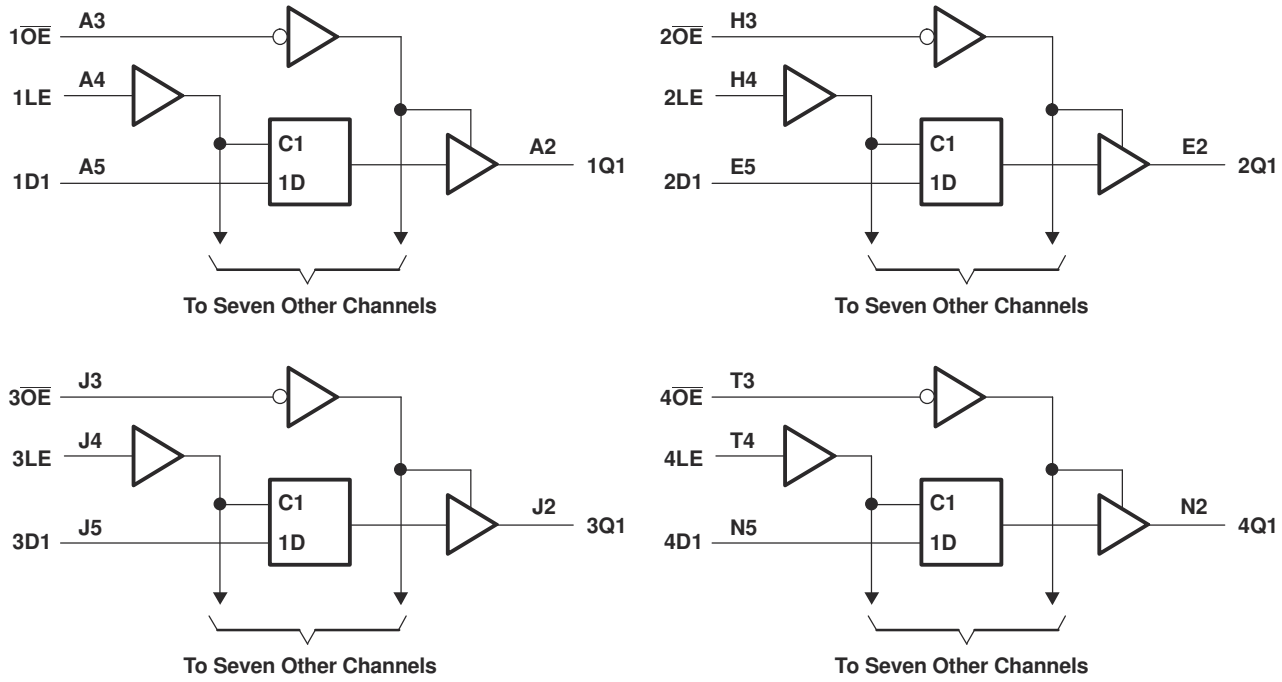


图 7-3. Logic Diagram (Positive Logic)

8 Application and Implementation

Note

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

In this application, the SN74LVCH32373A 32-bit D-type latch with bus-hold inputs is used to control a 24-bit bus.

8.2 Typical Application

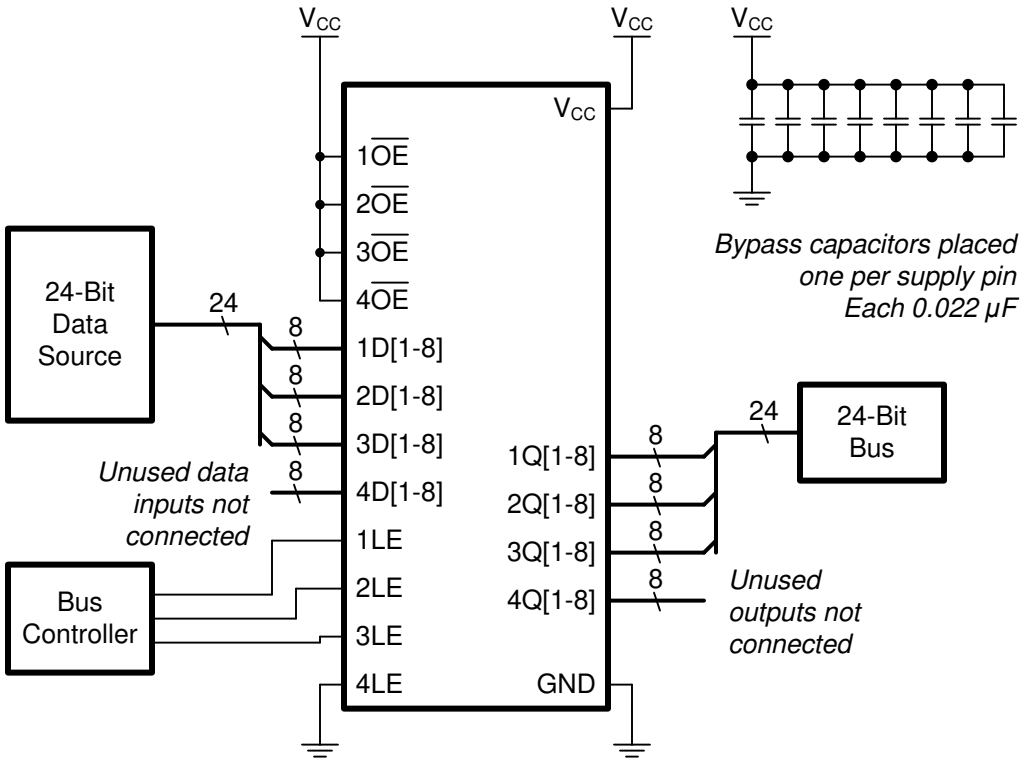


图 8-1. Simplified schematic for typical application

8.2.1 Design Requirements

- All signals in the system operate at the same voltage within the recommended operating range of the device
- Inputs can be disconnected or placed into the high-impedance state; bus-hold circuitry will maintain the last known state at the input
- Outputs must remain active at all times to prevent the bus from floating

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVCH32373A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

The SN74LVCH32373A can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LVCH32373A, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74LVCH32373A has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*. The plots in *图 8-2* and 图 8-3 provide a typical relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to *Feature Description* for additional information regarding the outputs for this device.

8.2.1.4 Timing Considerations

The SN74LVCH32373A is a latched device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Requirements*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Requirements*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Requirements*.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from each supply pin (V_{CC}) to a nearby GND pin. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. For BGA type

packages, these capacitors are often placed on the back of the board to minimize trace length. Adding one capacitor per supply pin is recommended.

2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVCH32373A to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / 50 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation. In multi-channel high-speed applications, it is possible to reach the thermal limits of the device without violating any other absolute maximum ratings.

8.2.3 Application Curves

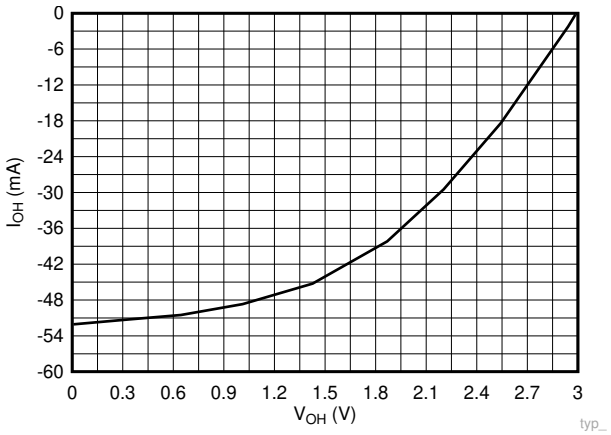


图 8-2. LVC family typical output voltage in the high state

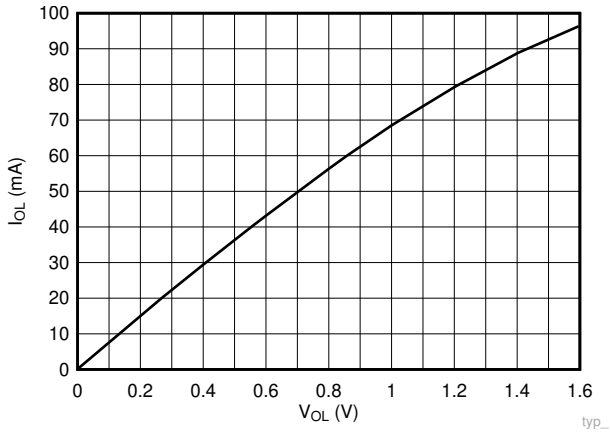


图 8-3. LVC family typical output voltage in the low state

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.022- μF capacitor at each supply pin is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for best results. With BGA packages, this often means putting the capacitors on the back of the board.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only 24 channels of a 32-channel D-type latch are used. Pins with bus-hold circuitry (xDy) are automatically held in a valid state and can be left unconnected without the input voltage floating. Other inputs, such as the xLE and x $\overline{OE}$ must be terminated at either ground or V_{CC} to prevent floating. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

It is not recommended to use pull-up or pull-down resistors with bus-hold inputs.

10.2 Layout Example

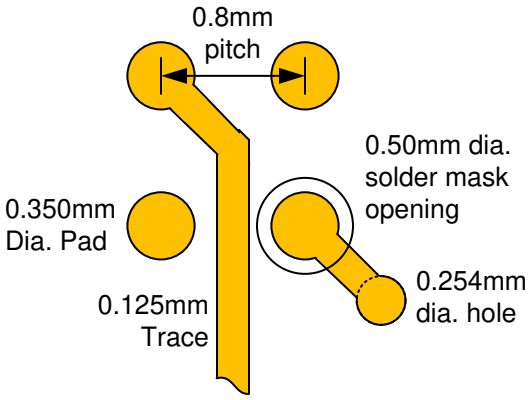


图 10-1. BGA layout examples

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- CMOS Power Consumption and CPD Calculation
- Designing with Logic

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVCH32373ANMJR	Active	Production	NFBGA (NMJ) | 96	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	29TW
SN74LVCH32373ANMJR.B	Active	Production	NFBGA (NMJ) | 96	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

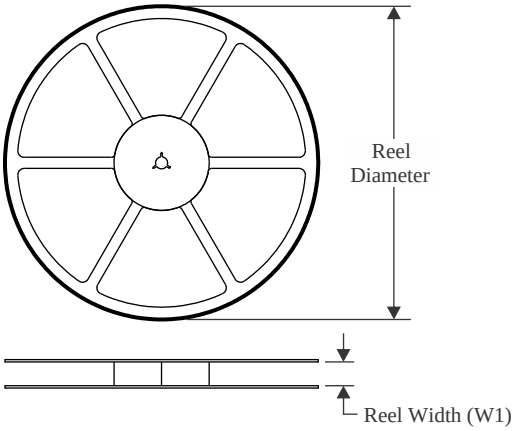
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

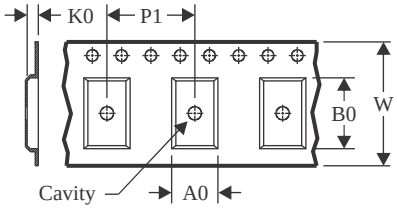
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

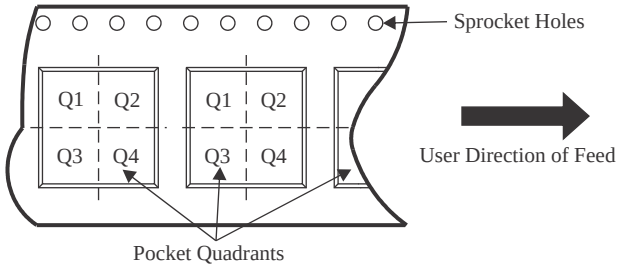


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

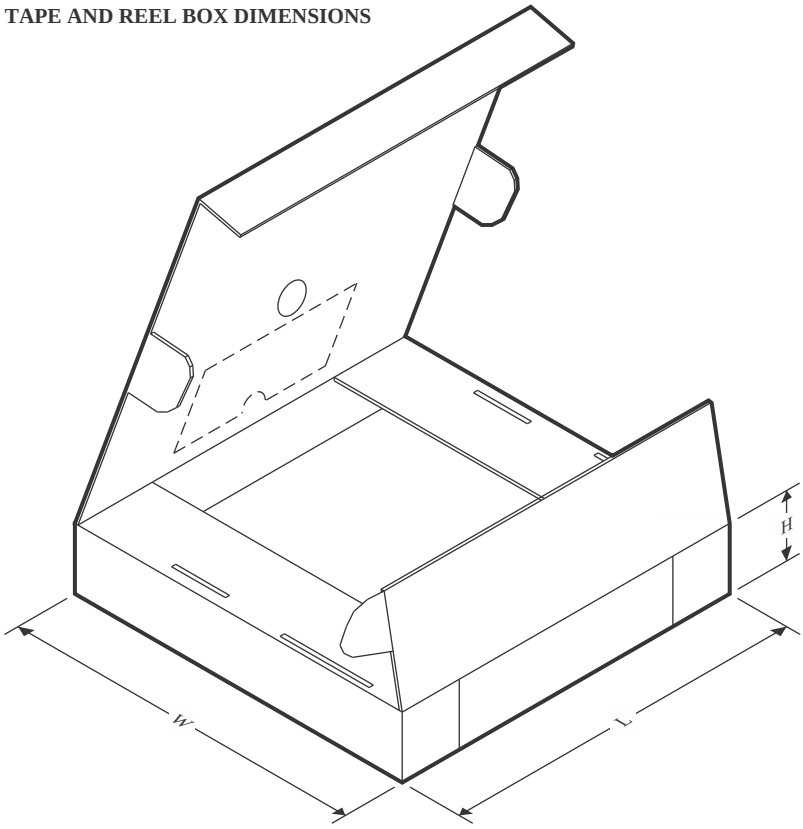
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH32373ANMJR	NFBGA	NMJ	96	1000	330.0	24.4	5.85	13.85	1.8	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

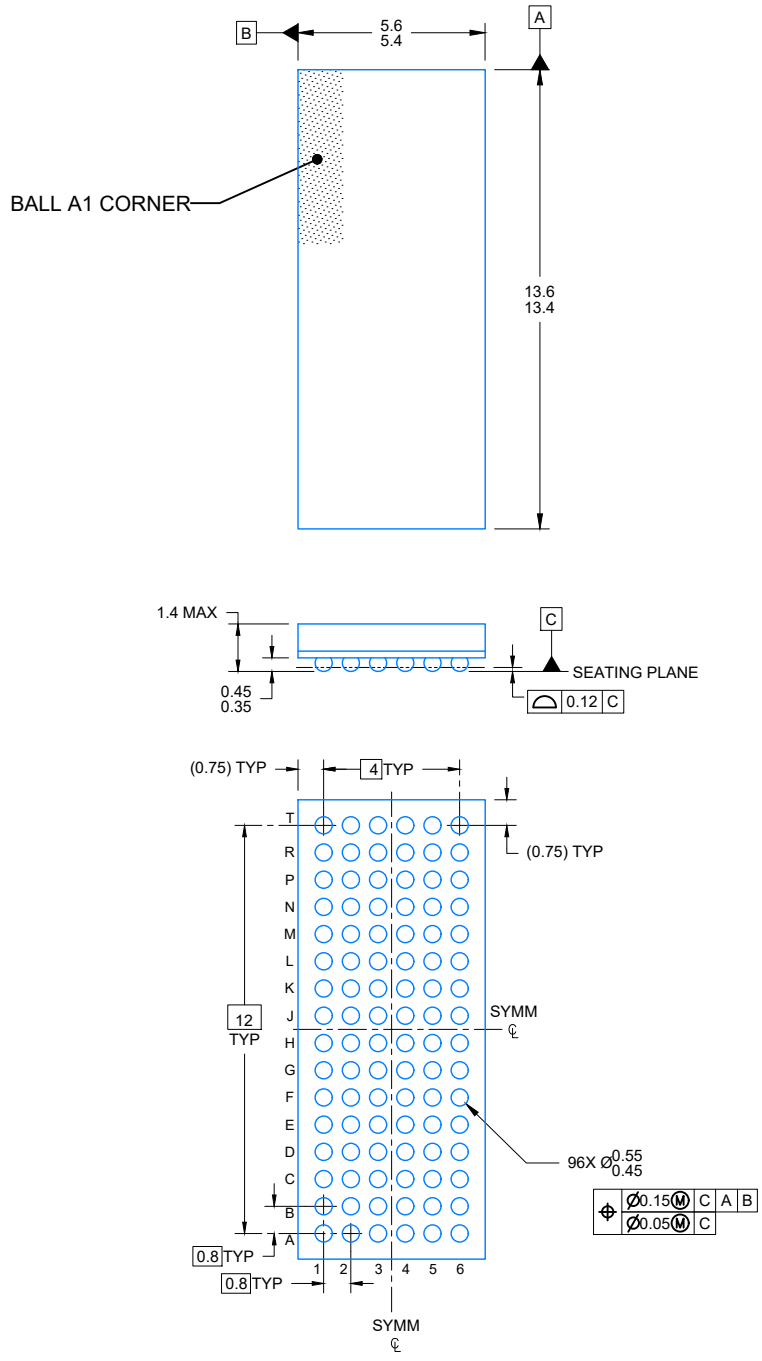
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH32373ANMJR	NFBGA	NMJ	96	1000	336.6	336.6	41.3

PACKAGE OUTLINE

NMJ0096A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



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NOTES:

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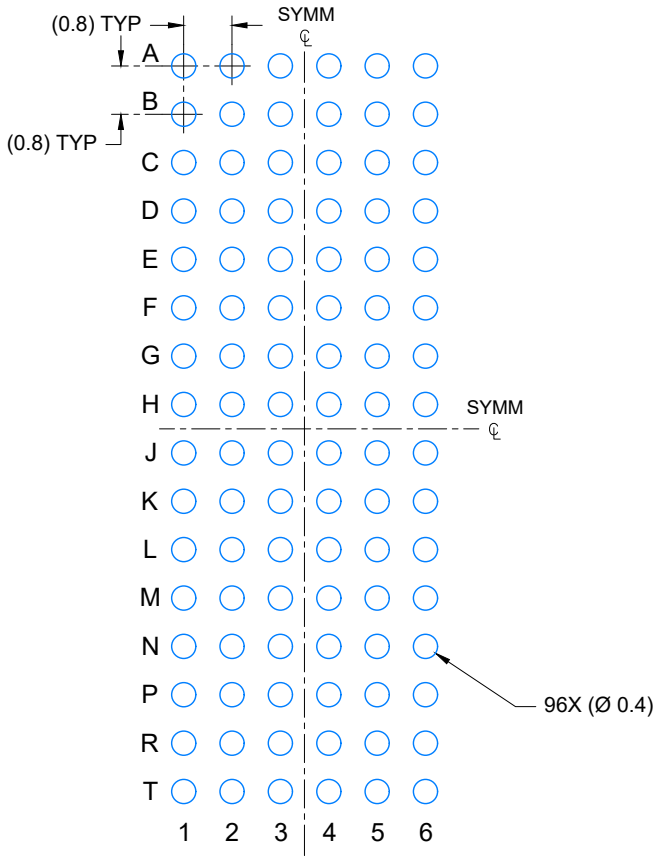
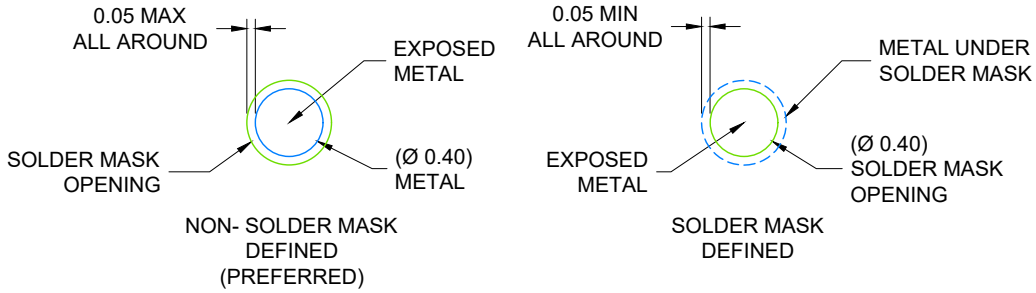
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

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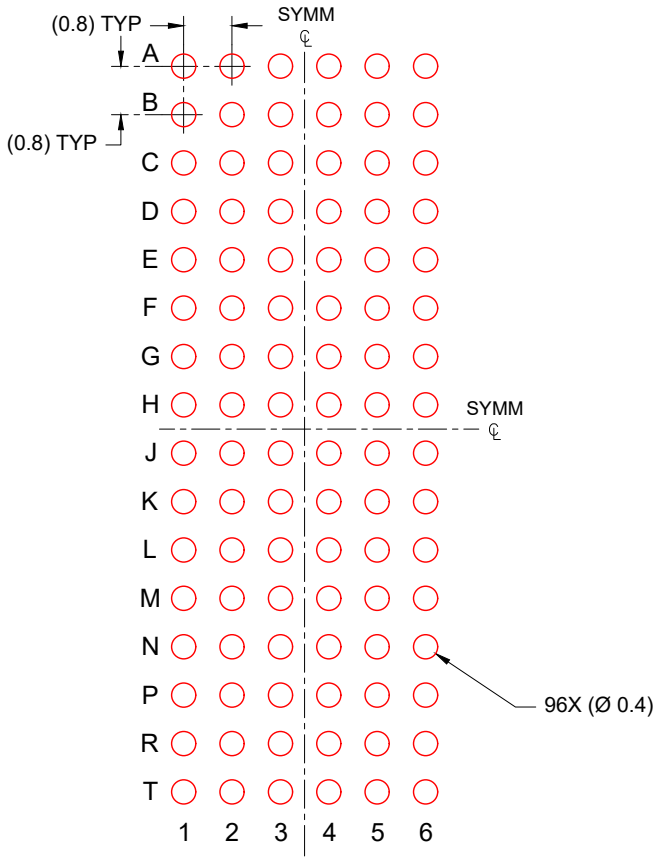
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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