16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74LVCH16T245-EP

FEATURES

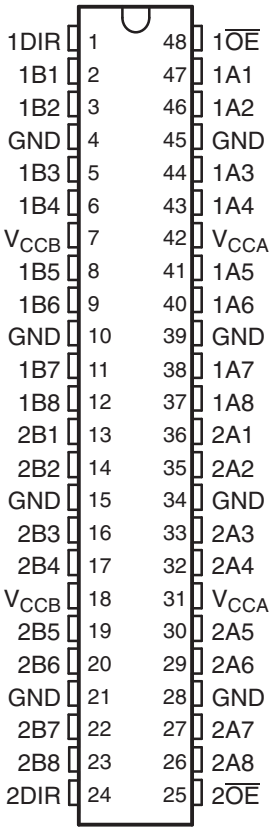
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DGV PACKAGE
(TOP VIEW)



DESCRIPTION

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVCH16T245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA}.

DESCRIPTION (CONTINUED)

The SN74LVCH16T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then all outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–50°C to 125°C	TVSOP – DGV	Tape and reel	CLVCH16T245MDGVREP	LDHT245MEP
	TSSOP - DGG	Tape and reel	CLVCH16T245MDGGREP	8UT245MEP

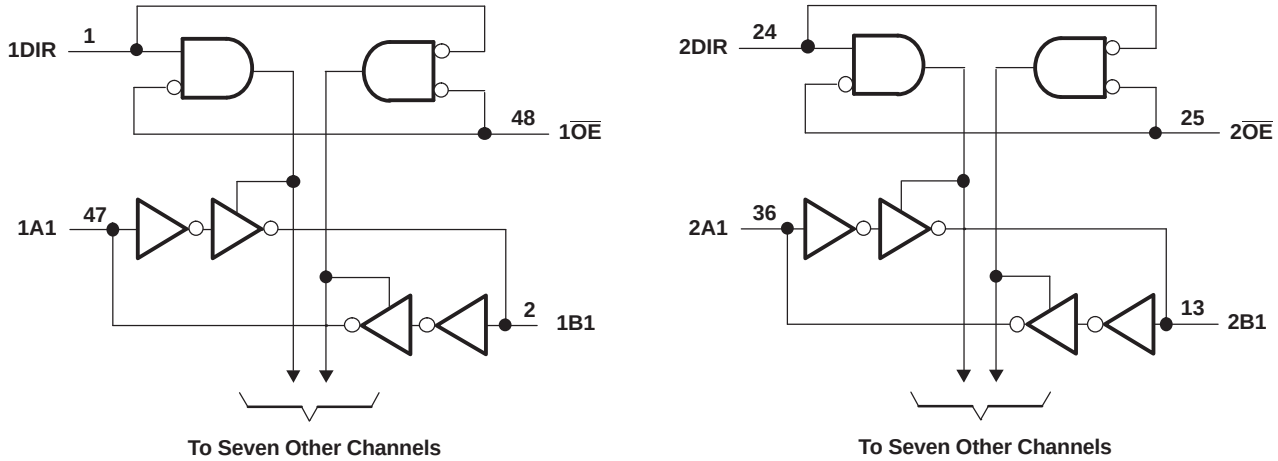
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE(1)
(EACH 16-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
θ_{JA}	Package thermal impedance(4)			58	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs(4)	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs(4)	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA})(5)	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA})(5)	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-State			0	5.5	
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused control inputs of the device must be held at V_{CCA} GND to ensure proper device operation and minimize power consumption. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics (1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA,	$V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} – 0.1		V
		I_{OH} = –4 mA,	$V_I = V_{IH}$	1.65 V	1.65 V				1.2		
		I_{OH} = –8 mA,	$V_I = V_{IH}$	2.3 V	2.3 V				1.9		
		I_{OH} = –24 mA,	$V_I = V_{IH}$	3 V	3 V				2.4		
		I_{OH} = –32 mA,	$V_I = V_{IH}$	4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 µA,	$V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA,	$V_I = V_{IL}$	1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA,	$V_I = V_{IL}$	2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA,	$V_I = V_{IL}$	3 V	3 V					0.55	
		I_{OL} = 32 mA,	$V_I = V_{IL}$	4.5 V	4.5 V					0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V		±0.5	±1		±2	µA
I_{BHL} (3)		V_I = 0.58 V		1.65 V	1.65 V				15		µA
		V_I = 0.7 V		2.3 V	2.3 V				45		
		V_I = 0.8 V		3 V	3 V				75		
		V_I = 0.1.35 V		4.5 V	4.5 V				100		
I_{BHH} (4)		V_I = 1.07 V		1.65 V	1.65 V				–15		µA
		V_I = 1.7 V		2.3 V	2.3 V				–45		
		V_I = 2 V		3 V	3 V				–75		
		V_I = 3.15 V		4.5 V	4.5 V				–100		
I_{BHLO} (5)		$V_I = 0$ to V_{CC}		1.95 V	1.95 V				200		µA
				2.7 V	2.7 V				300		
				3.6 V	3.6 V				500		
				5.5 V	5.5 V				900		
I_{BHHO} (6)		$V_I = 0$ to V_{CC}		1.95 V	1.95 V				–200		µA
				2.7 V	2.7 V				–300		
				3.6 V	3.6 V				–500		
				5.5 V	5.5 V				–900		
I_{off}	A port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V		±0.5	±1		±2	µA
	B port			0 to 5.5 V	0 V		±0.5	±1		±2	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	µA
	B port		$\overline{OE}$ = don't care	0 V	5.5 V			±1		±2	
	A port			5.5 V	0 V			±1		±2	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					20	µA
				5 V	0 V					20	
				0 V	5 V					–2	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					20	µA
				5 V	0 V					–2	
				0 V	5 V					20	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					30	µA

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Electrical Characteristics(1) (2) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	MIN	MAX	UNIT
ΔI_{CCA}	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND	3 V to 5.5 V	3 V to 5.5 V					50	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V	3.3 V		4			5	pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5			10	pF

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.4	7.1	ns
t_{PLH} / t_{PHL}	B	A	0.9	23.8	0.8	23.8	0.7	23.4	0.7	23.4	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.8	32	1.5	18	1.2	12.6	0.9	10.8	ns

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.5	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PLH} / t_{PHL}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.7	28.2	1.5	12.9	1.2	9.4	1	6.9	ns

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.6	21.2	1.1	8.8	0.8	6.2	0.6	4.4	ns
t_{PHL}											
t_{PLH}	B	A	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.8	0.8	6.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.8	7.8	0.8	8.1	0.8	8.1	0.8	8.1	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.8	27.7	1.4	12.4	1.1	8.5	0.8	6.4	ns
t_{PZL}											

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PHL}											
t_{PLH}	B	A	0.7	7	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2	28.7	1.8	9.7	1.4	8	0.7	5.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.5	27.6	1.3	11.4	1	8.1	0.9	6	ns
t_{PZL}											

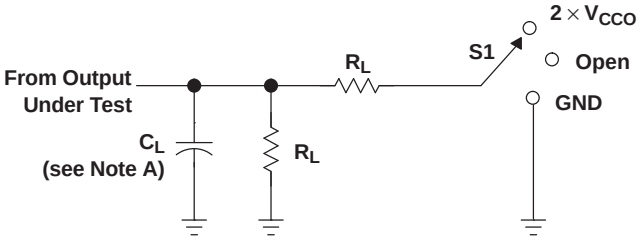
Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		18	19	19	22	
C_{pdB} (1)	A-port input, B-port output		18	19	20	22	
	B-port input, A-port output		2	2	2	2	

(1) Power dissipation capacitance per transceiver

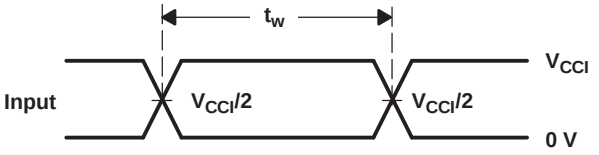
PARAMETER MEASUREMENT INFORMATION



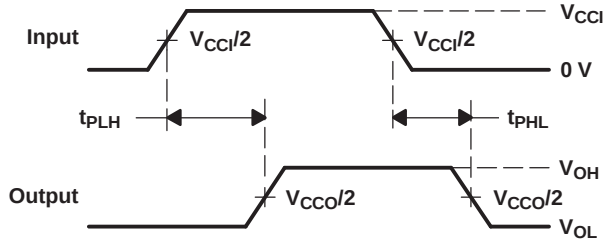
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CCO}$ GND

LOAD CIRCUIT

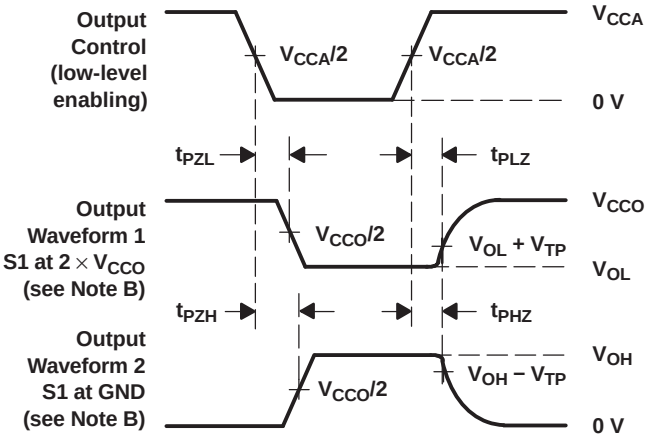
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLVCH16T245MDGGREP	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	8UT245MEP
CLVCH16T245MDGVREP	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LDHT245MEP
V62/09605-01XE	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	8UT245MEP
V62/09605-01YE	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LDHT245MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVCH16T245-EP :

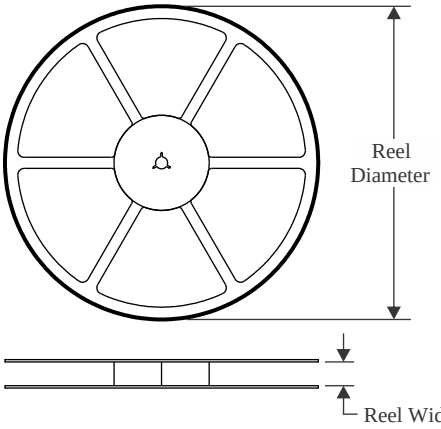
- Catalog : SN74LVCH16T245

NOTE: Qualified Version Definitions:

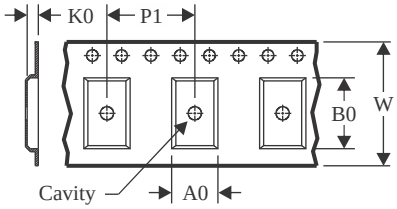
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

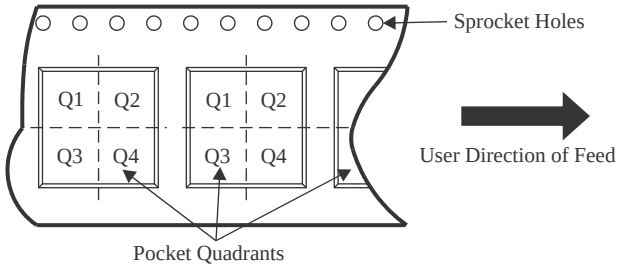


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

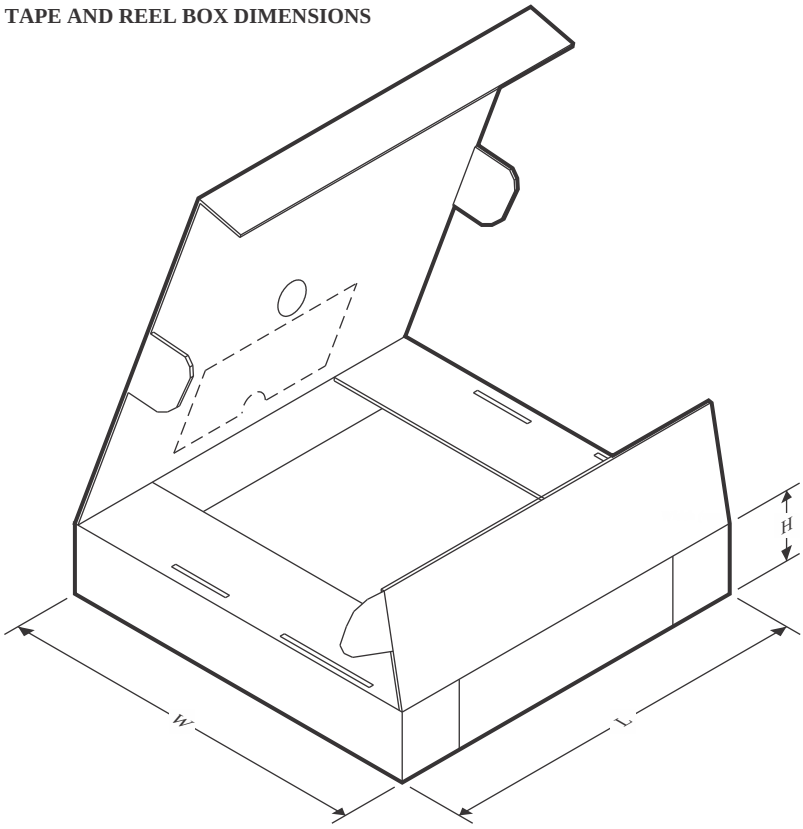
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

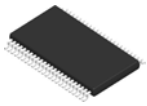
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVCH16T245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CLVCH16T245MDGVREP	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVCH16T245MDGGREP	TSSOP	DGG	48	2000	356.0	356.0	45.0
CLVCH16T245MDGVREP	TVSOP	DGV	48	2000	353.0	353.0	32.0

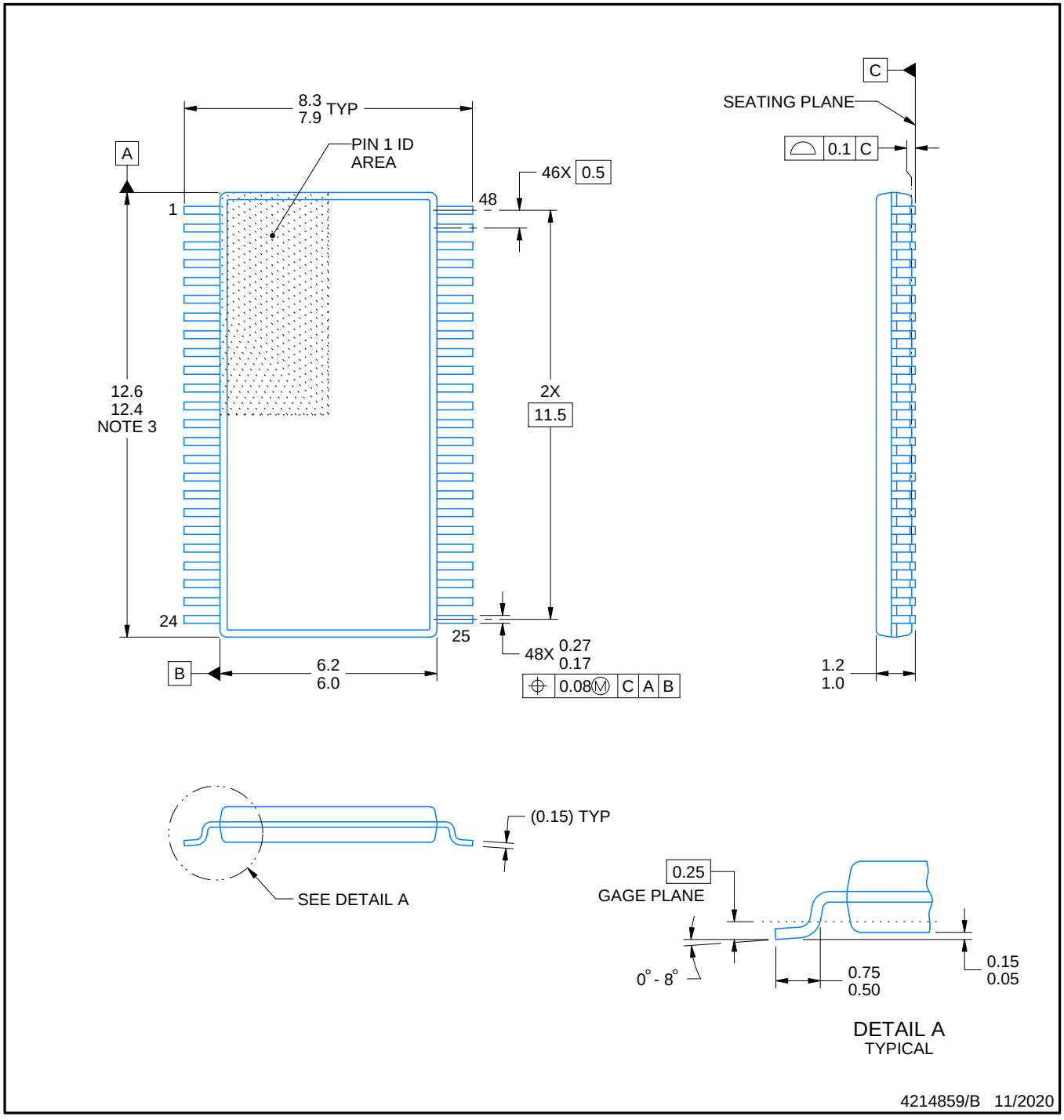


PACKAGE OUTLINE

DGG0048A

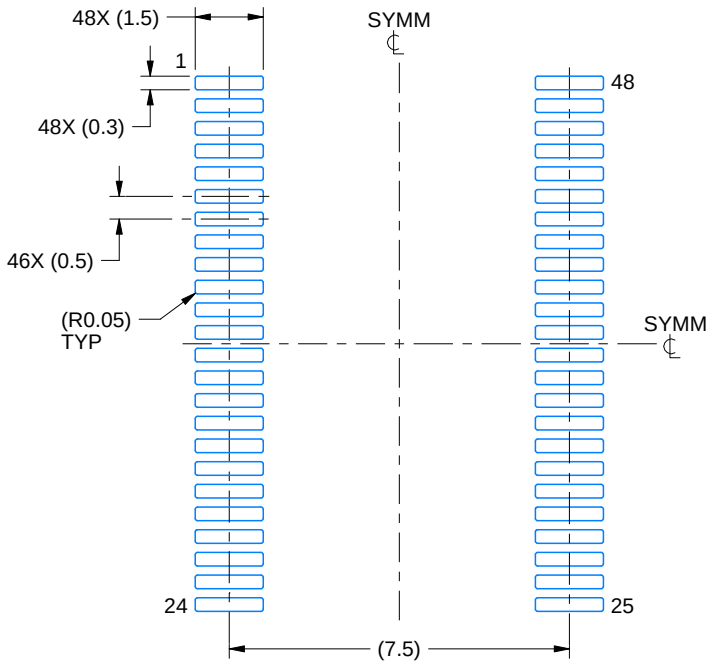
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

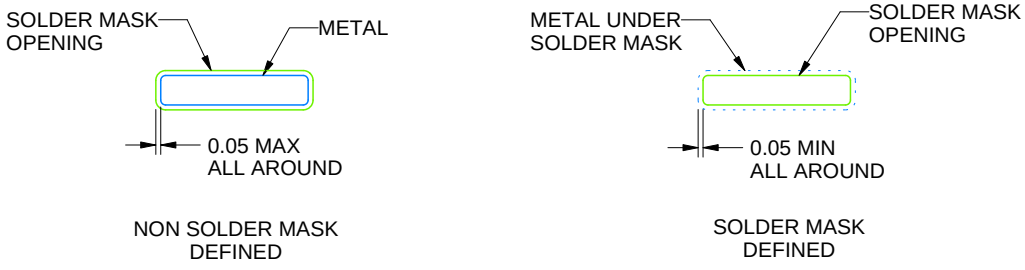


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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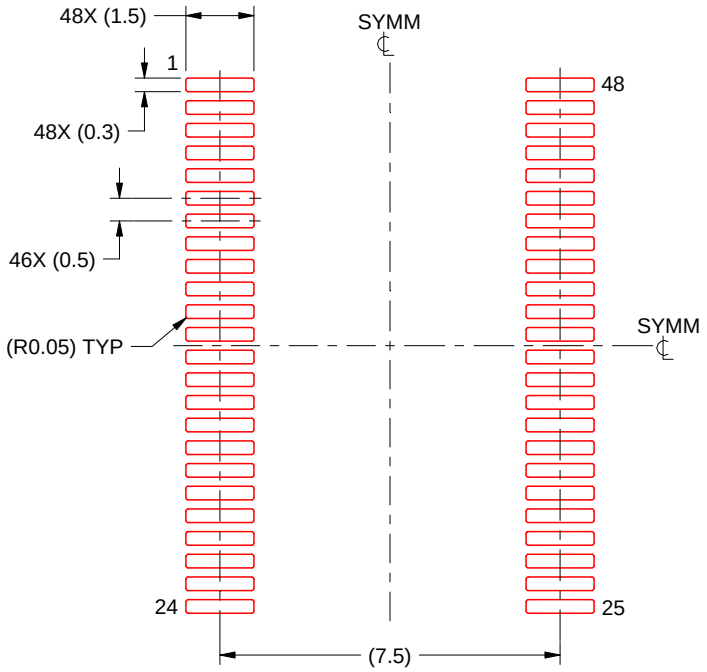
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

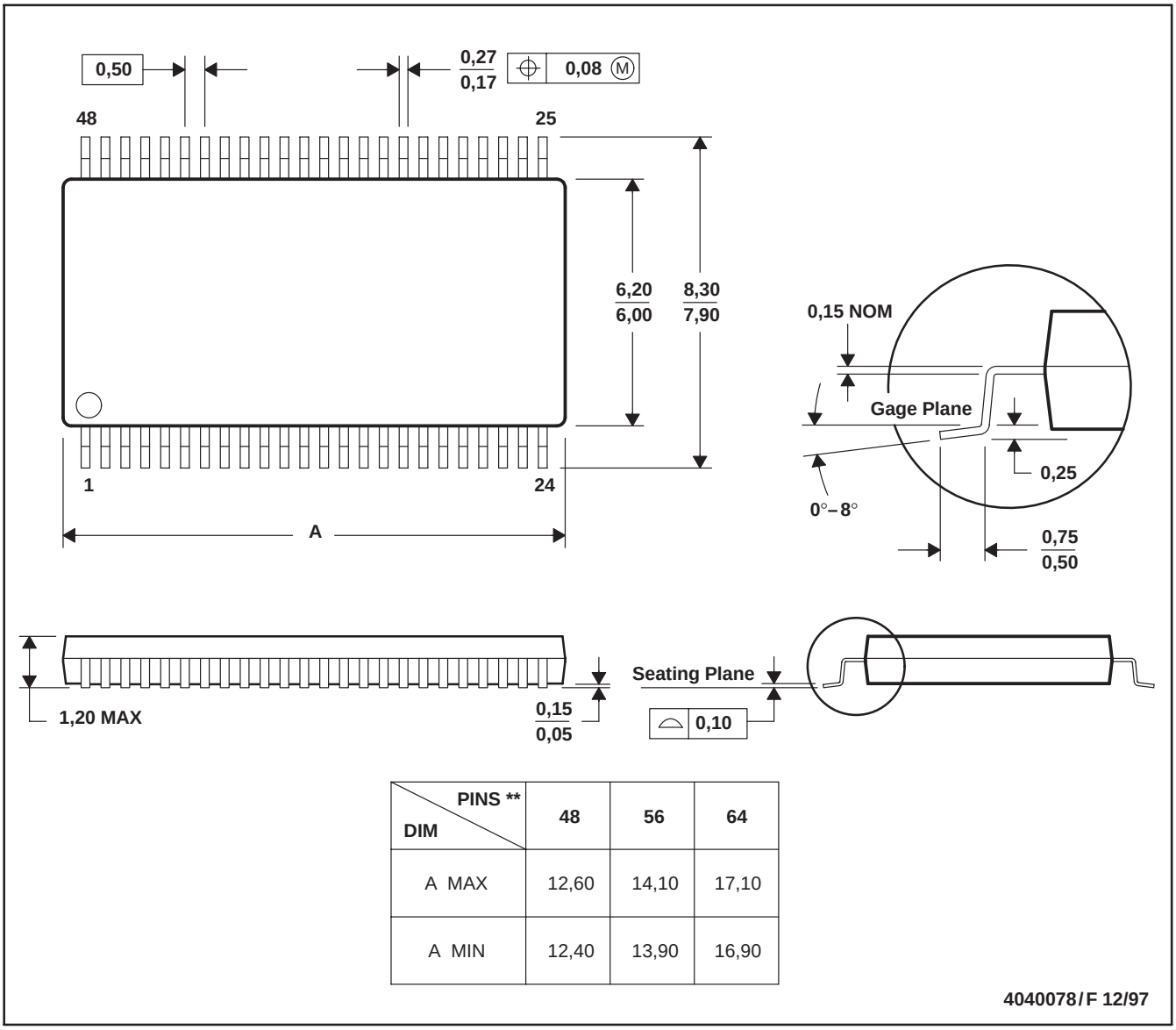
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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