# SN74LVCC4245A-EP
# OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

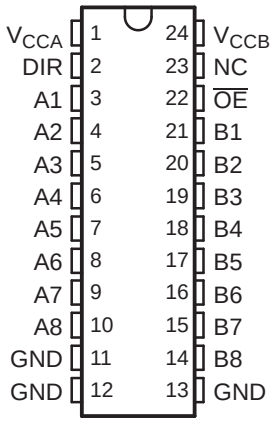
SCAS830 – MARCH 2007

## FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Bidirectional Voltage Translator**
- **4.5 V to 5.5 V on A Port and 2.7 V to 5.5 V on B Port**
- **Control Inputs $V_{IH}$/$V_{IL}$ Levels Are Referenced to $V_{CCA}$ Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**PW PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## DESCRIPTION/ORDERING INFORMATION

The SN74LVCC4245A is an 8-bit (octal) noninverting bus transceiver that uses two separate power-supply rails. The A port ($V_{CCA}$) is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track $V_{CCB}$, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses effectively are isolated. The control circuitry (DIR, $\overline{OE}$) is powered by $V_{CCA}$.

**ORDERING INFORMATION**(1)

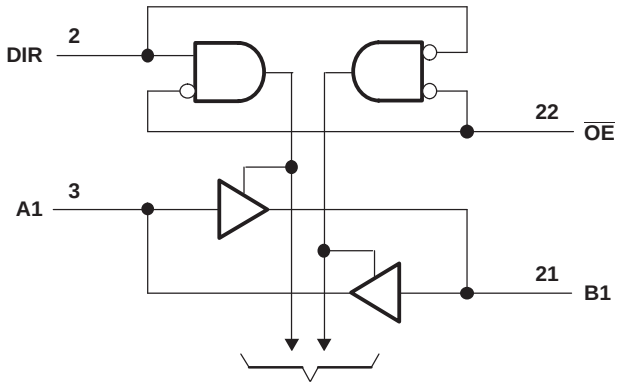
| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55 °C to 125 °C | TSSOP – PW | Reel of 2000 | CLVCC4245AMPWREP | LG245A-EP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### FUNCTION TABLE (EACH TRANSCEIVER)

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

### LOGIC DIAGRAM (POSITIVE LOGIC)




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ $V_{CCB}$ | Supply voltage range | | –0.5 | 6 | V |
| $V_I$ | Input voltage range(2) | I/O ports (A port) | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | I/O ports (B port) | –0.5 | $V_{CCB}$ + 0.5 | |
| | | Except I/O ports | –0.5 | $V_{CCA}$ + 0.5 | |
| $V_O$ | Output voltage range(2) | A port | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | B port | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 V | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 V | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | | | 88 | °C/W |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions[1]

| | | $V_{CCA}$ | $V_{CCB}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 4.5 | 5 | 5.5 | V |
| $V_{CCB}$ | | | | 2.7 | 3.3 | 5.5 | |
| $V_{IHA}$ | High-level input voltage | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 2 | | | |
| $V_{IHB}$ | High-level input voltage | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 3.85 | | | |
| $V_{ILA}$ | Low-level input voltage | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 0.8 | |
| $V_{ILB}$ | Low-level input voltage | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 1.65 | |
| $V_{IH}$ | High-level input voltage (control pins) (referenced to $V_{CCA}$) | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 2 | | | |
| $V_{IL}$ | Low-level input voltage (control pins) (referenced to $V_{CCA}$) | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 0.8 | |
| $V_{IA}$ | Input voltage | | | 0 | | $V_{CCA}$ | V |
| $V_{IB}$ | Input voltage | | | 0 | | $V_{CCB}$ | V |
| $V_{OA}$ | Output voltage | | | 0 | | $V_{CCA}$ | V |
| $V_{OB}$ | Output voltage | | | 0 | | $V_{CCB}$ | V |
| $I_{OHA}$ | High-level output current | 4.5 V | 3 V | | | –24 | mA |
| $I_{OHB}$ | High-level output current | 4.5 V | 2.7 V to 4.5 V | | | –24 | mA |
| $I_{OLA}$ | Low-level output current | 4.5 V | 3 V | | | 24 | mA |
| $I_{OLB}$ | Low-level output current | 4.5 V | 2.7 V to 4.5 V | | | 24 | mA |
| $T_A$ | Operating free-air temperature | | | –55 | | 125 | °C |

(1) All unused inputs of the device must be held at the associated $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –100 µA | 4.5 V | 3 V | 4.4 | 4.49 | | V |
| | | $I_{OH}$ = –24 mA | | | 3.76 | 4.25 | | |
| $V_{OHB}$ | | $I_{OH}$ = –100 µA | 4.5 V | 3 V | 2.9 | 2.99 | | V |
| | | $I_{OH}$ = –12 mA | 4.5 V | 2.7 V | 2.2 | 2.5 | | |
| | | | | 3 V | 2.46 | 2.85 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 2.7 V | 2.1 | 2.3 | | |
| | | | | 3 V | 2.25 | 2.65 | | |
| | | | | 4.5 V | 3.76 | 4.25 | | |
| $V_{OLA}$ | | $I_{OL}$ = 100 µA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.21 | 0.44 | |
| $V_{OLB}$ | | $I_{OL}$ = 100 µA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 12 mA | 4.5 V | 2.7 V | | 0.11 | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | 2.7 V | | 0.22 | 0.5 | |
| | | | | 3 V | | 0.21 | 0.44 | |
| | | | | 4.5 V | | 0.18 | 0.44 | |
| $I_I$ | Control inputs | $V_I$ = $V_{CCA}$ or GND | 5.5 V | 3.6 V | | ±0.1 | ±1 | µA |
| | | | | 5.5 V | | ±0.1 | ±1 | |
| $I_{OZ}$ (1) | A or B port | $V_O$ = $V_{CCA/B}$ or GND, $V_I$ = $V_{IL}$ or $V_{IH}$ | 5.5 V | 3.6 V | | ±0.5 | ±5 | µA |
| $I_{CCA}$ | B to A | $A_n$ = $V_{CC}$ or GND | 5.5 V | Open | | 8 | 80 | µA |
| | | $I_O$ (A port) = 0, $B_n$ = $V_{CCB}$ or GND | 5.5 V | 3.6 V | | 8 | 80 | |
| | | | | 5.5 V | | 8 | 80 | |
| $I_{CCB}$ | A to B | $A_n$ = $V_{CCA}$ or GND, $I_O$ (B port) = 0 | 5.5 V | 3.6 V | | 5 | 50 | µA |
| | | | | 5.5 V | | 8 | 80 | |
| $\Delta I_{CCA}$ (2) | A port | $V_I$ = $V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at GND and DIR at $V_{CCA}$ | 5.5 V | 5.5 V | | 1.35 | 1.5 | mA |
| | $\overline{OE}$ | $V_I$ = $V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, DIR at $V_{CCA}$ or GND | 5.5 V | 5.5 V | | 1 | 1.5 | |
| | DIR | $V_I$ = $V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at $V_{CCA}$ or GND | 5.5 V | 3.6 V | | 1 | 1.5 | |
| $\Delta I_{CCB}$ (2) | B port | $V_I$ = $V_{CCB}$ – 0.6 V, Other inputs at $V_{CCB}$ or GND, $\overline{OE}$ at GND and DIR at GND | 5.5 V | 3.6 V | | 0.35 | 0.5 | mA |
| $C_i$ | Control inputs | $V_I$ = $V_{CCA}$ or GND | Open | Open | | 5 | | pF |
| $C_{io}$ | A or B port | $V_O$ = $V_{CCA/B}$ or GND | 5 V | 3.3 V | | 11 | | pF |

(1) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated $V_{CC}$.

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1 through Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 5 V ± 0.5 V | | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 2.7 V to 3.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PHL}$ | A | B | 1 | 7.1 | 1 | 7 | ns |
| $t_{PLH}$ | | | 1 | 6 | 1 | 7 | |
| $t_{PHL}$ | B | A | 1 | 6.8 | 1 | 6.2 | ns |
| $t_{PLH}$ | | | 1 | 6.1 | 1 | 5.3 | |
| $t_{PZL}$ | $\overline{OE}$ | A | 1 | 9 | 1 | 9 | ns |
| $t_{PZH}$ | | | 1 | 8.3 | 1 | 8 | |
| $t_{PZL}$ | $\overline{OE}$ | B | 1 | 8.2 | 1 | 10 | ns |
| $t_{PZH}$ | | | 1 | 8.1 | 1 | 10.2 | |
| $t_{PLZ}$ | $\overline{OE}$ | A | 1 | 5.5 | 1 | 5.9 | ns |
| $t_{PHZ}$ | | | 1 | 5.7 | 1 | 5.9 | |
| $t_{PLZ}$ | $\overline{OE}$ | B | 1 | 6.4 | 1 | 6.4 | ns |
| $t_{PHZ}$ | | | 1 | 7.8 | 1 | 8.9 | |

## Operating Characteristics

$V_{CCA}$ = 5 V, $V_{CCB}$ = 3.3 V, $T_A$ = 25 °C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 0, f = 10 MHz | 20 | pF |
| | | Outputs disabled | | 6.5 | |

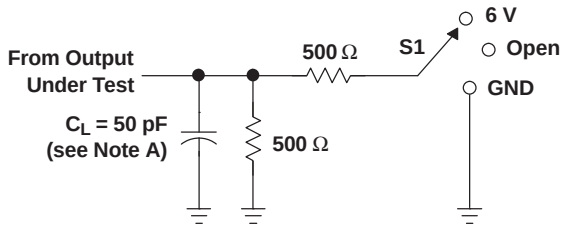
## Power-Up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence should always be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take the following precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ($V_{CCA}$ for all four of these devices).
3. Tie $\overline{OE}$ to $V_{CCA}$ with a pullup resistor so that it ramps with $V_{CCA}$.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with $V_{CCA}$. Otherwise, keep DIR low.

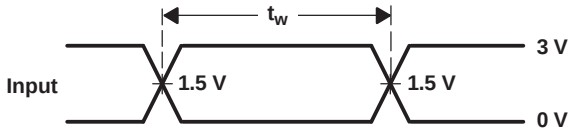
(1) See the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

## PARAMETER MEASUREMENT INFORMATION FOR A TO B
## $V_{CCA}$ = 4.5 V to 5.5 V and $V_{CCB}$ = 2.7 V to 3.6 V

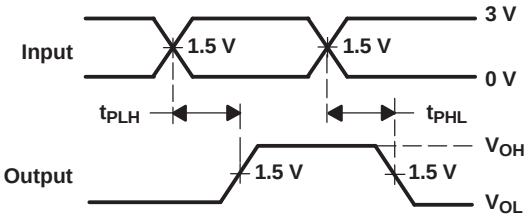



LOAD CIRCUIT

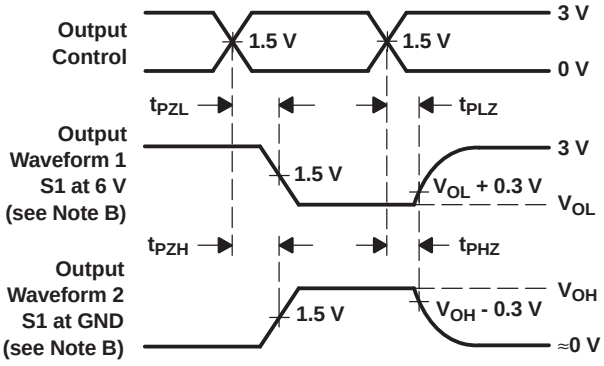
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

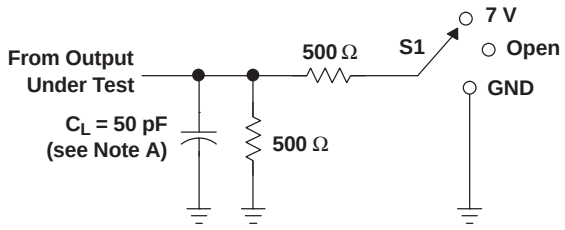



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

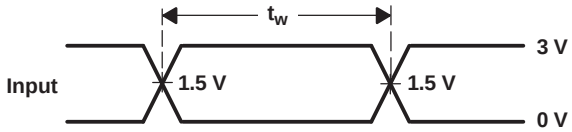
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR A TO B
## $V_{CCA}$ = 4.5 V to 5.5 V and $V_{CCB}$ = 3.6 V to 5.5 V

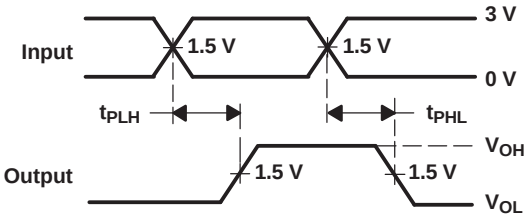



LOAD CIRCUIT

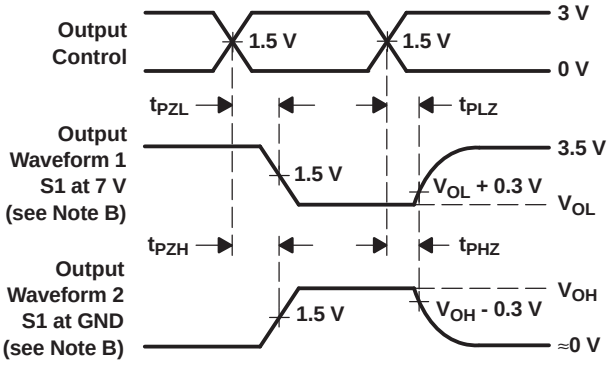
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

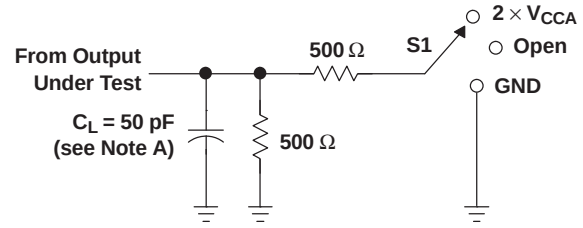



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

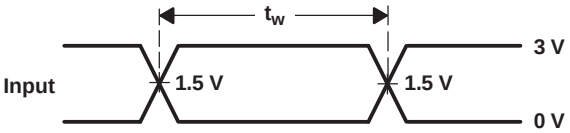
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ = 4.5 V to 5.5 V and $V_{CCB}$ = 2.7 V to 3.6 V

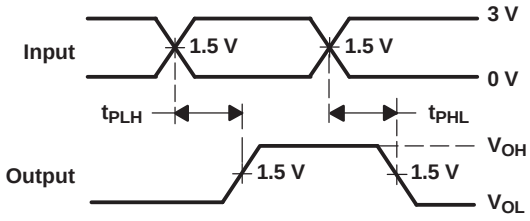



LOAD CIRCUIT

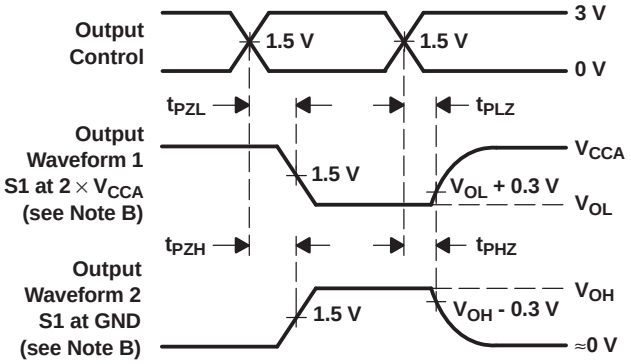
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCA}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

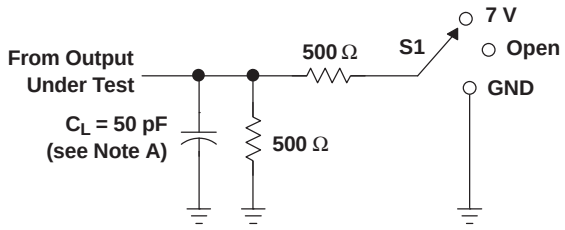



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

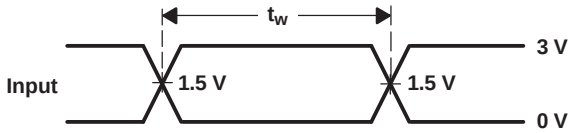
**Figure 3. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ = 4.5 V to 5.5 V and $V_{CCB}$ = 3.6 V to 5.5 V

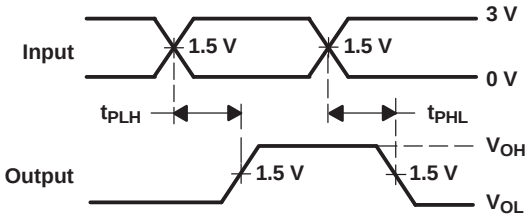



LOAD CIRCUIT

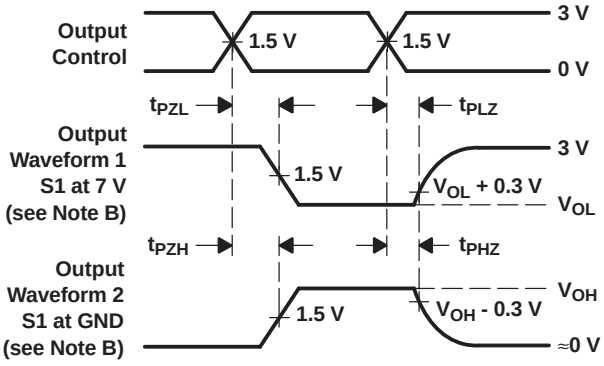
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CLVCC4245AMPWREP | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LG245A-EP |
| CLVCC4245AMPWREPG4 | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LG245A-EP |
| V62/06658-01XE | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LG245A-EP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF SN74LVCC4245A-EP :**

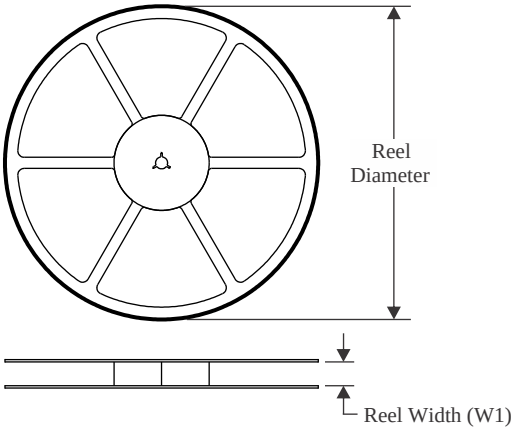
- Catalog : SN74LVCC4245A

NOTE: Qualified Version Definitions:

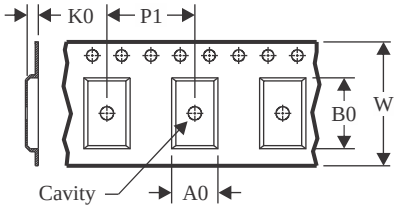
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

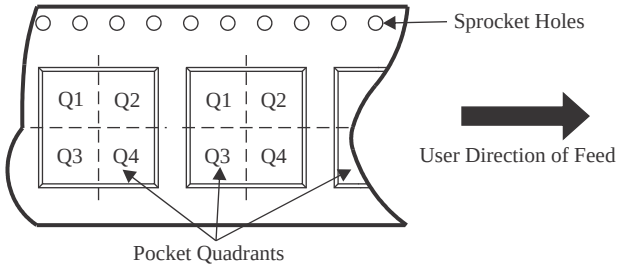



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

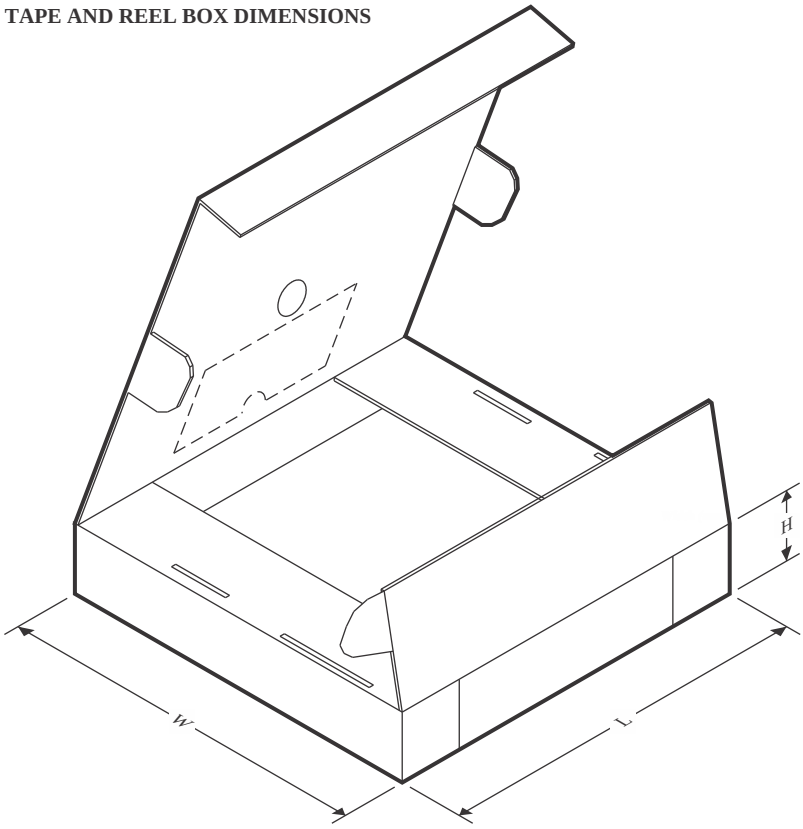
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLVCC4245AMPWREP | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

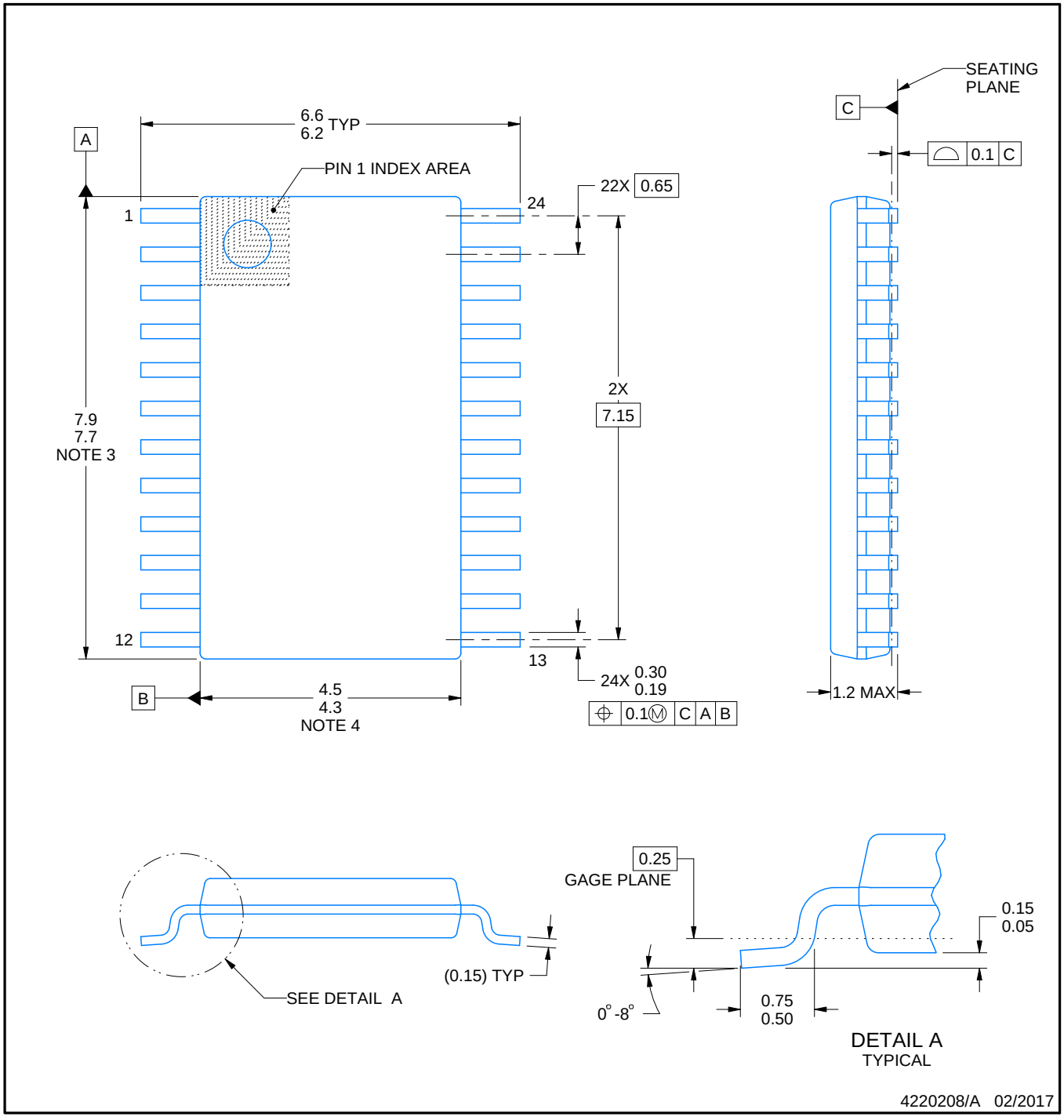
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CLVCC4245AMPWREP | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0024A

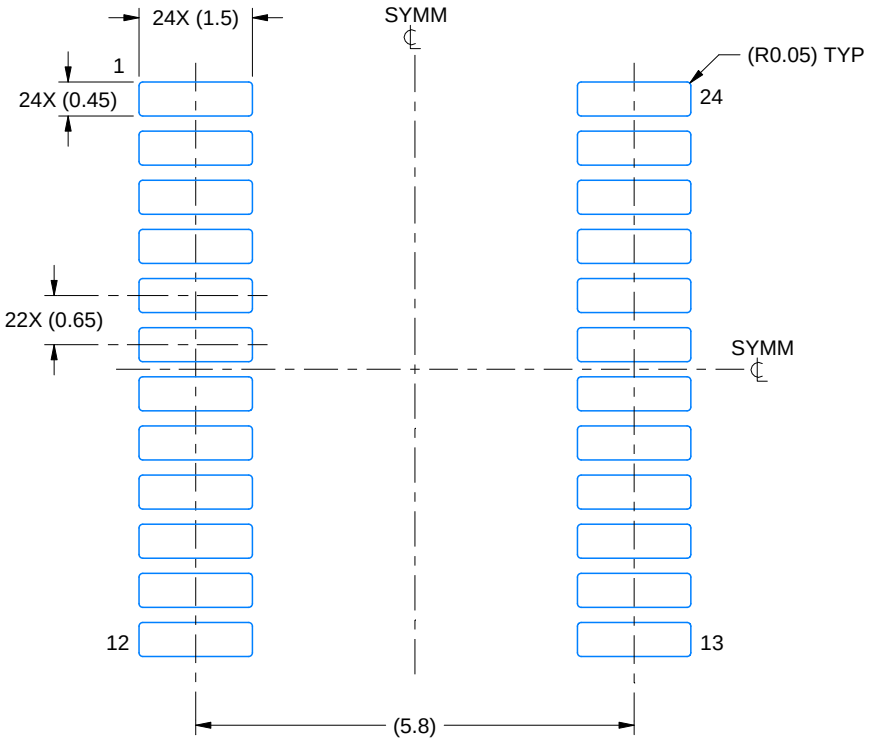
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

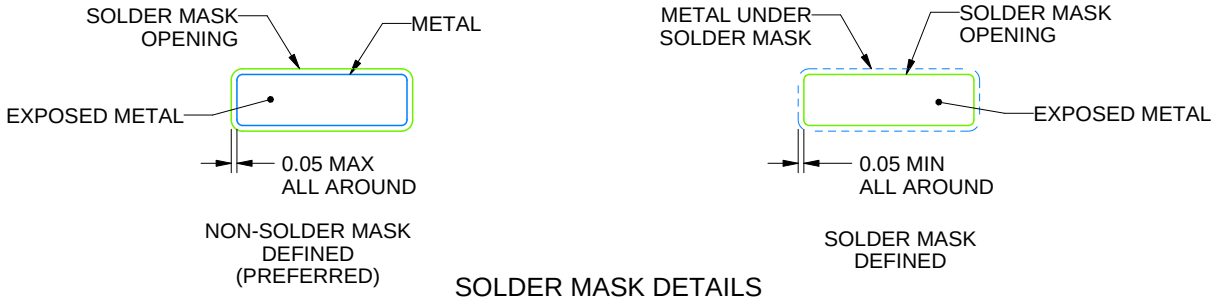



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

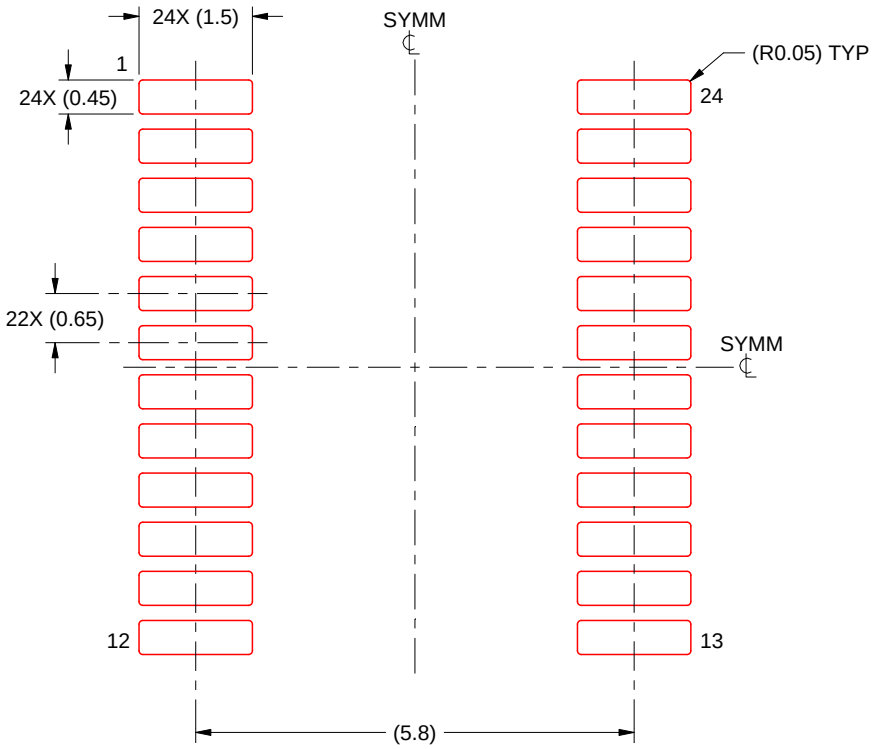



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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