

## SN74LVCC4245A 具有可配置输出电压和三态输出的八路双电源总线收发器

### 1 特性

- 双向电压转换器
- A 端口的电压范围为 4.5V 至 5.5V , B 端口的电压范围为 2.7V 至 5.5V
- 控制输入  $V_{IH}$  和  $V_{IL}$  电平以  $V_{CCA}$  电压为基准
- 闩锁性能超过 250mA , 符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 带电器件模型 (C101)

### 2 应用

- 电平转换
- 个人电子产品
- 工业
- 企业
- 电信

### 3 说明

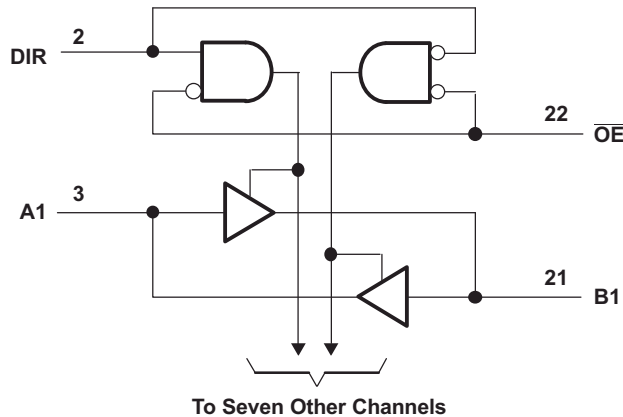
这款 8 位 ( 八路 ) 同相总线收发器采用两个独立的电源轨。A 端口  $V_{CCA}$  专用于接受 5V 电源电平, 可配置的 B 端口 ( 用于跟踪  $V_{CCB}$  ) 接受 3V 至 5V 的电压。这样可实现从 3.3V 到 5V 的环境转换, 反之亦然。

SN74LVCC4245A 器件旨在实现数据总线之间的异步通信。SN74LVCC4245A 器件根据方向控制 (DIR) 输入上的逻辑电平, 将数据从 A 总线发送至 B 总线, 或者将数据从 B 总线发送至 A 总线。输出使能 ( $\overline{OE}$ ) 输入可用于禁用器件, 这样可有效隔离总线。控制电路 ( DIR ,  $\overline{OE}$  ) 由  $V_{CCA}$  供电。

#### 封装信息<sup>(1)</sup>

| 器件型号          | 封装                | 封装尺寸 ( 标称值 )     |
|---------------|-------------------|------------------|
| SN74LVCC4245A | DB (SSOP, 24)     | 8.20mm × 5.30mm  |
|               | DW ( SOIC , 24 )  | 15.40mm × 7.50mm |
|               | NS ( SOP , 24 )   | 15.00mm × 5.30mm |
|               | PW ( TSSOP , 24 ) | 7.80mm × 4.40mm  |

(1) 如需了解可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 ( 正逻辑 )



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision M (March 2005) to Revision N (December 2022) | Page |
|--------------------------------------------------------------------|------|
| • 删除了订购信息.....                                                     | 1    |
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....                                     | 1    |
| • 添加了 引脚配置和功能、详细说明、应用和实施、布局 部分.....                                | 1    |
| • Added thermal values for PW package.....                         | 5    |

## 5 Pin Configuration and Functions

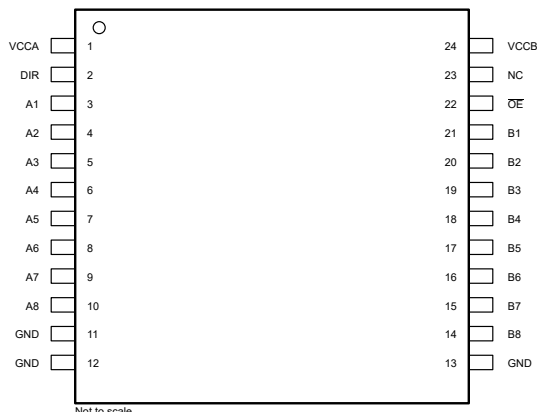


图 5-1. DB, DW, NS, or PW Package, SSOP, SOIC, SOP, or TSSOP (Top View)

表 5-1. Pin Functions

| PIN              |     | TYPE <sup>(1)</sup> | DESCRIPTION              |
|------------------|-----|---------------------|--------------------------|
| NAME             | NO. |                     |                          |
| V <sub>CCA</sub> | 1   | —                   | A port power             |
| DIR              | 2   | I                   | Dir input                |
| A1               | 3   | I/O                 | A1 port                  |
| A2               | 4   | I/O                 | A2 port                  |
| A3               | 5   | I/O                 | A3 port                  |
| A4               | 6   | I/O                 | A4 port                  |
| A5               | 7   | I/O                 | A5 port                  |
| A6               | 8   | I/O                 | A6 port                  |
| A7               | 9   | I/O                 | A7 port                  |
| A8               | 10  | I/O                 | A8 port                  |
| GND              | 11  | —                   | Ground                   |
| GND              | 12  | —                   |                          |
| GND              | 13  | —                   |                          |
| B8               | 14  | I/O                 | B8 port                  |
| B7               | 15  | I/O                 | B7 port                  |
| B6               | 16  | I/O                 | B6 port                  |
| B5               | 17  | I/O                 | B5 port                  |
| B4               | 18  | I/O                 | B4 port                  |
| B3               | 19  | I/O                 | B3 port                  |
| B2               | 20  | I/O                 | B2 port                  |
| B1               | 21  | I/O                 | B1 port                  |
| OE               | 22  | I                   | Output Enable active low |
| NC               | 23  | —                   | Unconnected              |
| V <sub>CCB</sub> | 24  | —                   | B port power             |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                        |                                                           |                    | MIN   | MAX             | UNIT |
|------------------------|-----------------------------------------------------------|--------------------|-------|-----------------|------|
| $V_{CCA}$<br>$V_{CCB}$ | Supply voltage range                                      |                    | - 0.5 | 6               | V    |
| $V_I$                  | Input voltage range <sup>(2)</sup>                        | I/O ports (A port) | - 0.5 | $V_{CCA} + 0.5$ | V    |
|                        |                                                           | I/O ports (B port) | - 0.5 | $V_{CCB} + 0.5$ |      |
|                        |                                                           | Except I/O ports   | - 0.5 | $V_{CCA} + 0.5$ |      |
| $V_O$                  | Output voltage range <sup>(2)</sup>                       | A port             | - 0.5 | $V_{CCA} + 0.5$ | V    |
|                        |                                                           | B port             | - 0.5 | $V_{CCB} + 0.5$ |      |
| $I_{IK}$               | Input clamp current                                       | $V_I < 0$          |       | - 50            | mA   |
| $I_{OK}$               | Output clamp current                                      | $V_O < 0$          |       | - 50            | mA   |
| $I_O$                  | Continuous output current                                 |                    |       | ±50             | mA   |
|                        | Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND |                    |       | ±100            | mA   |
| $\theta_{JA}$          | Package thermal impedance <sup>(3)</sup>                  | DW package         |       | 46              | °C/W |
|                        |                                                           | NS package         |       | 65              |      |
| $T_{stg}$              | Storage temperature range                                 |                    | - 65  | 150             | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 6 V maximum.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

### 6.2 ESD Ratings

| PARAMETER          |                         | DEFINITION                                                                               | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 2000  | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 1000  |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

(1)

|                  |                                                                           | V <sub>CCA</sub> | V <sub>CCB</sub> | MIN  | NOM | MAX              | UNIT |
|------------------|---------------------------------------------------------------------------|------------------|------------------|------|-----|------------------|------|
| V <sub>CCA</sub> | Supply voltage                                                            |                  |                  | 4.5  | 5   | 5.5              | V    |
| V <sub>CCB</sub> | Supply voltage                                                            |                  |                  | 2.7  | 3.3 | 5.5              | V    |
| V <sub>IHA</sub> | High-level input voltage                                                  | 4.5 V            | 2.7 V            | 2    |     |                  | V    |
|                  |                                                                           |                  | 3.6 V            | 2    |     |                  |      |
|                  |                                                                           | 5.5 V            | 5.5 V            | 2    |     |                  |      |
| V <sub>IHB</sub> | High-level input voltage                                                  | 4.5 V            | 2.7 V            | 2    |     |                  | V    |
|                  |                                                                           |                  | 3.6 V            | 2    |     |                  |      |
|                  |                                                                           | 5.5 V            | 5.5 V            | 3.85 |     |                  |      |
| V <sub>ILA</sub> | Low-level input voltage                                                   | 4.5 V            | 2.7 V            |      |     | 0.8              | V    |
|                  |                                                                           |                  | 3.6 V            |      |     | 0.8              |      |
|                  |                                                                           | 5.5 V            | 5.5 V            |      |     | 0.8              |      |
| V <sub>ILB</sub> | Low-level input voltage                                                   | 4.5 V            | 2.7 V            |      |     | 0.8              | V    |
|                  |                                                                           |                  | 3.6 V            |      |     | 0.8              |      |
|                  |                                                                           | 5.5 V            | 5.5 V            |      |     | 1.65             |      |
| V <sub>IH</sub>  | High-level input voltage (control pins) (referenced to V <sub>CCA</sub> ) | 4.5 V            | 2.7 V            | 2    |     |                  | V    |
|                  |                                                                           |                  | 3.6 V            | 2    |     |                  |      |
|                  |                                                                           | 5.5 V            | 5.5 V            | 2    |     |                  |      |
| V <sub>IL</sub>  | Low-level input voltage (control pins) (referenced to V <sub>CCA</sub> )  | 4.5 V            | 2.7 V            |      |     | 0.8              | V    |
|                  |                                                                           |                  | 3.6 V            |      |     | 0.8              |      |
|                  |                                                                           | 5.5 V            | 5.5 V            |      |     | 0.8              |      |
| V <sub>IA</sub>  | Input voltage                                                             |                  |                  | 0    |     | V <sub>CCA</sub> | V    |
| V <sub>IB</sub>  | Input voltage                                                             |                  |                  | 0    |     | V <sub>CCB</sub> | V    |
| V <sub>OA</sub>  | Output voltage                                                            |                  |                  | 0    |     | V <sub>CCA</sub> | V    |
| V <sub>OB</sub>  | Output voltage                                                            |                  |                  | 0    |     | V <sub>CCB</sub> | V    |
| I <sub>OHA</sub> | High-level output current                                                 | 4.5 V            | 3 V              |      |     | – 24             | mA   |
| I <sub>OHB</sub> | High-level output current                                                 | 4.5 V            | 2.7 V to 4.5 V   |      |     | – 24             | mA   |
| I <sub>OLA</sub> | Low-level output current                                                  | 4.5 V            | 3 V              |      |     | 24               | mA   |
| I <sub>OLB</sub> | Low-level output current                                                  | 4.5 V            | 2.7 V to 4.5 V   |      |     | 24               | mA   |
| T <sub>A</sub>   | Operating free-air temperature                                            |                  |                  | – 40 |     | 85               | °C   |

(1) All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                            | SN74LVCC4245A |           | UNIT |
|-------------------------------|--------------------------------------------|---------------|-----------|------|
|                               |                                            | PW (TSSOP)    | DB (SSOP) |      |
|                               |                                            | 24 PINS       | 24 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance     | 100.6         | 90.7      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance  | 44.7          | 51.9      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance       | 55.8          | 49.7      | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter | 6.8           | 18.8      | °C/W |

## 6.4 Thermal Information (continued)

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVCC4245A |           | UNIT |
|-------------------------------|----------------------------------------------|---------------|-----------|------|
|                               |                                              | PW (TSSOP)    | DB (SSOP) |      |
|                               |                                              | 24 PINS       | 24 PINS   |      |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 55.4          | 49.3      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                |                | TEST CONDITIONS                                                                                                           | V <sub>CCA</sub> | V <sub>CCB</sub> | MIN       | TYP     | MAX  | UNIT    |
|------------------------------------------|----------------|---------------------------------------------------------------------------------------------------------------------------|------------------|------------------|-----------|---------|------|---------|
| V <sub>OHA</sub>                         |                | I <sub>OH</sub> = -100 $\mu$ A                                                                                            | 4.5 V            | 3 V              | 4.4       | 4.49    |      | V       |
|                                          |                | I <sub>OH</sub> = -24 mA                                                                                                  | 4.5 V            | 3 V              | 3.76      | 4.25    |      |         |
| V <sub>OHB</sub>                         |                | I <sub>OH</sub> = -100 $\mu$ A                                                                                            | 4.5 V            | 3 V              | 2.9       | 2.99    |      | V       |
|                                          |                | I <sub>OH</sub> = -12 mA                                                                                                  | 4.5 V            | 2.7 V            | 2.2       | 2.5     |      |         |
|                                          |                |                                                                                                                           |                  | 3 V              | 2.46      | 2.85    |      |         |
|                                          |                | I <sub>OH</sub> = -24 mA                                                                                                  | 4.5 V            | 2.7 V            | 2.1       | 2.3     |      |         |
|                                          |                |                                                                                                                           |                  | 3 V              | 2.25      | 2.65    |      |         |
|                                          |                |                                                                                                                           |                  | 4.5 V            | 3.76      | 4.25    |      |         |
| V <sub>OLA</sub>                         |                | I <sub>OL</sub> = 100 $\mu$ A                                                                                             | 4.5 V            | 3 V              |           |         | 0.1  | V       |
|                                          |                | I <sub>OL</sub> = 24 mA                                                                                                   | 4.5 V            | 3 V              |           | 0.21    | 0.44 |         |
| V <sub>OLB</sub>                         |                | I <sub>OL</sub> = 100 $\mu$ A                                                                                             | 4.5 V            | 3 V              |           |         | 0.1  | V       |
|                                          |                | I <sub>OL</sub> = 12 mA                                                                                                   | 4.5 V            | 2.7 V            |           | 0.11    | 0.44 |         |
|                                          |                | I <sub>OL</sub> = 24 mA                                                                                                   | 4.5 V            | 2.7 V            |           | 0.22    | 0.5  |         |
|                                          |                |                                                                                                                           |                  | 3 V              |           | 0.21    | 0.44 |         |
|                                          |                |                                                                                                                           |                  | 4.5 V            |           | 0.18    | 0.44 |         |
| I <sub>I</sub>                           | Control inputs | V <sub>I</sub> = V <sub>CCA</sub> or GND                                                                                  | 5.5 V            | 3.6 V            | $\pm 0.1$ | $\pm 1$ |      | $\mu$ A |
|                                          |                |                                                                                                                           |                  | 5.5 V            | $\pm 0.1$ | $\pm 1$ |      |         |
| I <sub>OZ</sub> <sup>(1)</sup>           | A or B ports   | V <sub>O</sub> = V <sub>CCA/B</sub> or GND, V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                           | 5.5 V            | 3.6 V            | $\pm 0.5$ | $\pm 5$ |      | $\mu$ A |
| I <sub>CCA</sub>                         | B to A         | A <sub>n</sub> = V <sub>CC</sub> or GND                                                                                   | 5.5 V            | Open             |           | 8       | 80   | $\mu$ A |
|                                          |                | I <sub>O</sub> (A port) = 0, B <sub>n</sub> = V <sub>CCB</sub> or GND                                                     | 5.5 V            | 3.6 V            |           | 8       | 80   |         |
|                                          |                |                                                                                                                           |                  | 5.5 V            |           | 8       | 80   |         |
| I <sub>CCB</sub>                         | A to B         | A <sub>n</sub> = V <sub>CCA</sub> or GND, I <sub>O</sub> (B port) = 0                                                     | 5.5 V            | 3.6 V            |           | 5       | 50   | $\mu$ A |
|                                          |                |                                                                                                                           |                  | 5.5 V            |           | 8       | 80   |         |
| $\Delta$ I <sub>CCA</sub> <sup>(2)</sup> | A port         | V <sub>I</sub> = V <sub>CCA</sub> - 2.1 V, Other inputs at V <sub>CCA</sub> or GND, OE at GND and DIR at V <sub>CCA</sub> | 5.5 V            | 5.5 V            |           | 1.35    | 1.5  | mA      |
|                                          | OE             | V <sub>I</sub> = V <sub>CCA</sub> - 2.1 V, Other inputs at V <sub>CCA</sub> or GND, DIR at V <sub>CCA</sub> or GND        | 5.5 V            | 5.5 V            |           | 1       | 1.5  |         |
|                                          | DIR            | V <sub>I</sub> = V <sub>CCA</sub> - 2.1 V, Other inputs at V <sub>CCA</sub> or GND, OE at V <sub>CCA</sub> or GND         | 5.5 V            | 3.6 V            |           | 1       | 1.5  |         |
| $\Delta$ I <sub>CCB</sub> <sup>(2)</sup> | B port         | V <sub>I</sub> = V <sub>CCB</sub> - 0.6 V, Other inputs at V <sub>CCB</sub> or GND, OE at GND and DIR at GND              | 5.5 V            | 3.6 V            |           | 0.35    | 0.5  | mA      |
| C <sub>i</sub>                           | Control inputs | V <sub>I</sub> = V <sub>CCA</sub> or GND                                                                                  | Open             | Open             |           | 5       |      | pF      |
| C <sub>io</sub>                          | A or B ports   | V <sub>O</sub> = V <sub>CCA/B</sub> or GND                                                                                | 5 V              | 3.3 V            |           | 11      |      | pF      |

- (1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

- (2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V<sub>CC</sub>.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see 图 8-1 through 图 11-1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ ,<br>$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ |     | $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ ,<br>$V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$ |      | UNIT |
|-----------|-----------------|----------------|--------------------------------------------------------------------------------------|-----|----------------------------------------------------------------------------------------|------|------|
|           |                 |                | MIN                                                                                  | MAX | MIN                                                                                    | MAX  |      |
| $t_{PHL}$ | A               | B              | 1                                                                                    | 7.1 | 1                                                                                      | 7    | ns   |
| $t_{PLH}$ |                 |                | 1                                                                                    | 6   | 1                                                                                      | 7    |      |
| $t_{PHL}$ | B               | A              | 1                                                                                    | 6.8 | 1                                                                                      | 6.2  | ns   |
| $t_{PLH}$ |                 |                | 1                                                                                    | 6.1 | 1                                                                                      | 5.3  |      |
| $t_{PZL}$ | $\overline{OE}$ | A              | 1                                                                                    | 9   | 1                                                                                      | 9    | ns   |
| $t_{PZH}$ |                 |                | 1                                                                                    | 8.3 | 1                                                                                      | 8    |      |
| $t_{PZL}$ | $\overline{OE}$ | B              | 1                                                                                    | 8.2 | 1                                                                                      | 10   | ns   |
| $t_{PZH}$ |                 |                | 1                                                                                    | 8.1 | 1                                                                                      | 10.2 |      |
| $t_{PLZ}$ | $\overline{OE}$ | A              | 1                                                                                    | 4.7 | 1                                                                                      | 5.2  | ns   |
| $t_{PHZ}$ |                 |                | 1                                                                                    | 4.9 | 1                                                                                      | 5.2  |      |
| $t_{PLZ}$ | $\overline{OE}$ | B              | 1                                                                                    | 5.4 | 1                                                                                      | 5.9  | ns   |
| $t_{PHZ}$ |                 |                | 1                                                                                    | 6.3 | 1                                                                                      | 7.4  |      |

## 6.7 Operating Characteristics

$V_{CCA} = 5\text{ V}$ ,  $V_{CCB} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                                               | TEST CONDITIONS  |                                 | TYP | UNIT |
|-----------|-----------------------------------------------|------------------|---------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per transceiver | Outputs enabled  | $C_L = 0$ , $f = 10\text{ MHz}$ | 20  | pF   |
|           |                                               | Outputs disabled |                                 | 6.5 |      |

## 6.8 Typical Characteristics

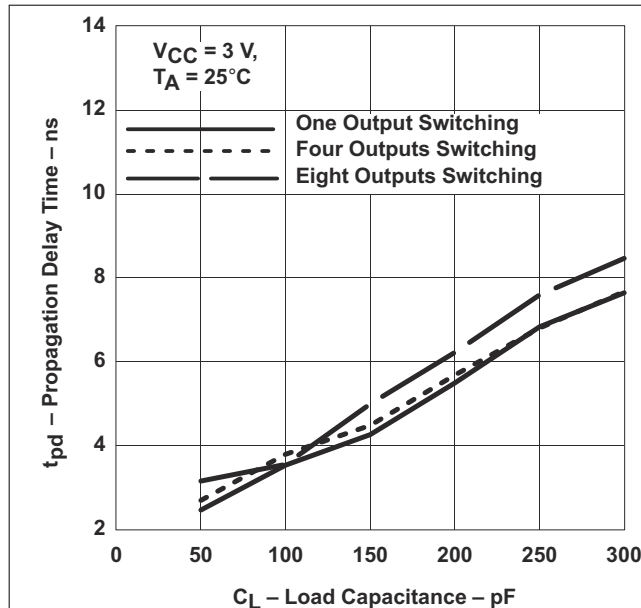


图 6-1. Propagation Delay (Low to High Transition) vs Load Capacitance

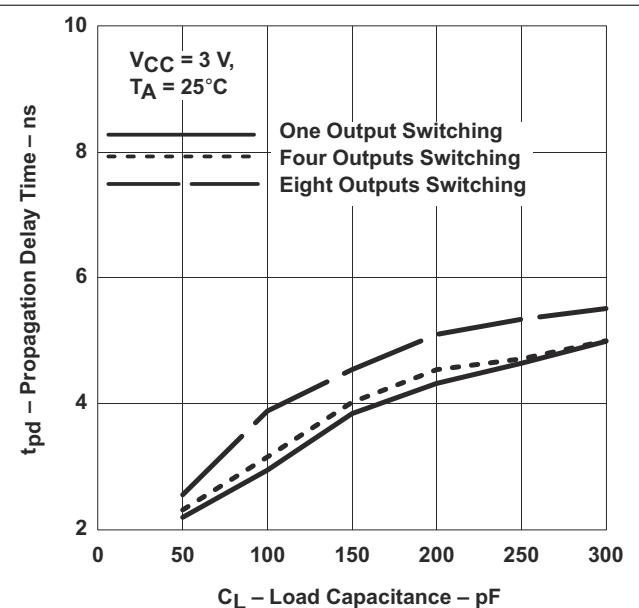


图 6-2. Propagation Delay (High to Low Transition) vs Load Capacitance

## 7 Power-Up Consideration

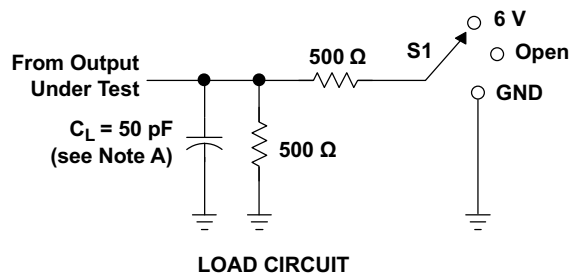
TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pull up resistor so that it ramps with  $V_{CCA}$ .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), then ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

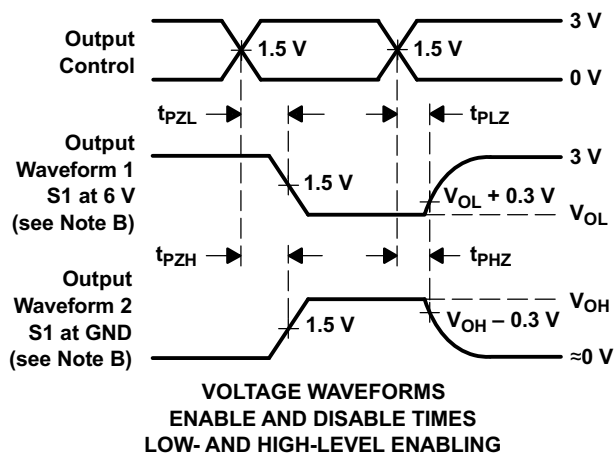
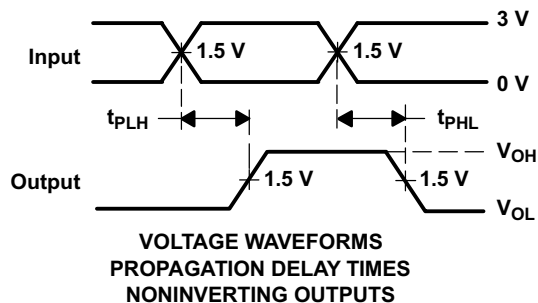
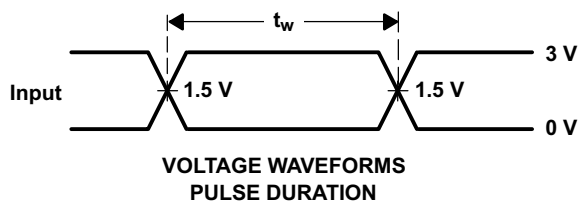
For more information, refer to the [Voltage-Level-Translation Devices](#) application note.

## 8 Parameter Measurement Information For A to B

$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  and  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$



| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |

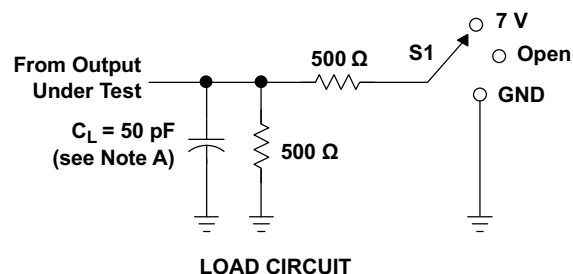


- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

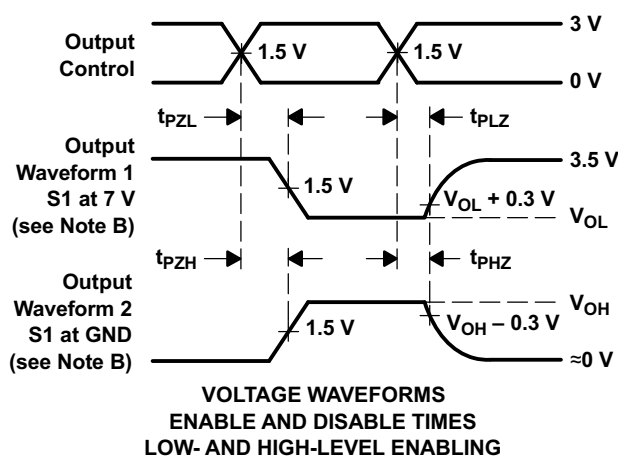
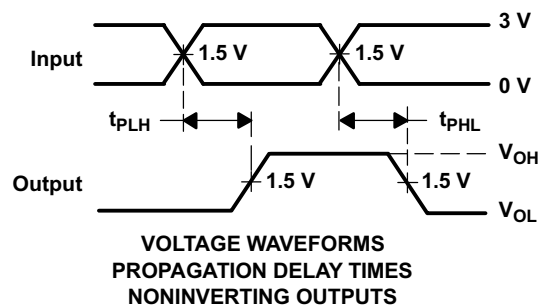
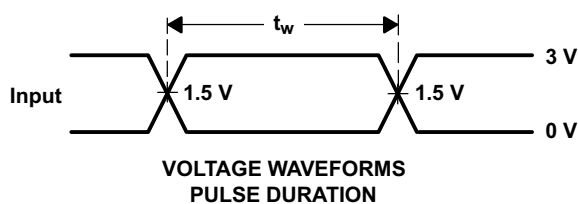
图 8-1. Load Circuit and Voltage Waveforms

## 9 Parameter Measurement Information For A to B

$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  and  $V_{CCB} = 3.6\text{ V to }5.5\text{ V}$



| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |

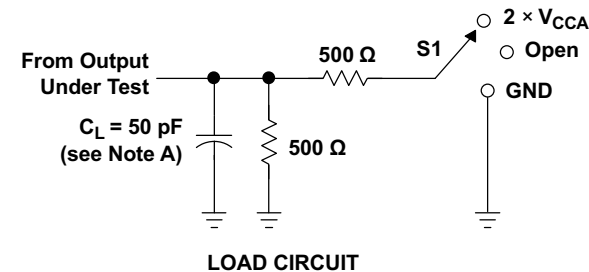


- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

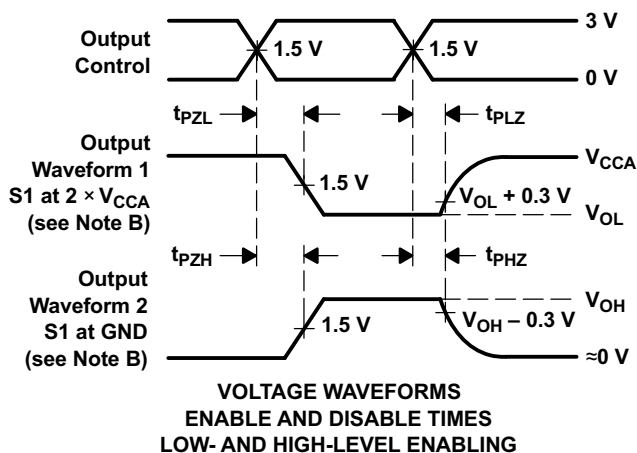
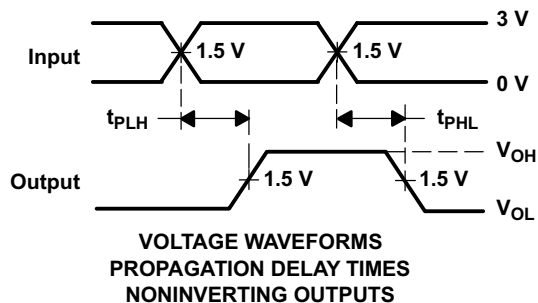
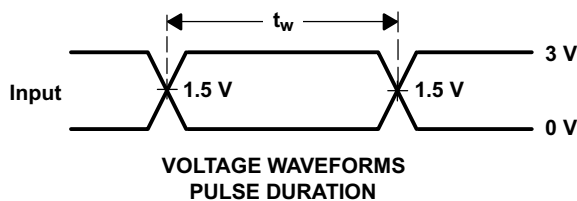
图 9-1. Load Circuit and Voltage Waveforms

## 10 Parameter Measurement Information For B to A

$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  and  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$



| TEST              | S1                 |
|-------------------|--------------------|
| $t_{PLH}/t_{PHL}$ | Open               |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CCA}$ |
| $t_{PHZ}/t_{PZH}$ | GND                |

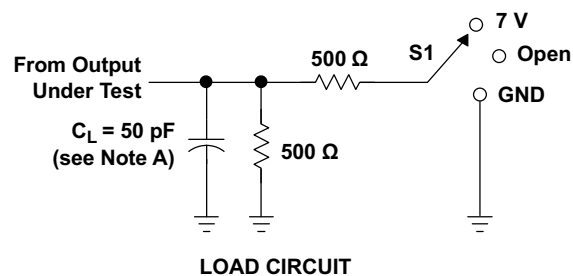


- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

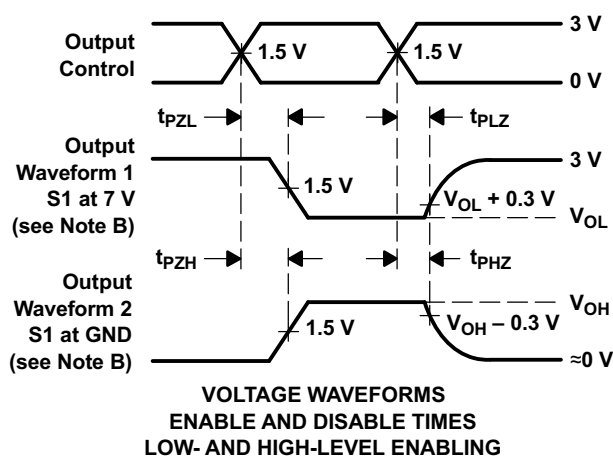
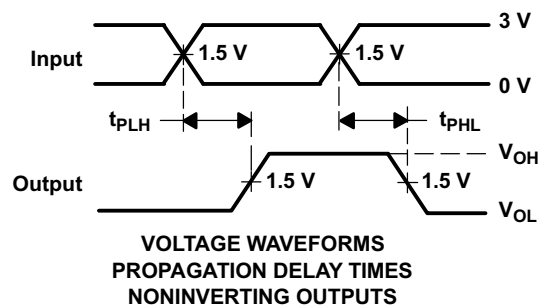
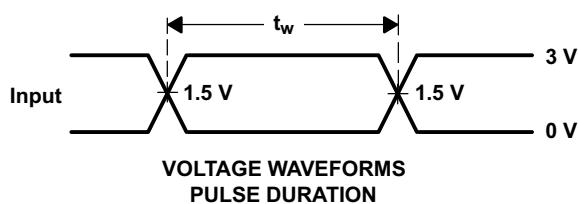
图 10-1. Load Circuit and Voltage Waveforms

## 11 Parameter Measurement Information For B to A

$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  and  $V_{CCB} = 3.6\text{ V to }5.5\text{ V}$



| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

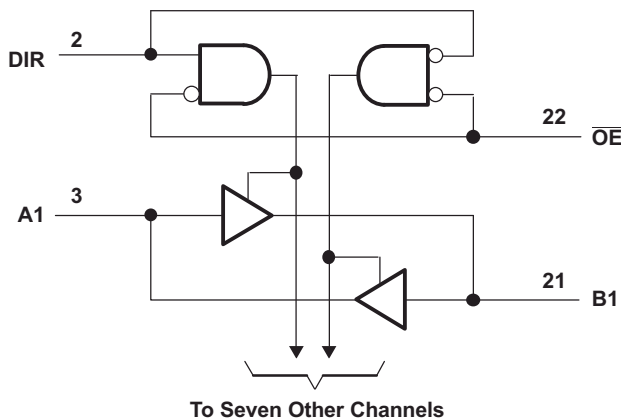
**图 11-1. Load Circuit and Voltage Waveforms**

## 12 Detailed Description

### 12.1 Overview

SN74LVCC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has  $V_{CCB}$ , which is set at 3.3 V, and A port has  $V_{CCA}$ , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

### 12.2 Functional Block Diagram



### 12.3 Feature Description

- 24 mA drive at 3-V supply
  - Good for heavier loads and longer traces
- Low  $V_{IH}$ 
  - Allows 3.3-V to 5-V translation

### 12.4 Device Functional Modes

表 12-1. Function Table  
(Each Transceiver)

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

## 13 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 13.1 Application Information

The SN74LVCC4245A device pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2 - 11 and 14 - 23 of the SN74LVCC4245A to align with the conventional SN74LVCC4245A device's pinout. SN74LVCC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 13.2 Typical Application

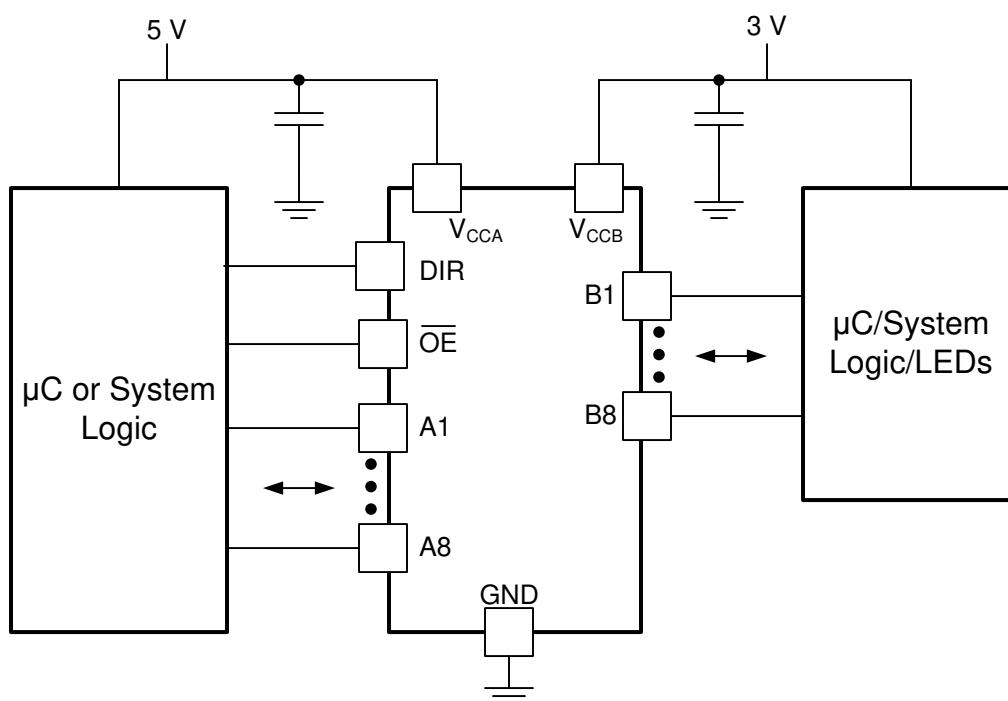


图 13-1. Typical Application Schematic

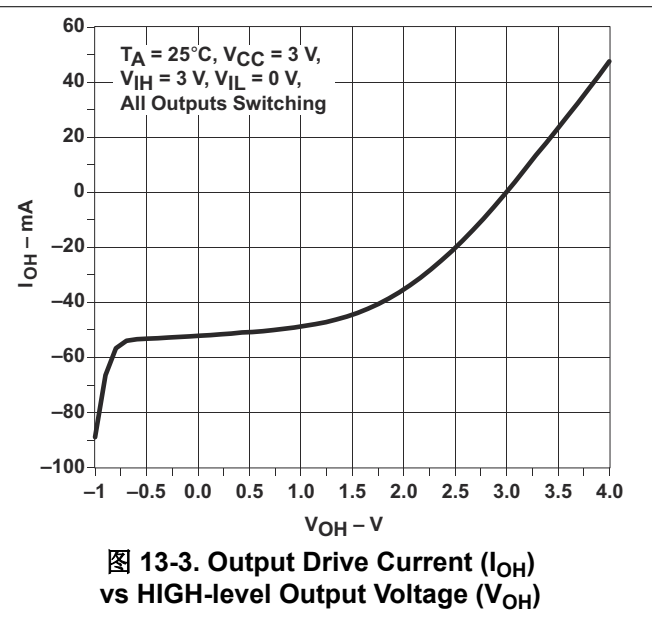
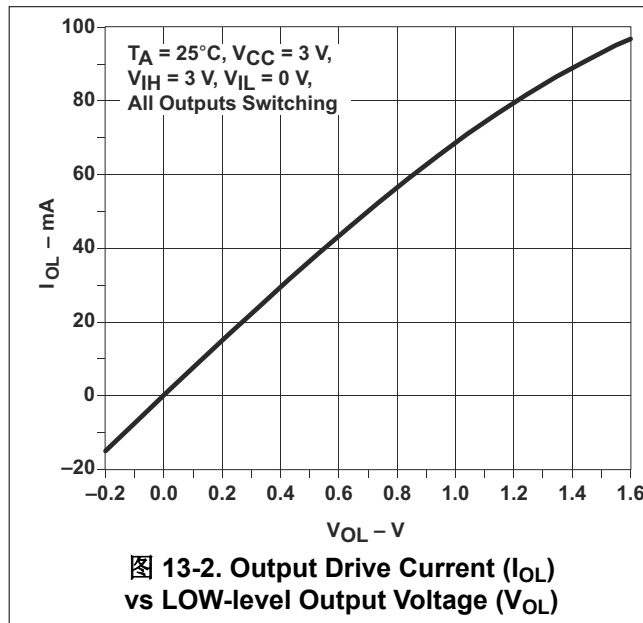
#### 13.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 13.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - For rise time and fall time specifications, see ( $\Delta t / \Delta V$ ) in the 节 6.3 table.
  - For specified high and low levels, see ( $V_{IH}$  and  $V_{IL}$ ) in the 节 6.3 table.
- Recommend Output Conditions:
  - Load currents should not exceed ( $I_O$  max) per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the 节 6.1 table.
  - Outputs should not be pulled above  $V_{CC}$ .
  - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

### 13.2.3 Application Curves



## 14 Power Supply Recommendations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. Take these precautions to guard against such power-up problems:

- Connect ground before any supply voltage is applied.
- Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
- Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
- Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), then ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

## 15 Layout

### 15.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 15-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 15.2 Layout Example

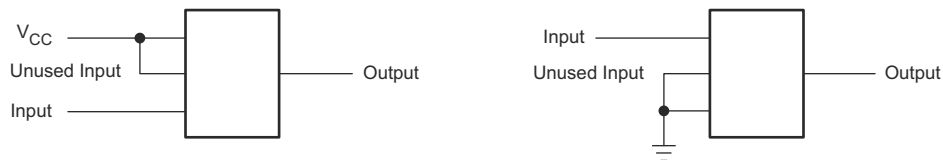


图 15-1. Layout Diagram

## 16 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 16.1 Documentation Support

#### 16.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Voltage-Level-Translation Devices application note](#)

### 16.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 16.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 16.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 16.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 16.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVCC4245ADBR</a>   | Active        | Production           | SSOP (DB)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245ADBR.B                 | Active        | Production           | SSOP (DB)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245ADBRG4.B               | Active        | Production           | SSOP (DB)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| <a href="#">SN74LVCC4245ADW</a>    | Active        | Production           | SOIC (DW)   24  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ADW.B                  | Active        | Production           | SOIC (DW)   24  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ADWE4                  | Active        | Production           | SOIC (DW)   24  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| <a href="#">SN74LVCC4245ADWR</a>   | Active        | Production           | SOIC (DW)   24  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ADWR.B                 | Active        | Production           | SOIC (DW)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| <a href="#">SN74LVCC4245ADWRG4</a> | Active        | Production           | SOIC (DW)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ADWRG4.B               | Active        | Production           | SOIC (DW)   24  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| <a href="#">SN74LVCC4245ANSR</a>   | Active        | Production           | SOP (NS)   24   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ANSR.B                 | Active        | Production           | SOP (NS)   24   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| SN74LVCC4245ANSRG4.B               | Active        | Production           | SOP (NS)   24   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVCC4245A           |
| <a href="#">SN74LVCC4245APW</a>    | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APW.B                  | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| <a href="#">SN74LVCC4245APWR</a>   | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APWR.A                 | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APWRE4                 | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APWRG4                 | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| <a href="#">SN74LVCC4245APWT</a>   | Active        | Production           | TSSOP (PW)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APWT.B                 | Active        | Production           | TSSOP (PW)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |
| SN74LVCC4245APWTE4                 | Active        | Production           | TSSOP (PW)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LG245A              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVCC4245A :**

- Enhanced Product : [SN74LVCC4245A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVCC4245ADBR   | SSOP         | DB              | 24   | 2000 | 330.0              | 16.4               | 8.2     | 8.8     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVCC4245ADWR   | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVCC4245ADWRG4 | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVCC4245ANSR   | SOP          | NS              | 24   | 2000 | 330.0              | 24.4               | 8.3     | 15.4    | 2.6     | 12.0    | 24.0   | Q1            |
| SN74LVCC4245APWR   | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVCC4245APWR   | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVCC4245APWT   | TSSOP        | PW              | 24   | 250  | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



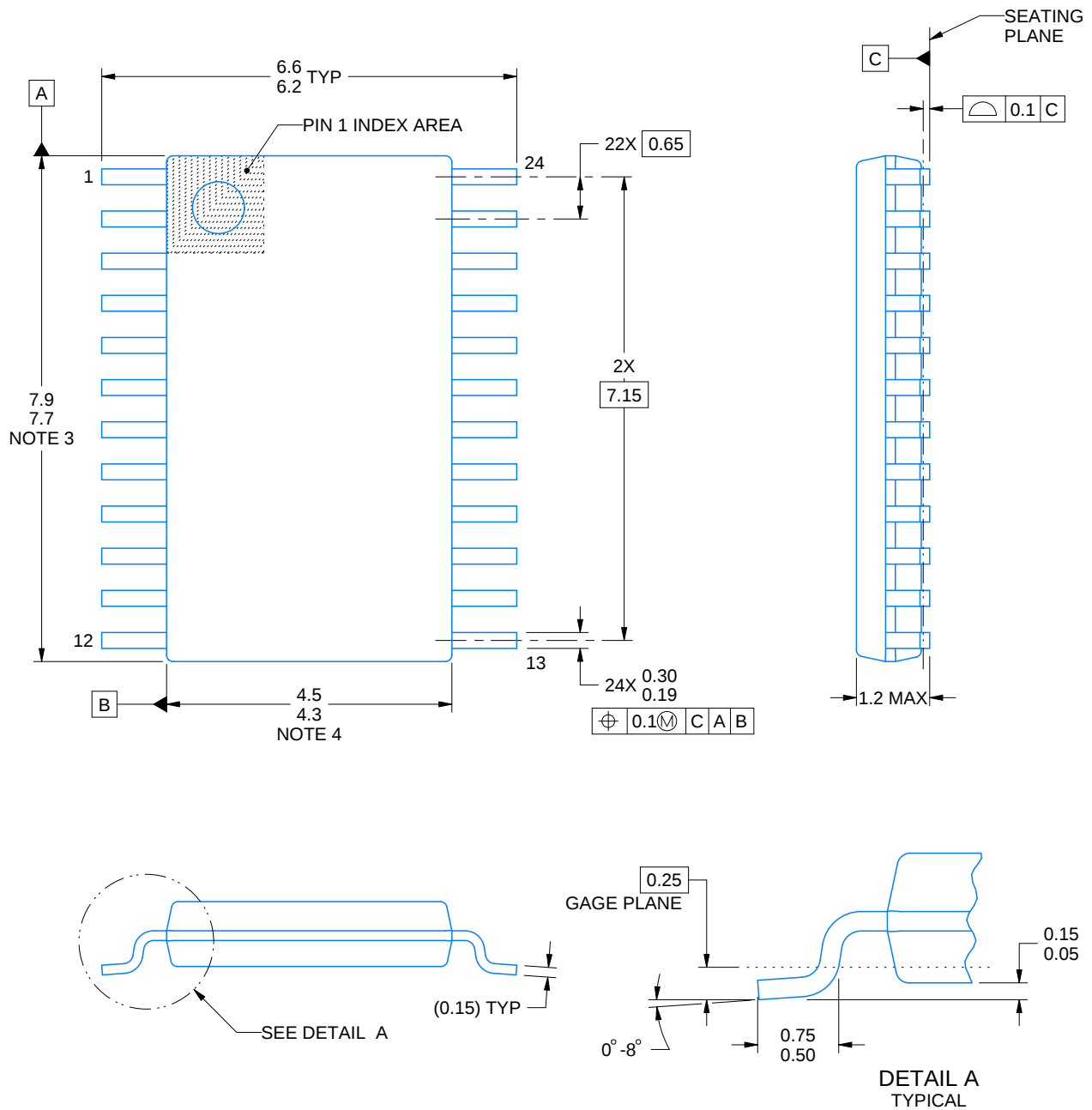
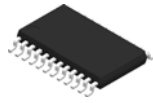
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVCC4245ADBR   | SSOP         | DB              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVCC4245ADWR   | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |
| SN74LVCC4245ADWRG4 | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |
| SN74LVCC4245ANSR   | SOP          | NS              | 24   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVCC4245APWR   | TSSOP        | PW              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVCC4245APWR   | TSSOP        | PW              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVCC4245APWT   | TSSOP        | PW              | 24   | 250  | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVCC4245ADW   | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74LVCC4245ADW.B | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74LVCC4245ADWE4 | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74LVCC4245APW   | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVCC4245APW.B | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |



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## NOTES:

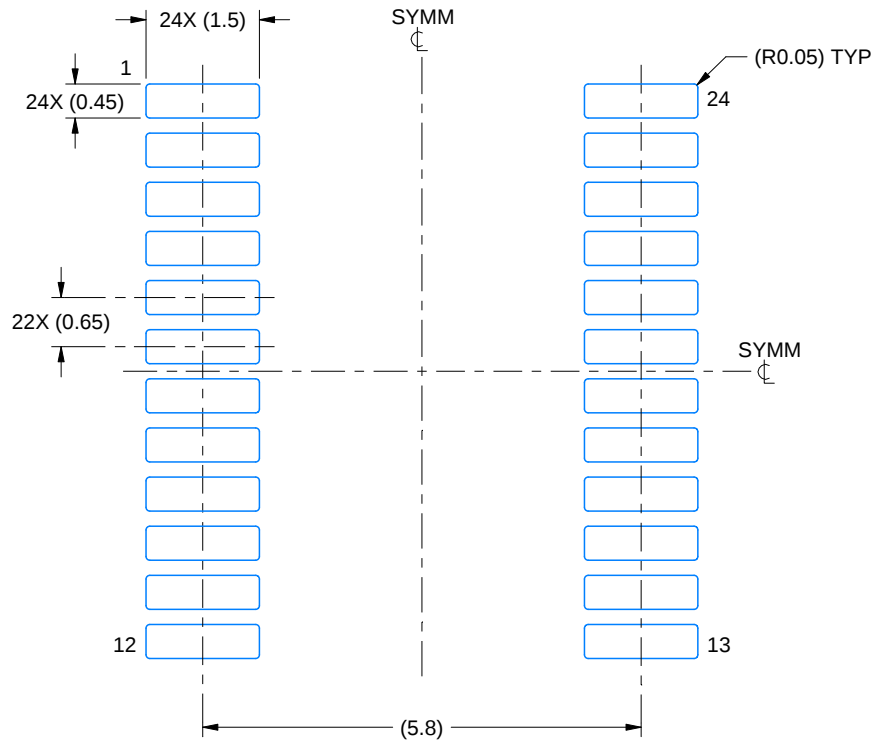
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

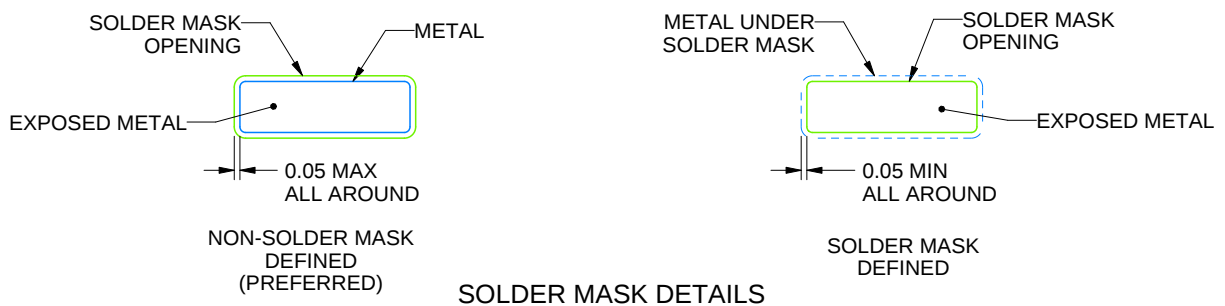
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

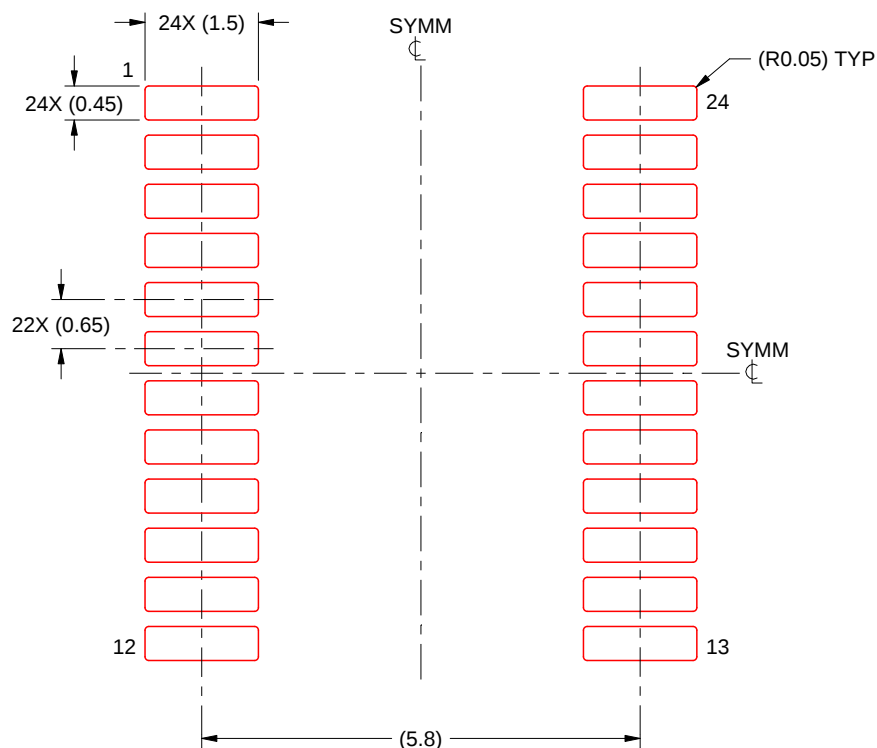
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

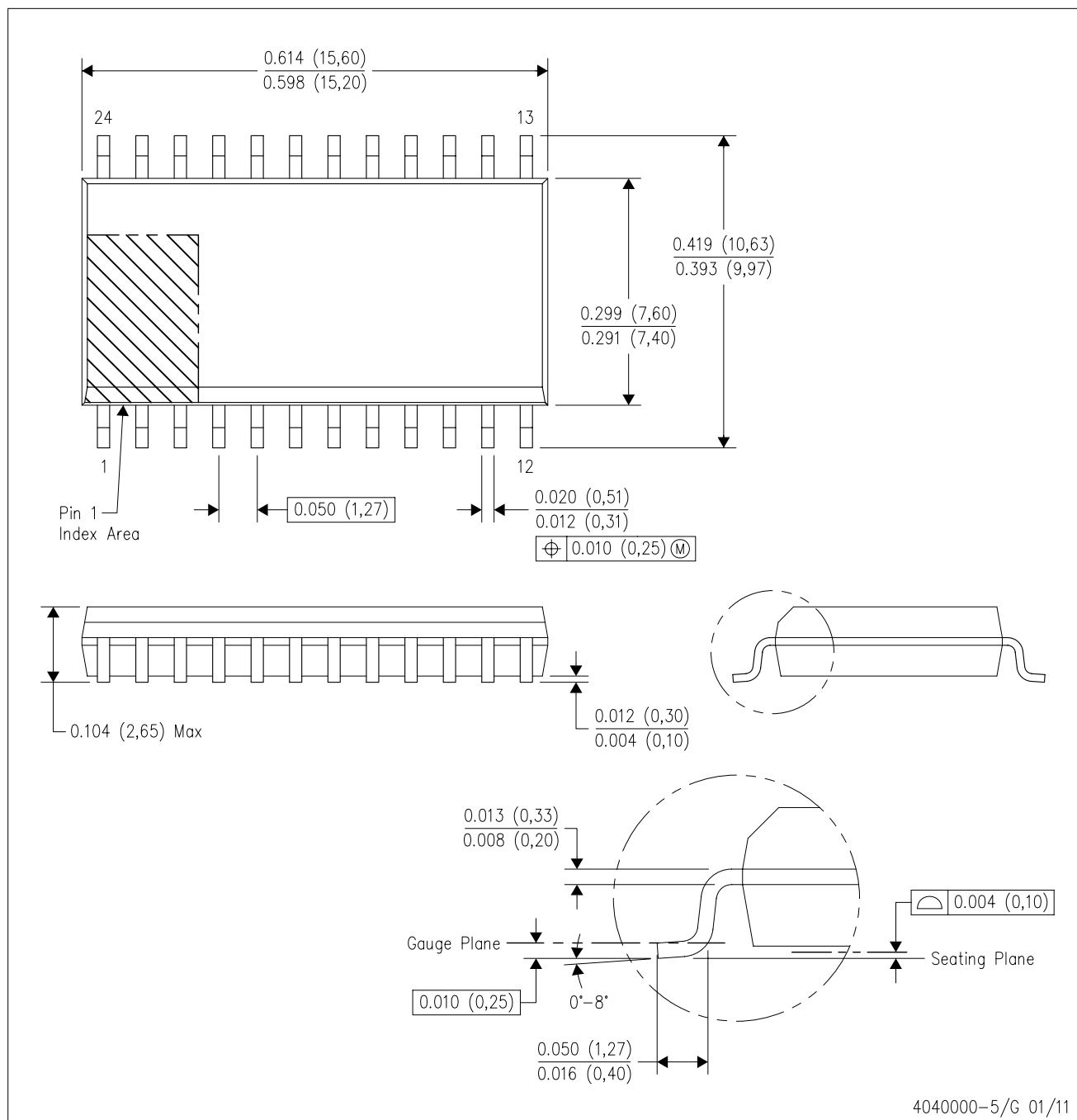
14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R-PDSO-G24)

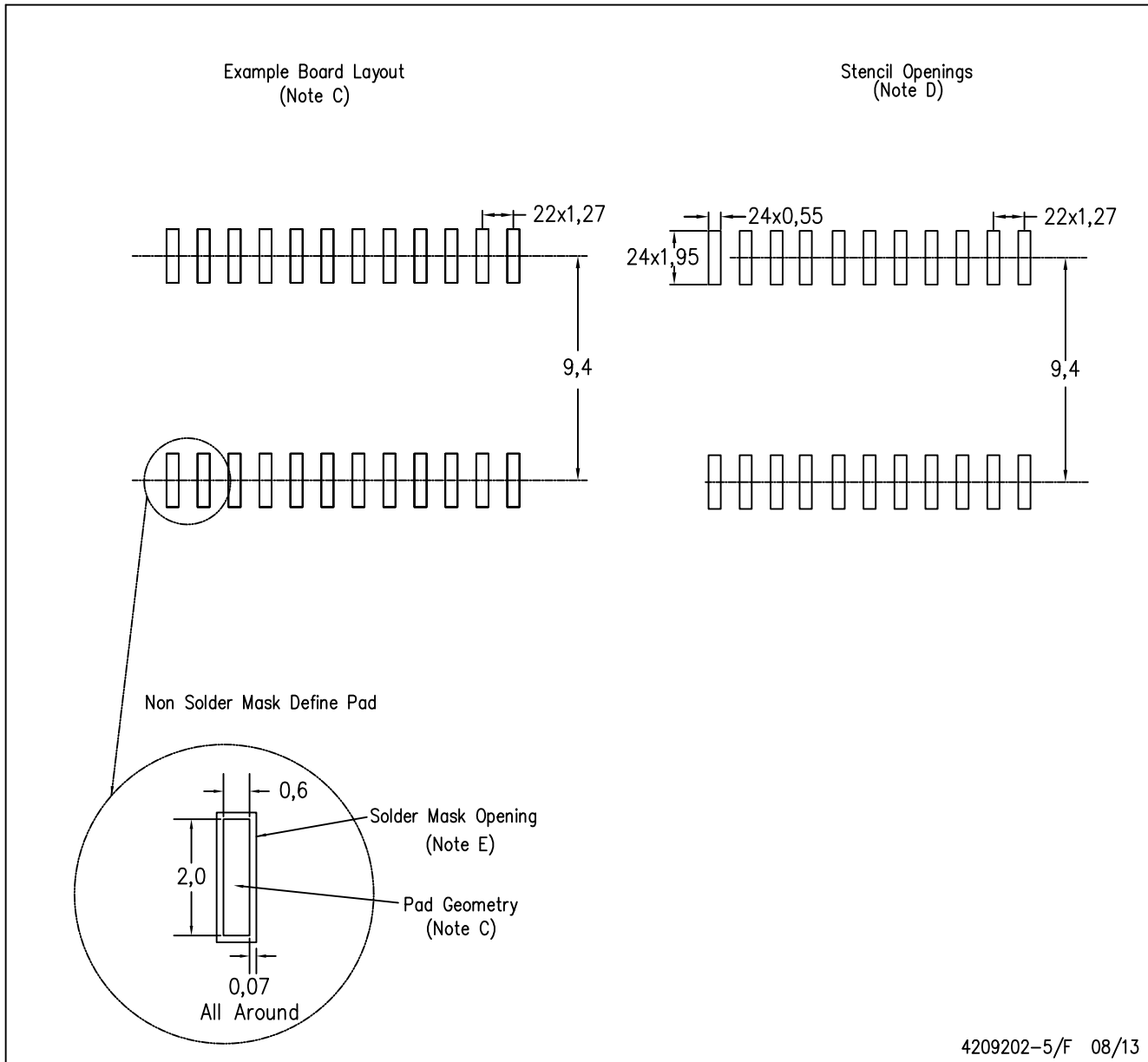
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

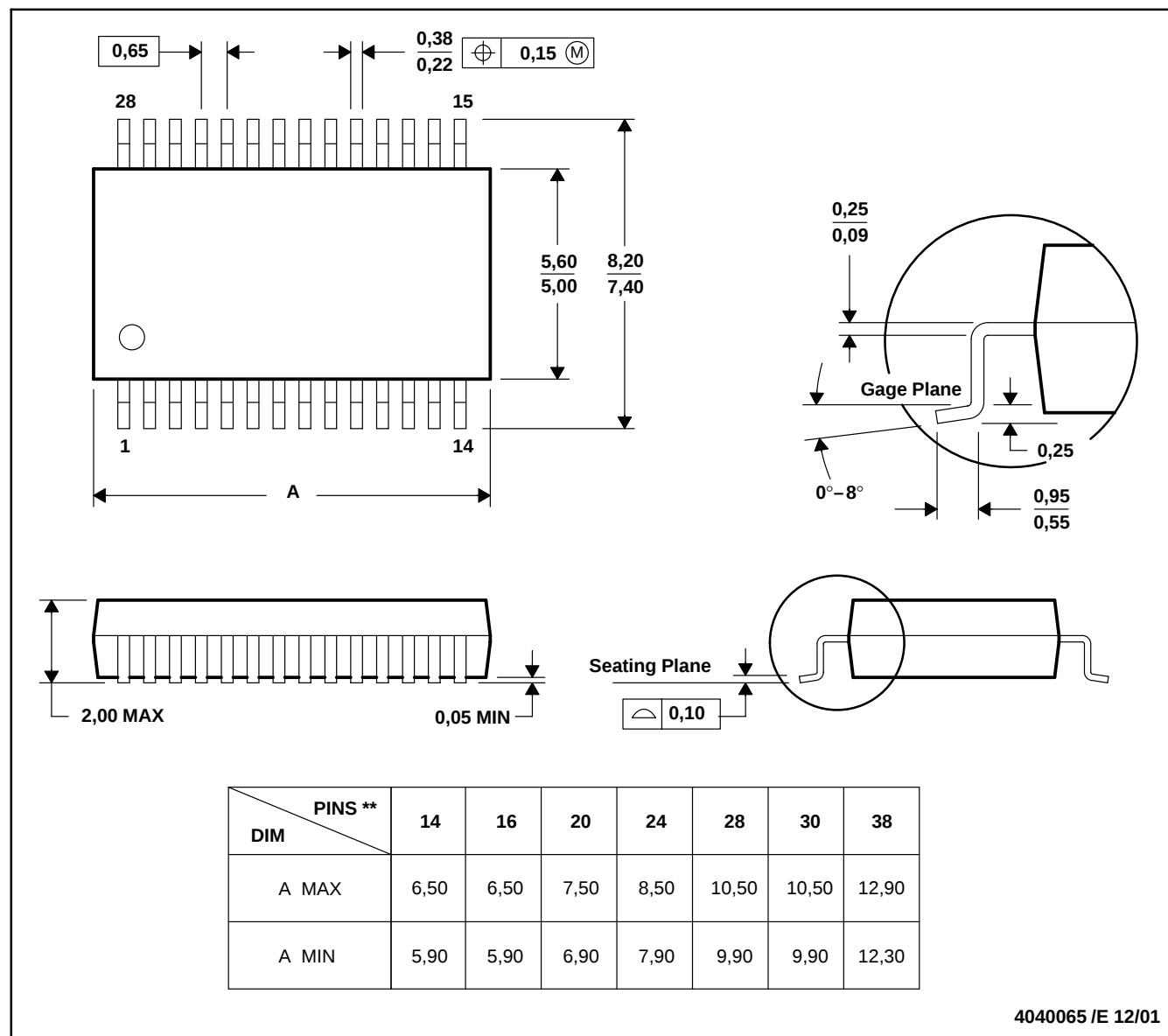


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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