

## SN74LVC2G125 Dual Bus Buffer Gate With 3-State Outputs

### 1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.3 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the  $V_{CC}$  Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

### 2 Applications

- Cable Modem Termination Systems
- High-Speed Data Acquisition and Generation
- Military: Radars and Sonars
- Motor Controls: High-Voltage
- Power Line Communication Modems
- SSDs: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platforms
- Video Broadcasting: IP-Based Multi-Format Transcoders
- Video Communications Systems

### 3 Description

The SN74LVC2G125 device is a dual bus buffer gate, designed for 1.65-V to 5.5-V  $V_{CC}$  operation. This device features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

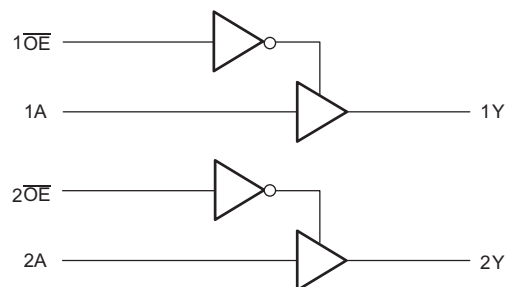
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information<sup>(1)</sup>

| PART NUMBER      | PACKAGE   | BODY SIZE         |
|------------------|-----------|-------------------|
| SN74LVC2G125DCTR | SM8 (8)   | 2.95 mm × 2.80 mm |
| SN74LVC2G125DCUR | VSSOP (8) | 2.30 mm × 2.00 mm |
| SN74LVC2G125YZPR | DSBGA (8) | 1.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision P (January 2016) to Revision Q                                                                                                                                                                  | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Removed '200-V Machine Model' from Features for consistency with ESD ratings table. ....                                                                                                                              | 1    |
| Added orderable part numbers associated with each package. Changed US8 to VSSOP. ....                                                                                                                                 | 1    |
| Updated YZP package drawing to match mechanical drawing pinout. ....                                                                                                                                                  | 4    |
| Added YZP pin identifiers to Pin Function table. Added 'buffer #' to Description for pins 2, 3, 5, and 6. Changed 'Power pin' to 'Positive supply' .....                                                              | 4    |
| Added updated package thermal values based on new models. Changes: $R_{\theta JA}$ DCT 220 -> 199.0, DCU 227 -> 217.8, YZP 102 -> 99.8. Added: $R_{\theta JCTop}$ , $R_{\theta JB}$ , $\Psi_{JT}$ , $\Psi_{JB}$ ..... | 6    |
| Added 'Balanced Push-Pull Outputs,' 'CMOS Inputs,' 'Clamp Diodes,' 'Partial Power Down,' 'Over-voltage Tolerant Inputs.' Removed bullet list. ....                                                                    | 10   |
| Added improved layout guidelines and trace example image. ....                                                                                                                                                        | 13   |
| Added <i>Documentation Support</i> section, <i>Receiving Notification of Documentation Updates</i> section, and <i>Community Resources</i> section .....                                                              | 15   |

| Changes from Revision O (January 2015) to Revision P                                                               | Page |
|--------------------------------------------------------------------------------------------------------------------|------|
| Added overbar for active low to $1\overline{OE}$ and $2\overline{OE}$ to the <i>Simplified Schematic</i> .....     | 1    |
| Added $T_J$ Junction temperature to the <i>Absolute Maximum Ratings</i> .....                                      | 5    |
| Added overbar for active low to $1\overline{OE}$ and $2\overline{OE}$ to the <i>Functional Block Diagram</i> ..... | 10   |

| Changes from Revision N (November 2013) to Revision O                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... | 1    |

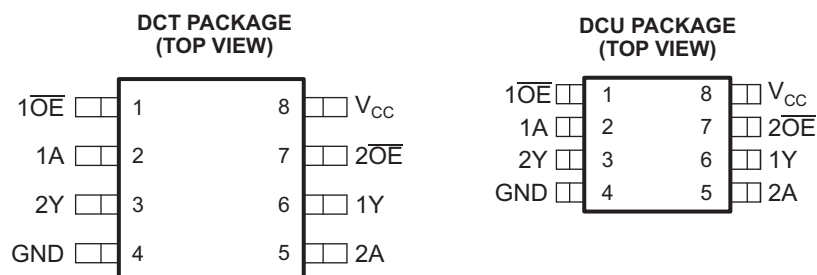
| Changes from Revision M (January 2007) to Revision N                                                | Page              |
|-----------------------------------------------------------------------------------------------------|-------------------|
| • Updated <i>Features</i> . .....                                                                   | <a href="#">1</a> |
| • Updated document to new TI data sheet format. ....                                                | <a href="#">1</a> |
| • Removed Ordering Information table. ....                                                          | <a href="#">1</a> |
| • Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table. .... | <a href="#">6</a> |

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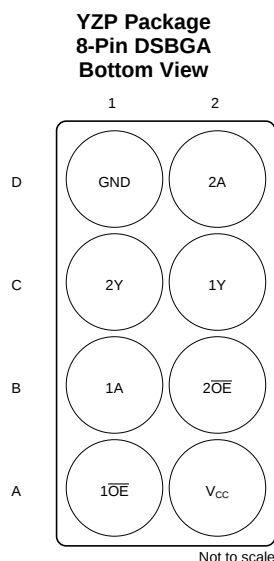
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## 5 Pin Configuration and Functions



See mechanical drawings for dimensions.



See mechanical drawings for dimensions.

### Pin Functions

| PIN             |          |     | TYPE | DESCRIPTION                |
|-----------------|----------|-----|------|----------------------------|
| NAME            | DCT, DCU | YZP |      |                            |
| 1A              | 2        | B1  | I    | Input of buffer 1          |
| 2A              | 5        | D2  | I    | Input of buffer 2          |
| 1OE             | 1        | A1  | I    | Output Enable for buffer 1 |
| 2OE             | 7        | B2  | I    | Output Enable for buffer 2 |
| 1Y              | 6        | C2  | O    | Output of buffer 1         |
| 2Y              | 3        | C1  | O    | Output of buffer 2         |
| GND             | 4        | D1  | —    | Ground                     |
| V <sub>CC</sub> | 8        | A2  | —    | Positive supply            |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See<sup>(1)</sup>

|                  |                                                                                             |                    | MIN  | MAX                   | UNIT |
|------------------|---------------------------------------------------------------------------------------------|--------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                                                              |                    | −0.5 | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                                                                |                    | −0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> |                    | −0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              |                    | −0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0 | −50  |                       | mA   |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0 | −50  |                       | mA   |
| I <sub>O</sub>   | Continuous output current                                                                   |                    | ±50  |                       | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                    | ±100 |                       | mA   |
| T <sub>J</sub>   | Junction temperature                                                                        |                    | 150  |                       | °C   |
| T <sub>stg</sub> | Storage temperature                                                                         |                    | −65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

|             |                         |                                                                                | VALUE | UNIT |
|-------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | 2000  | V    |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 1000  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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### 6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | MIN                                             | MAX                    | UNIT            |      |
|-----------------|------------------------------------|-------------------------------------------------|------------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                                       | 1.65                   | 5.5             | V    |
|                 |                                    | Data retention only                             | 1.5                    |                 |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.65 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 1.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 2                      |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.7 × V <sub>CC</sub>  |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.35 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 0.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 0.8                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.3 × V <sub>CC</sub>  |                 |      |
| V <sub>I</sub>  | Input voltage                      | 0                                               | 5.5                    | V               |      |
| V <sub>O</sub>  | Output voltage                     | High or low state                               | 0                      | V <sub>CC</sub> | V    |
|                 |                                    | 3-state                                         | 0                      | 5.5             |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V                        | –4                     |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         | –8                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           | –16                    |                 |      |
|                 |                                    |                                                 | –24                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         | –32                    |                 |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V                        | 4                      |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         | 8                      |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           | 16                     |                 |      |
|                 |                                    |                                                 | 24                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         | 32                     |                 |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | 20                     |                 | ns/V |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V                 | 10                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V                   | 5                      |                 |      |
| T <sub>A</sub>  | Operating free-air temperature     | –40                                             | 125                    | °C              |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC2G125 |             |             | UNIT |
|-------------------------------|----------------------------------------------|--------------|-------------|-------------|------|
|                               |                                              | DCT (SM8)    | DCU (VSSOP) | YZP (DSBGA) |      |
|                               |                                              | 8 PINS       | 8 PINS      | 8 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 199.0        | 217.8       | 99.8        | °C/W |
| R <sub>θJCTop</sub>           | Junction-to-case (top) thermal resistance    | 89.5         | 98.3        | 1.0         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 118.7        | 138.7       | 29.6        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 14.3         | 34.6        | 0.5         | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 117.4        | 138.2       | 29.8        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                    | TEST CONDITIONS                                                              | V <sub>CC</sub> | T <sub>A</sub> = –40°C to +85°C |                    |      | T <sub>A</sub> = –40°C to +125°C |                    |     | UNIT |
|------------------|------------------------------------|------------------------------------------------------------------------------|-----------------|---------------------------------|--------------------|------|----------------------------------|--------------------|-----|------|
|                  |                                    |                                                                              |                 | MIN                             | TYP <sup>(1)</sup> | MAX  | MIN                              | TYP <sup>(1)</sup> | MAX |      |
| V <sub>OH</sub>  |                                    | I <sub>OH</sub> = –100 μA                                                    | 1.65 V to 5.5 V | V <sub>CC</sub> – 0.1           |                    |      | V <sub>CC</sub> – 0.1            |                    |     | V    |
|                  |                                    | I <sub>OH</sub> = –4 mA                                                      | 1.65 V          | 1.2                             |                    |      | 1.2                              |                    |     |      |
|                  |                                    | I <sub>OH</sub> = –8 mA                                                      | 1.8 V           | 1.4                             |                    |      |                                  |                    |     |      |
|                  |                                    |                                                                              | 2.3 V           | 1.9                             |                    |      | 1.9                              |                    |     |      |
|                  |                                    | I <sub>OH</sub> = –16 mA                                                     | 3 V             | 2.4                             |                    |      | 2.4                              |                    |     |      |
|                  |                                    | I <sub>OH</sub> = –24 mA                                                     |                 | 2.3                             |                    |      | 2.3                              |                    |     |      |
|                  | I <sub>OH</sub> = –32 mA           | 4.5 V                                                                        | 3.8             |                                 |                    | 3.8  |                                  |                    |     |      |
| V <sub>OL</sub>  |                                    | I <sub>OL</sub> = 100 μA                                                     | 1.65 V to 5.5 V |                                 |                    |      | 0.1                              |                    |     | V    |
|                  |                                    | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          |                                 |                    |      | 0.45                             |                    |     |      |
|                  |                                    | I <sub>OL</sub> = 8 mA                                                       | 1.8 V           |                                 |                    |      | 0.45                             |                    |     |      |
|                  |                                    |                                                                              | 2.3 V           |                                 |                    |      | 0.3                              |                    |     |      |
|                  |                                    | I <sub>OL</sub> = 16 mA                                                      | 3 V             |                                 |                    |      | 0.4                              |                    |     |      |
|                  |                                    | I <sub>OL</sub> = 24 mA                                                      |                 |                                 |                    |      | 0.55                             |                    |     |      |
|                  | I <sub>OL</sub> = 32 mA            | 4.5 V                                                                        |                 |                                 |                    | 0.55 |                                  |                    |     |      |
| I <sub>I</sub>   | A or $\overline{\text{OE}}$ inputs | V <sub>I</sub> = 5.5 V or GND                                                | 0 to 5.5 V      |                                 |                    |      | ±5                               |                    |     | μA   |
| I <sub>off</sub> |                                    | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     | 0               |                                 |                    |      | ±10                              |                    |     | μA   |
| I <sub>OZ</sub>  |                                    | V <sub>O</sub> = 0 to 5.5 V                                                  | 3.6 V           |                                 |                    |      | 10                               |                    |     | μA   |
| I <sub>CC</sub>  |                                    | V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0                            | 1.65 V to 5.5 V |                                 |                    |      | 10                               |                    |     | μA   |
| ΔI <sub>CC</sub> |                                    | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 5.5 V    |                                 |                    |      | 500                              |                    |     | μA   |
| C <sub>i</sub>   | Data inputs                        | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 3.5                             |                    |      | 3.5                              |                    |     | pF   |
|                  | Control inputs                     |                                                                              |                 | 4                               |                    |      | 4                                |                    |     |      |
| C <sub>O</sub>   |                                    | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 6.5                             |                    |      | 6.5                              |                    |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics: T<sub>A</sub> = –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | T <sub>A</sub> = –40°C to +85°C     |      |                                    |     |                                    |     |                                  |     | UNIT |
|------------------|------------------------|----------------|-------------------------------------|------|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
|                  |                        |                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |      | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 5 V<br>± 0.5 V |     |      |
|                  |                        |                | MIN                                 | MAX  | MIN                                | MAX | MIN                                | MAX | MIN                              | MAX |      |
| t <sub>pd</sub>  | A                      | Y              | 3.3                                 | 9.1  | 1.5                                | 4.8 | 1.4                                | 4.3 | 1                                | 3.7 | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y              | 4                                   | 9.9  | 1.9                                | 5.6 | 1.2                                | 4.7 | 1.2                              | 3.8 | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y              | 1.5                                 | 11.6 | 1                                  | 5.8 | 1.4                                | 4.6 | 1                                | 3.4 | ns   |

## 6.7 Switching Characteristics: T<sub>A</sub> = –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | T <sub>A</sub> = –40°C to +125°C    |      |                                    |     |                                    |     |                                  |     | UNIT |
|------------------|------------------------|----------------|-------------------------------------|------|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
|                  |                        |                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |      | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 5 V<br>± 0.5 V |     |      |
|                  |                        |                | MIN                                 | MAX  | MIN                                | MAX | MIN                                | MAX | MIN                              | MAX |      |
| t <sub>pd</sub>  | A                      | Y              | 3.3                                 | 10.1 | 1.5                                | 5.8 | 1.4                                | 5.3 | 1                                | 4.2 | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y              | 4                                   | 10.9 | 1.9                                | 6.6 | 1.2                                | 5.7 | 1.2                              | 4.3 | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y              | 1.5                                 | 12.6 | 1                                  | 6.8 | 1.4                                | 5.6 | 1                                | 3.9 | ns   |

# SN74LVC2G125

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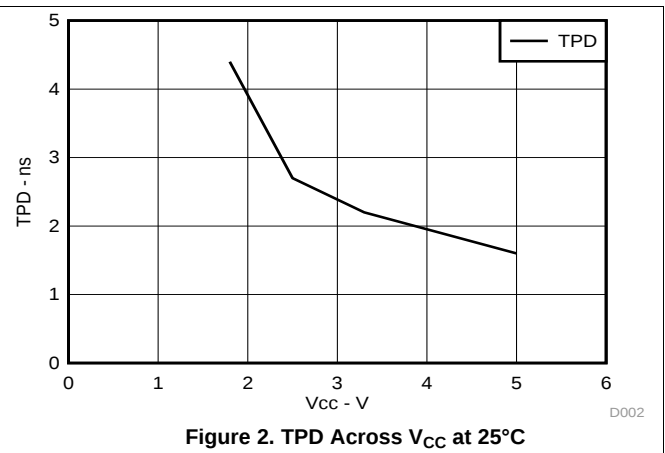
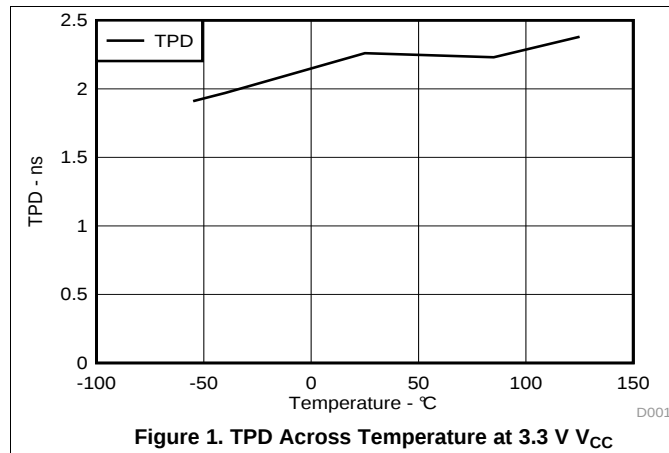
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## 6.8 Operating Characteristics

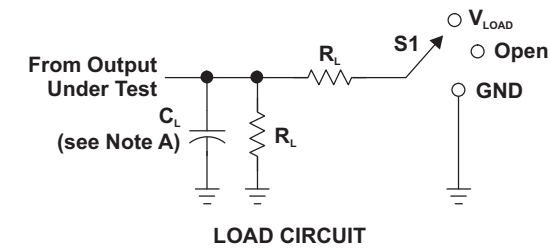
$T_A = 25^\circ$

| PARAMETER |                               | TEST CONDITIONS  | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|-----------|-------------------------------|------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|           |                               |                  | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled  | 19                      | 19                      | 20                      | 22                    | pF   |
|           |                               | Outputs disabled | 2                       | 2                       | 2                       | 3                     |      |

## 6.9 Typical Characteristics

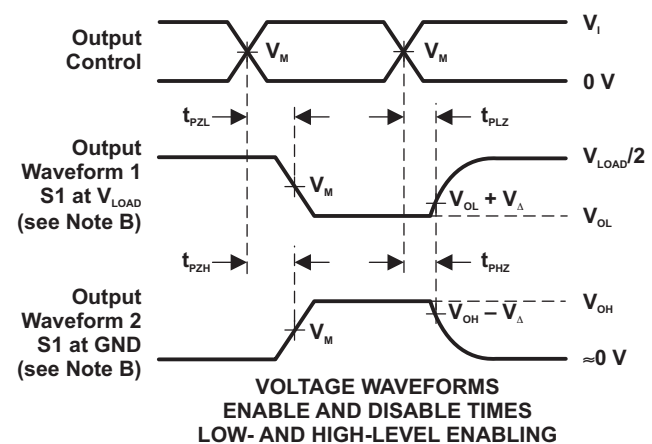
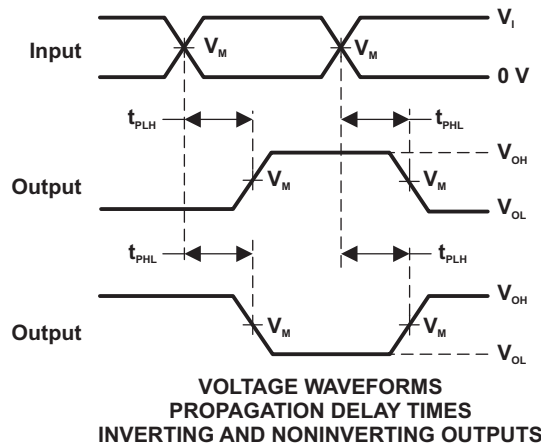
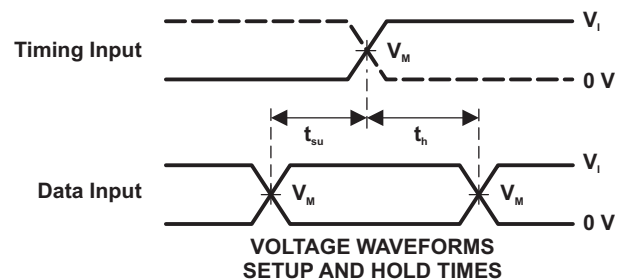
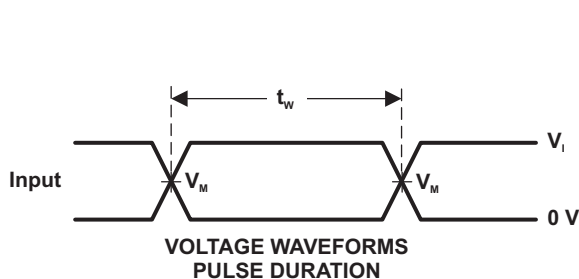


## 7 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_f/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

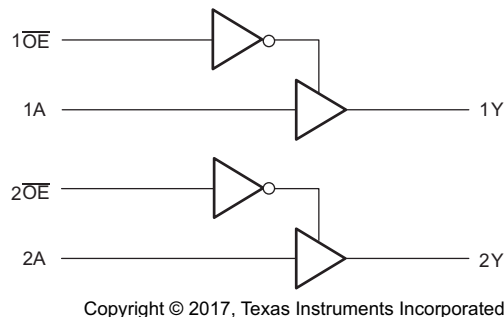
**Figure 3. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74LVC2G125 device contains dual buffer gate device with output enable control and performs the Boolean function  $Y = A$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in [Recommended Operating Conditions](#) to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

#### 8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

#### CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## Feature Description (continued)

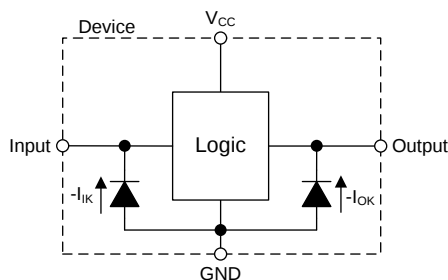


Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.3.4 Partial Power Down ( $I_{off}$ )

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by  $I_{off}$  in the [Electrical Characteristics](#).

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G125.

Table 1. Function Table

| INPUTS          |   | OUTPUT<br>Y |
|-----------------|---|-------------|
| $\overline{OE}$ | A |             |
| L               | H | H           |
| L               | L | L           |
| H               | X | Z           |

## 9 Application and Implementation

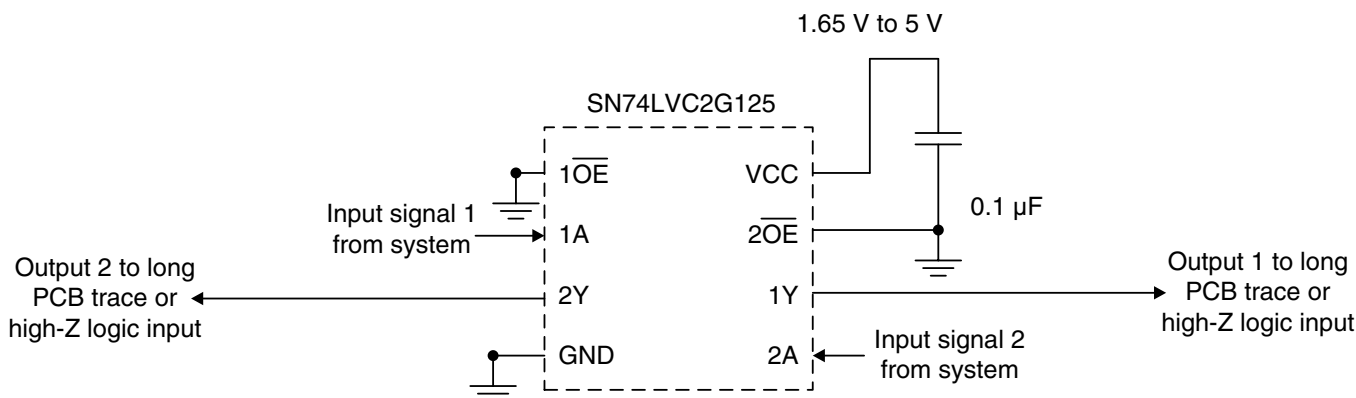
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC2G125 device is a high drive CMOS device that can be used as a output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to  $V_{CC}$ .

### 9.2 Typical Application



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**Figure 5. Typical Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions:

- For rise time and fall time specifications, see ( $\Delta t/\Delta V$ ) in the [Recommended Operating Conditions](#) table.
- For specified high and low levels, see ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

##### 2. Recommended Output Conditions:

- Load currents should not exceed ( $I_O$  max) per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curve

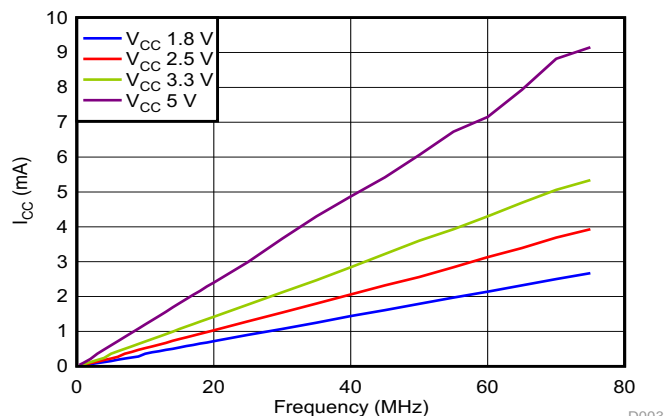


Figure 6. I<sub>CC</sub> vs Frequency

## 10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple V<sub>CC</sub> pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

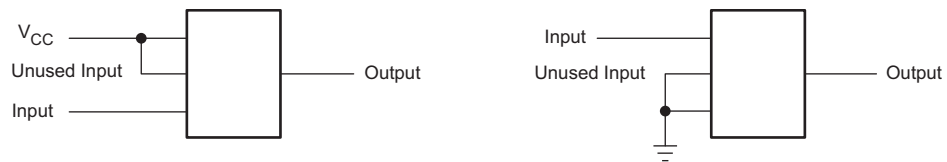
### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

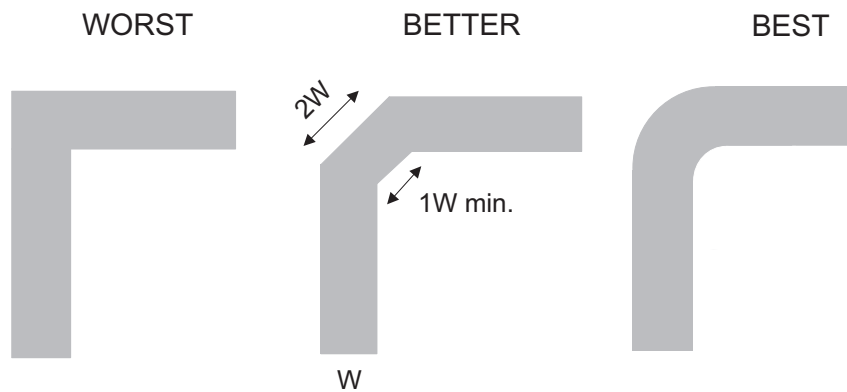
Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example



**Figure 7. Proper multi-gate input termination diagram**



**Figure 8. Trace Example**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1)    | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)              |
|----------------------------------|------------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------|
| 74LVC2G125DCTRE4                 | Active           | Production           | SSOP (DCT)   8  | 3000   null           | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25<br>(R, Z)                    |
| 74LVC2G125DCTRE4.B               | Active           | Production           | SSOP (DCT)   8  | 3000   null           | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25<br>(R, Z)                    |
| <a href="#">74LVC2G125DCTRE6</a> | Last<br>Time Buy | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | C25<br>Z                         |
| 74LVC2G125DCTRE6.B               | Last<br>Time Buy | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | C25<br>Z                         |
| <a href="#">74LVC2G125DCTRG4</a> | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25<br>(R, Z)                    |
| 74LVC2G125DCTRG4.B               | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25<br>(R, Z)                    |
| 74LVC2G125DCURE4                 | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25R                             |
| <a href="#">74LVC2G125DCURG4</a> | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25R                             |
| 74LVC2G125DCURG4.B               | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25R                             |
| <a href="#">74LVC2G125DCUTG4</a> | Active           | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25R                             |
| 74LVC2G125DCUTG4.B               | Active           | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C25R                             |
| <a href="#">SN74LVC2G125DCT3</a> | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | C25<br>Z                         |
| SN74LVC2G125DCT3.B               | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | C25<br>Z                         |
| <a href="#">SN74LVC2G125DCTR</a> | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | (2WK5, C25)<br>(R, Z)            |
| SN74LVC2G125DCTR.B               | Active           | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | (2WK5, C25)<br>(R, Z)            |
| <a href="#">SN74LVC2G125DCU3</a> | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | 25<br>CZ                         |
| SN74LVC2G125DCU3.B               | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 125   | 25<br>CZ                         |
| <a href="#">SN74LVC2G125DCUR</a> | Active           | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | (25, C25J, C25Q, C<br>25R)<br>CZ |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)          |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------|
| SN74LVC2G125DCUR.B               | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (25, C25J, C25Q, C25R)<br>CZ |
| <a href="#">SN74LVC2G125DCUT</a> | Active        | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | (C25J, C25Q, C25R)           |
| SN74LVC2G125DCUT.B               | Active        | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (C25J, C25Q, C25R)           |
| <a href="#">SN74LVC2G125YZPR</a> | Active        | Production           | DSBGA (YZP)   8 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | (CM7, CMN)                   |
| SN74LVC2G125YZPR.B               | Active        | Production           | DSBGA (YZP)   8 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | (CM7, CMN)                   |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LVC2G125 :**

- Automotive : [SN74LVC2G125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVC2G125DCTRE6 | SSOP         | DCT             | 8    | 3000 | 180.0              | 13.0               | 3.35    | 4.5     | 1.55    | 4.0     | 12.0   | Q3            |
| 74LVC2G125DCTRG4 | SSOP         | DCT             | 8    | 3000 | 177.8              | 12.4               | 3.45    | 4.4     | 1.45    | 4.0     | 12.0   | Q3            |
| 74LVC2G125DCURG4 | VSSOP        | DCU             | 8    | 3000 | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| 74LVC2G125DCUTG4 | VSSOP        | DCU             | 8    | 250  | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G125DCT3 | SSOP         | DCT             | 8    | 3000 | 180.0              | 13.0               | 3.35    | 4.5     | 1.55    | 4.0     | 12.0   | Q3            |
| SN74LVC2G125DCTR | SSOP         | DCT             | 8    | 3000 | 180.0              | 12.4               | 3.15    | 4.35    | 1.55    | 4.0     | 12.0   | Q3            |
| SN74LVC2G125DCUR | VSSOP        | DCU             | 8    | 3000 | 178.0              | 9.0                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G125DCUT | VSSOP        | DCU             | 8    | 250  | 178.0              | 9.0                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G125YZPR | DSBGA        | YZP             | 8    | 3000 | 178.0              | 9.2                | 1.02    | 2.02    | 0.63    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVC2G125DCTRE6 | SSOP         | DCT             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| 74LVC2G125DCTRG4 | SSOP         | DCT             | 8    | 3000 | 183.0       | 183.0      | 20.0        |
| 74LVC2G125DCURG4 | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| 74LVC2G125DCUTG4 | VSSOP        | DCU             | 8    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC2G125DCT3 | SSOP         | DCT             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| SN74LVC2G125DCTR | SSOP         | DCT             | 8    | 3000 | 190.0       | 190.0      | 30.0        |
| SN74LVC2G125DCUR | VSSOP        | DCU             | 8    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC2G125DCUT | VSSOP        | DCU             | 8    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC2G125YZPR | DSBGA        | YZP             | 8    | 3000 | 220.0       | 220.0      | 35.0        |



## VSSOP - 0.9 mm max height

## SMALL OUTLINE PACKAGE



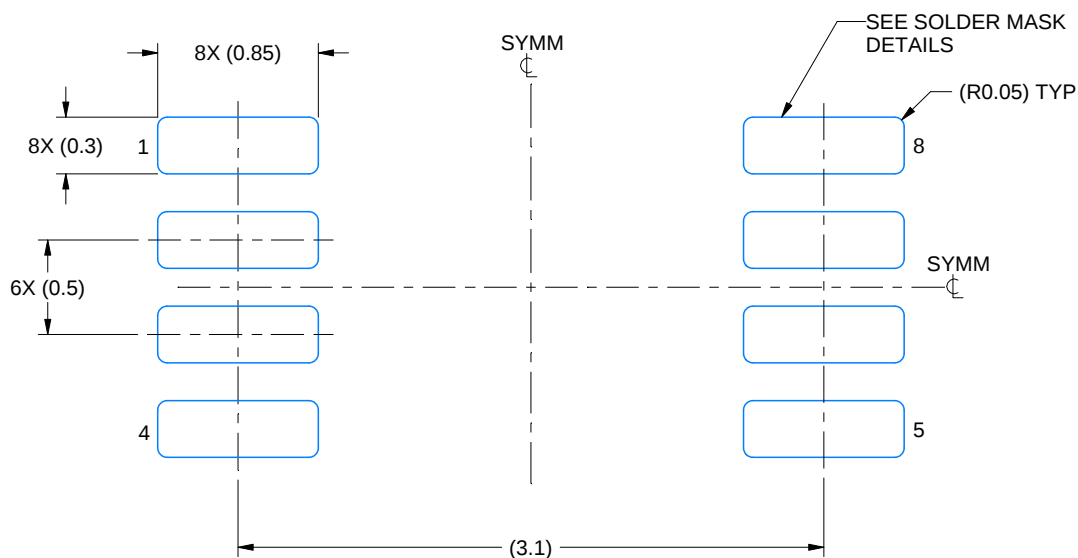
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

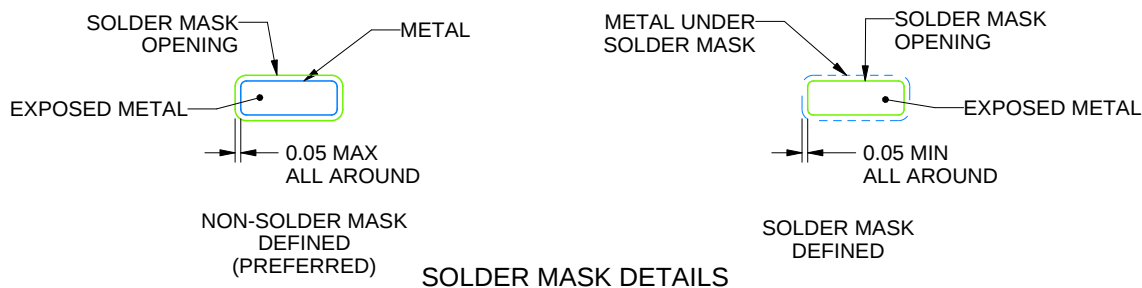
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

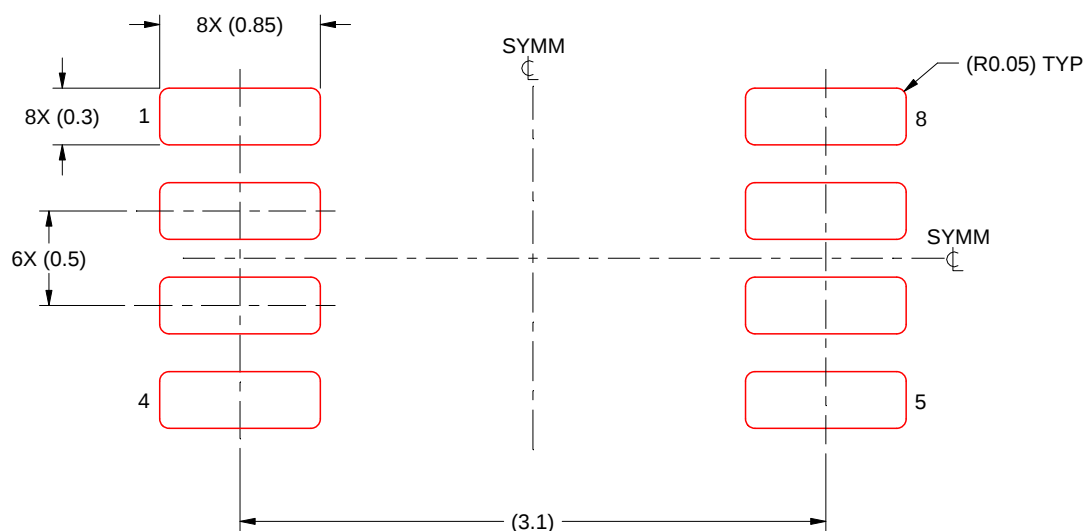
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

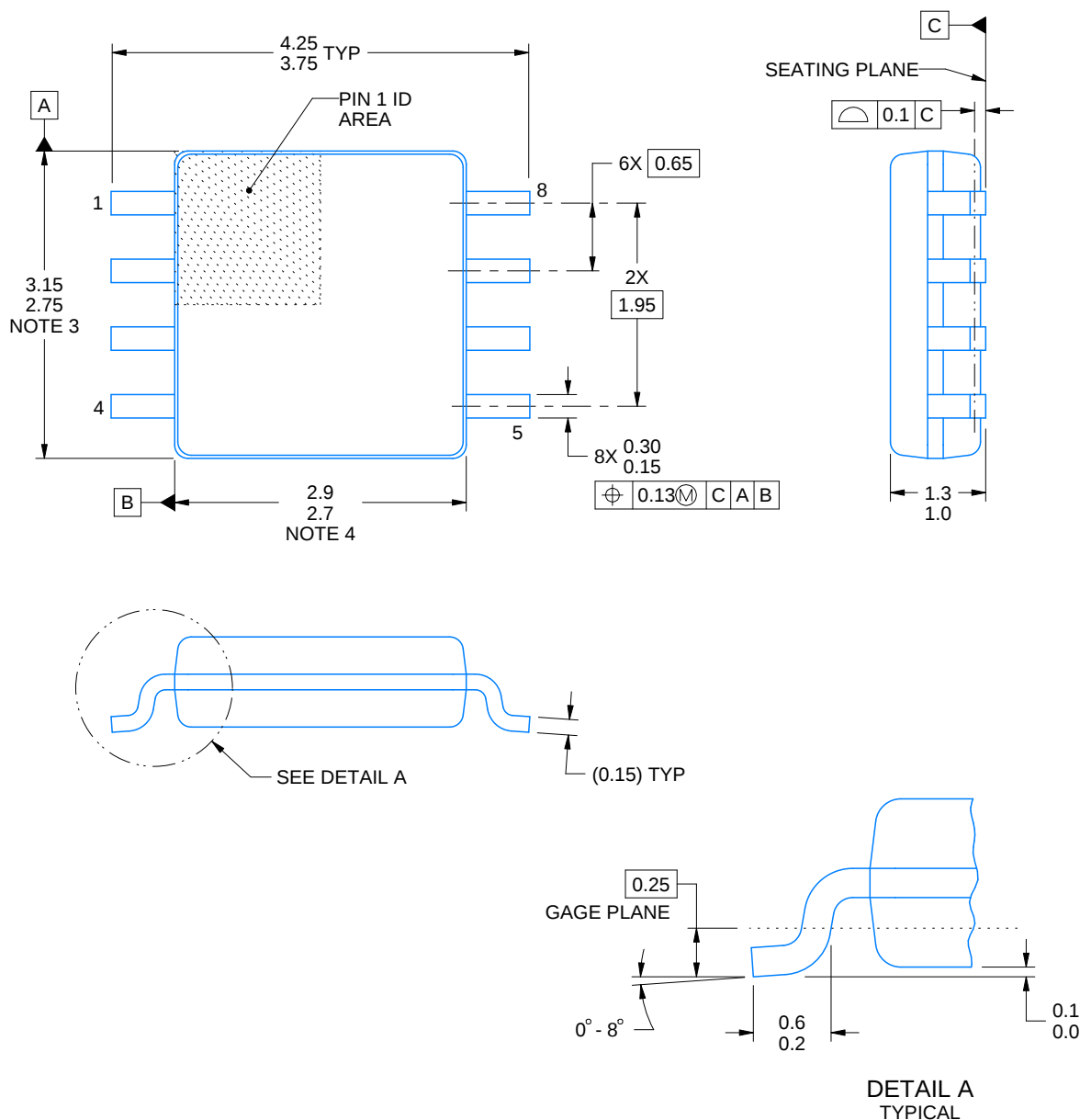
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## PACKAGE OUTLINE

## SSOP - 1.3 mm max height

## SMALL OUTLINE PACKAGE



4220784/C 06/2021

NOTES:

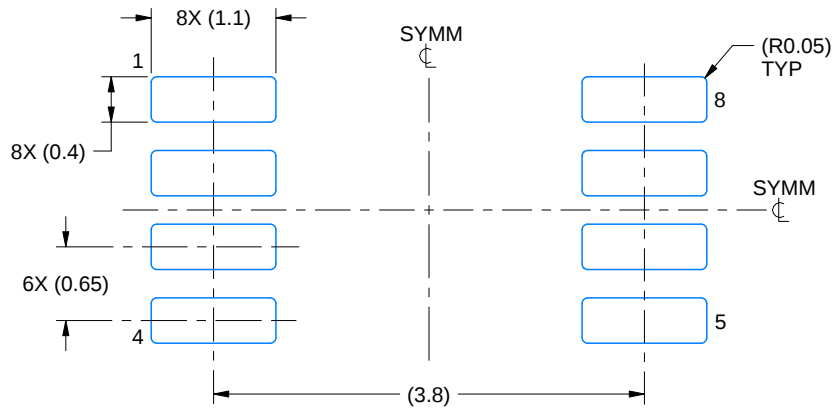
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

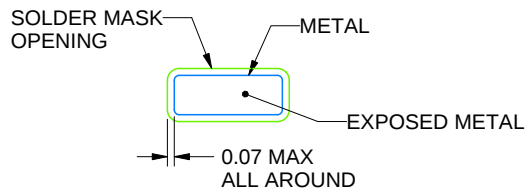
DCT0008A

SSOP - 1.3 mm max height

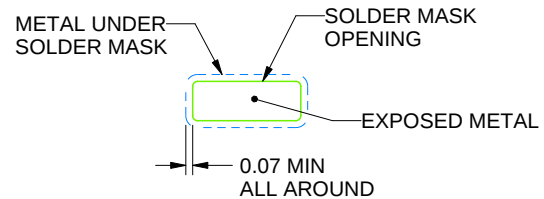
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

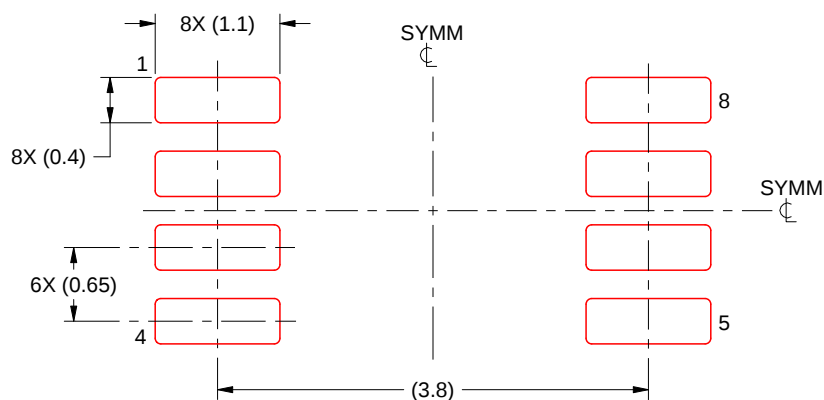
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



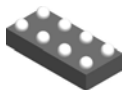
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

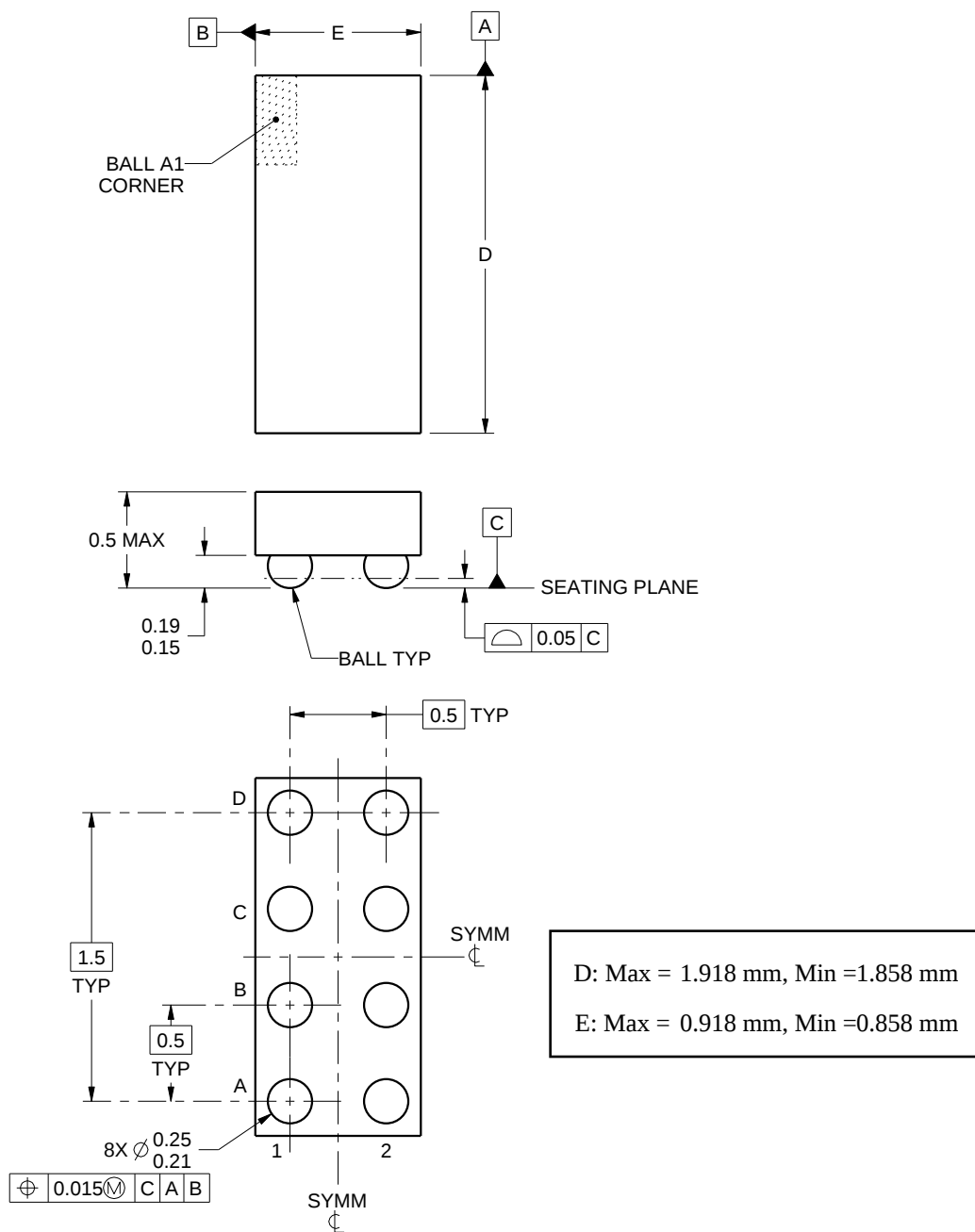
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

## NOTES:

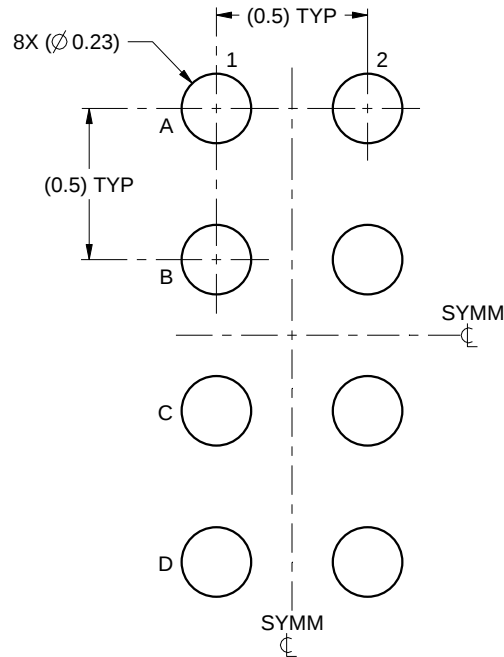
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

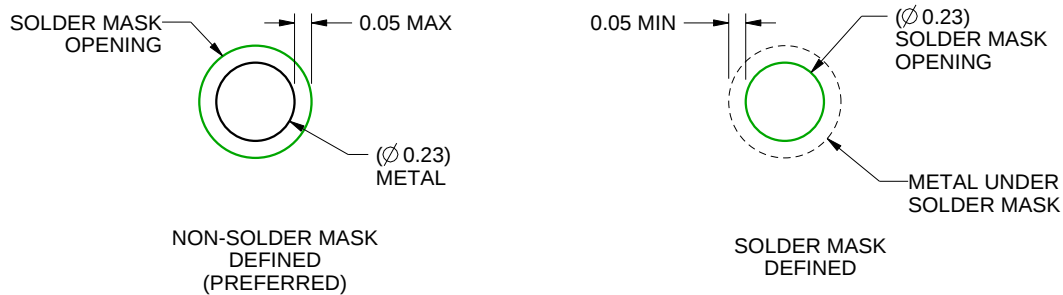
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

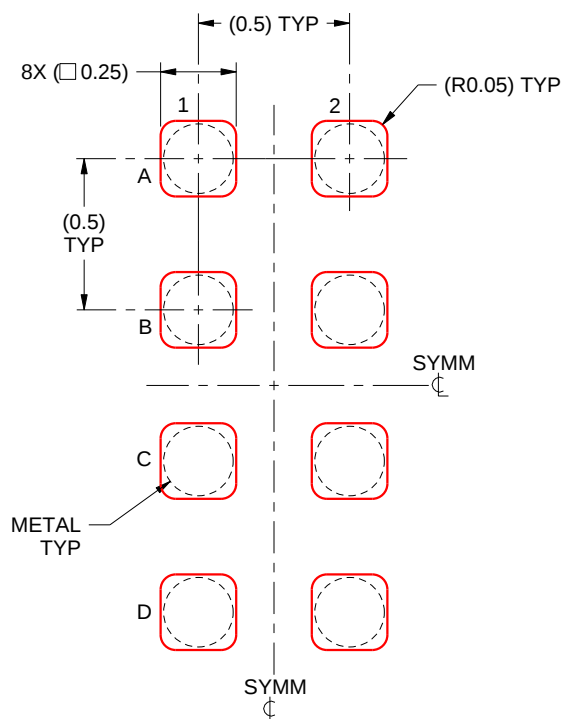
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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