



SN74LVC138A 3-Line to 8-Line Decoders Demultiplexers

1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- LED Displays
- Servers
- White Goods
- Power Infrastructure
- Building Automation
- Factory Automation

3 Description

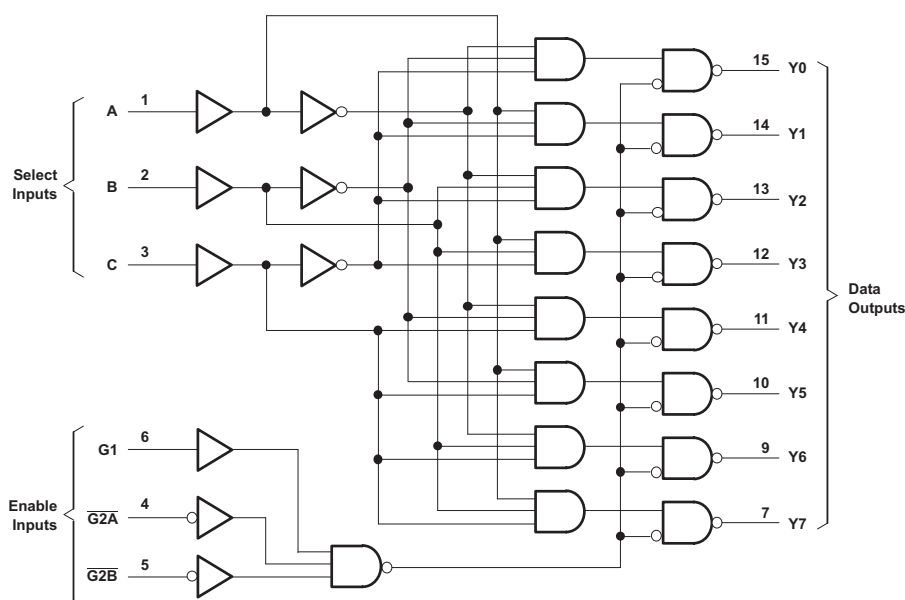
The SN74LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories using a fast enable circuit, delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LVC138A	LCCC (20)	8.89 mm × 8.89 mm
	CDIP (16)	19.56 mm × 6.92 mm
	CFP (16)	10.30 mm × 6.73 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SSOP (16)	6.20 mm × 5.30 mm
	TVSOP (16)	3.60 mm × 4.40 mm
	BGA MICROSTAR JUNIOR (20)	4.00 mm × 3.00 mm
	TSSOP (16)	5.00 mm × 4.40 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

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4 Revision History

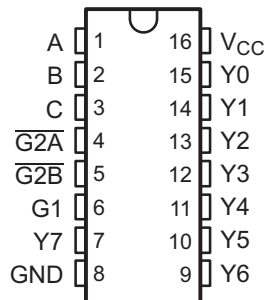
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision V (November 2013) to Revision W	Page
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Deleted Ordering Information table; see Packaging Ordering Addendum at the end of the data sheet	1
• Changed R _{0JA} values from: 73 to 86.8 (D), 82 to 100.1 (DB), 120 to 122.1 (DGV), 78 to 84 (ZQN), 108 to 108.9 (PW)	6
• Deleted R _{0JA} values for NS and RGY packages	6

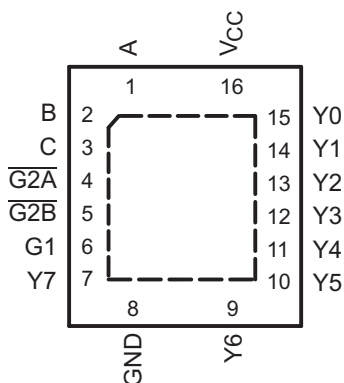
Changes from Revision U (OCTOBER 2012) to Revision V	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Removed Ordering Information table	1
• Added ESD warning	1

5 Pin Configuration and Functions

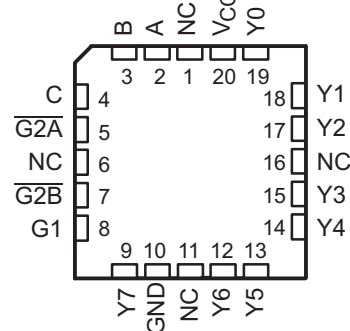
SN54LVC138A . . . J OR W PACKAGE
SN74LVC138A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC138A . . . RGY PACKAGE
(TOP VIEW)

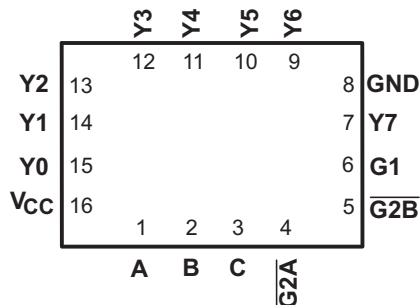


SN54LVC138A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

SN54LVC138A . . . RSV PACKAGE
(TOP VIEW)



GQN OR ZQN PACKAGE
(TOP VIEW)

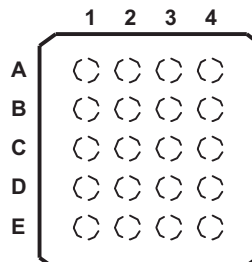


Table 1. Pin Assignments for ZQN (BGA)

	1	2	3	4
A	B	A	V _{CC}	Y0
B	C	NC ⁽¹⁾	NC ⁽¹⁾	Y1
C	G2B	G2A	Y3	Y2
D	G1	NC ⁽¹⁾	NC ⁽¹⁾	Y4
E	GND	Y7	Y6	Y5

(1) NC - No internal connection

SN54LVC138A, SN74LVC138A

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Pin Functions

NAME	PIN				DESCRIPTION
	SOIC, SSOP, TVSOP, SO, TSSOP, VQFN, UQFN	LCCC	BGA MICROSTAR JUNIOR	I/O	
A	1	2	A2	I	Select input A (least significant bit)
B	2	3	A1	I	Select input B
C	3	4	B1	I	Select input C (most significant bit)
$\overline{G}2A$	4	5	C2	I	Active low enable A
$\overline{G}2B$	5	7	C1	I	Active low enable B
G1	6	8	D1	I	Active high enable
GND	8	10	E1	—	Ground
NC	—	1, 11, 16	B2, B3, D2, D3	—	No internal connection
V _{CC}	16	20	A3	—	Supply voltage
Y0	15	19	A4	O	Output 0 (least significant bit)
Y1	14	18	B4	O	Output 1
Y2	13	17	C4	O	Output 2
Y3	12	15	C3	O	Output 3
Y4	11	14	D4	O	Output 4
Y5	10	13	E4	O	Output 5
Y6	9	12	E3	O	Output 6
Y7	7	9	E2	O	Output 7 (most significant bit)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage ⁽²⁾		–0.5	6.5	V
V_O	Output voltage ⁽²⁾⁽³⁾		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000	
	Machine model (MM)	200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

SN54LVC138A, SN74LVC138A

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6.3 Recommended Operating Conditions

			MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	SN54LVC138A ⁽¹⁾	2	3.6	V
			SN74LVC138A ⁽¹⁾	1.65	3.6	
		Data retention only		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	SN74LVC138A ⁽¹⁾	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	SN74LVC138A ⁽¹⁾	1.7		
		V _{CC} = 2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	SN74LVC138A ⁽¹⁾	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	SN74LVC138A ⁽¹⁾	0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8		
V _I	Input voltage			0	5.5	V
V _O	Output voltage			0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	SN74LVC138A ⁽¹⁾	−4		mA
		V _{CC} = 2.3 V	SN74LVC138A ⁽¹⁾	−8		
		V _{CC} = 2.7 V		−12		
		V _{CC} = 3 V		−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	SN74LVC138A ⁽¹⁾	4		mA
		V _{CC} = 2.3 V	SN74LVC138A ⁽¹⁾	8		
		V _{CC} = 2.7 V		12		
		V _{CC} = 3 V		24		
Δt/Δv	Input transition rise or fall rate			10		ns/V
T _A	Operating free-air temperature	SN54LVC138A ⁽¹⁾		−55	125	°C
		SN74LVC138A ⁽¹⁾		−40	85	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4LVC138A									UNIT
		FK (LCCC)	J (CDIP)	W (CFP)	D (SOIC)	DB (SSOP)	DGV (TVSOP)	ZQN (BGA MICROSTAR JUNIOR)	PW (TSSOP)	RSV (UQFN)	
		20 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	20 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	79.2	85.8	138.0	86.8	100.1	122.1	84	108.9	168.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.5	49.3	74.6	47.9	50.6	47.4	56.9	42.5	78.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.2	64.9	127.7	43.8	50.7	53.8	46.1	54.5	96.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	49.8	37.4	50	15.7	14.3	4.6	3	4.4	4.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55.0	69.5	115.7	43.5	50.1	53.2	48.9	53.8	96.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –100 µA	SN74LVC138A	1.65 V to 3.6 V	V _{CC} – 0.2		V
			SN54LVC138A	2.7 V to 3.6 V	V _{CC} – 0.2		
	I _{OH} = –4 mA		SN74LVC138A	1.65 V	1.2		
		I _{OH} = –8 mA	SN74LVC138A	2.3 V	1.7		
				2.7 V	2.2		
				3 V	2.4		
V _{OL}	Low-level output voltage	I _{OL} = 100 µA	SN74LVC138A	1.65 V to 3.6 V		0.2	V
			SN54LVC138A	2.7 V to 3.6 V		0.2	
	I _{OL} = 4 mA		SN74LVC138A	1.65 V		0.45	
		I _{OL} = 8 mA	SN74LVC138A	2.3 V		0.7	
				2.7 V		0.4	
				3 V		0.55	
I _I	Input current	V _I = 5.5 V or GND		3.6 V		±5	µA
I _{CC}	Supply current	V _I = V _{CC} or GND, I _O = 0		3.6 V		10	µA
ΔI _{CC}	Change in supply current	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V		500	µA
C _i	Input capacitance	V _I = V _{CC} or GND		3.3 V		5	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics—SN54LVC138A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{pd} Propagation (delay) time	A or B or C	Y	V _{CC} = 2.7 V		7.9	ns
			V _{CC} = 3.3 V ± 0.3 V	1	6.7	
	$\overline{G2A}$ or $\overline{G2B}$		V _{CC} = 2.7 V		7.4	
			V _{CC} = 3.3 V ± 0.3 V	1	6.5	
	G1		V _{CC} = 2.7 V		6.4	
			V _{CC} = 3.3 V ± 0.3 V	1	5.8	

6.7 Switching Characteristics—SN74LVC138A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{pd} Propagation (delay) time	A or B or C	Y	V _{CC} = 1.8 V ± 0.15 V	1	22	ns
			V _{CC} = 2.5 V ± 0.2 V	1	9.9	
			V _{CC} = 2.7 V	1	7.9	
			V _{CC} = 3.3 V ± 0.3 V	1	6.7	
	$\overline{G2A}$ or $\overline{G2B}$		V _{CC} = 1.8 V ± 0.15 V	1	21	
			V _{CC} = 2.5 V ± 0.2 V	1	9.4	
			V _{CC} = 2.7 V	1	7.4	
			V _{CC} = 3.3 V ± 0.3 V	1	6.5	
	G1		V _{CC} = 1.8 V ± 0.15 V	1	20.3	
			V _{CC} = 2.5 V ± 0.2 V	1	8.4	
			V _{CC} = 2.7 V	1	6.4	
			V _{CC} = 3.3 V ± 0.3 V	1	5.8	
t _{sk(o)} Skew (time), output	—	—	V _{CC} = 3.3 V ± 0.3 V		1	ns

6.8 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	25
			$V_{CC} = 2.5\text{ V}$	26
			$V_{CC} = 3.3\text{ V}$	27

6.9 Typical Characteristics

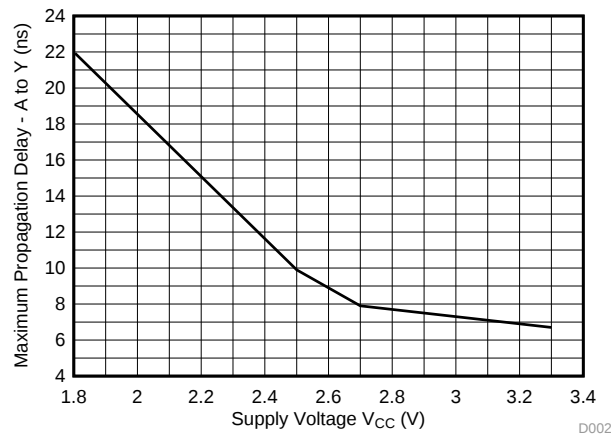
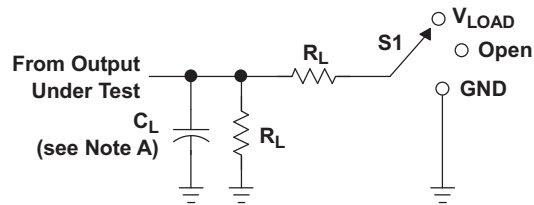


Figure 1. Maximum Propagation Delay vs Supply Voltage

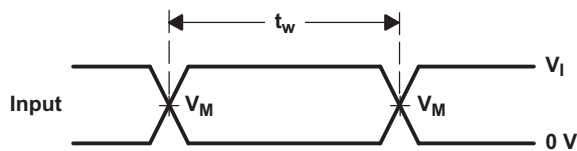
7 Parameter Measurement Information



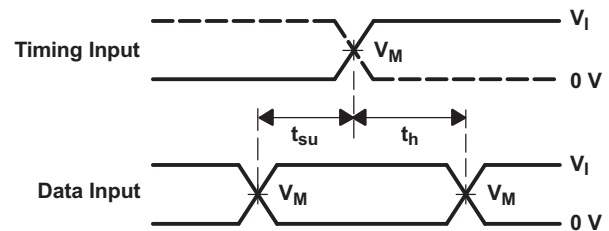
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

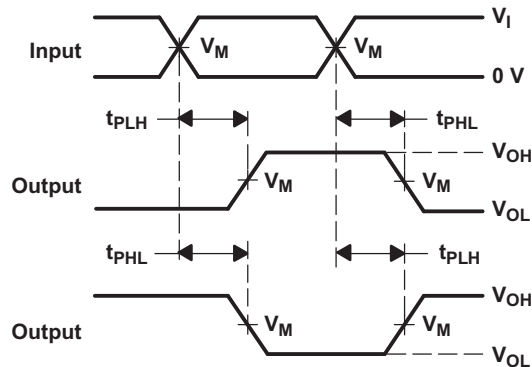
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V



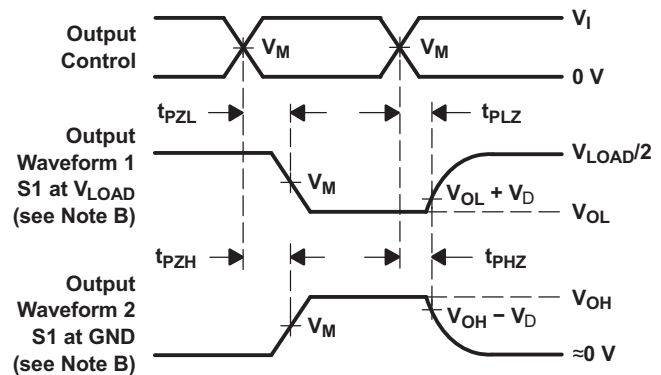
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

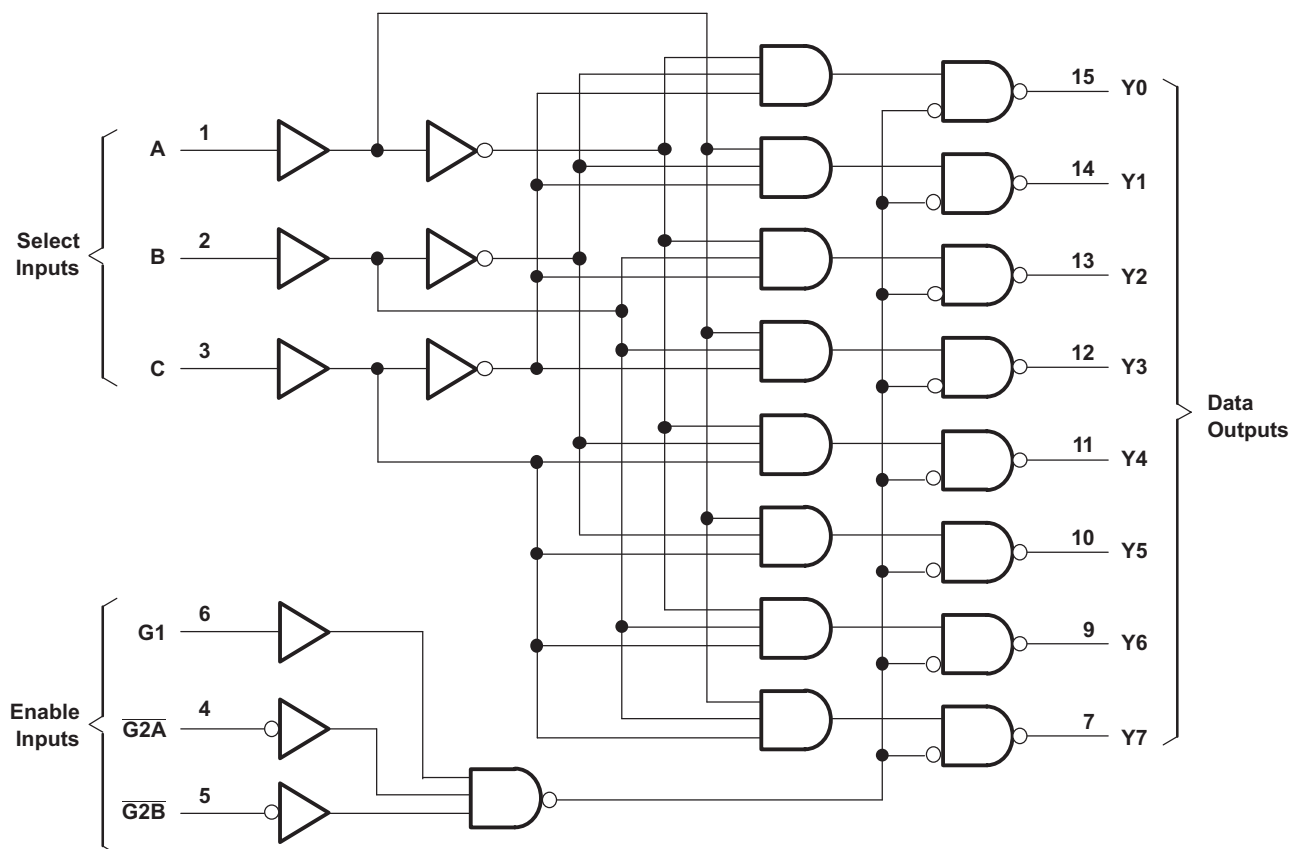
8 Detailed Description

8.1 Overview

The SNx4LVC138A devices are 3-to-8 decoders and demultiplexers. The three input pins, A, B, and C, select which output is active. The selected output is pulled LOW, while the remaining outputs are all HIGH. The conditions at the binary-select inputs at the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the requirement for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

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8.3 Feature Description

8.3.1 3-Line to 8-Line Decoder

This device features three binary inputs to select a single active-low output. Three enable pins are also available to enable or disable the outputs. One active high enable and two active low enable pins are available, and any enable pin can be deactivated to force all outputs high. All three enable pins must be active for the output to be enabled.

Feature Description (continued)

8.3.2 1.65-V to 3.6-V Operation With Inputs up to 5.5 V

The SN54LVC138A 3-line to 8-line decoder demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC138A 3-line to 8-line decoder demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment.

8.4 Device Functional Modes

Table 2 lists the outputs of the SNx4LVC138A devices based on the possible input configurations.

Table 2. Function Table

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

9 Application and Implementation

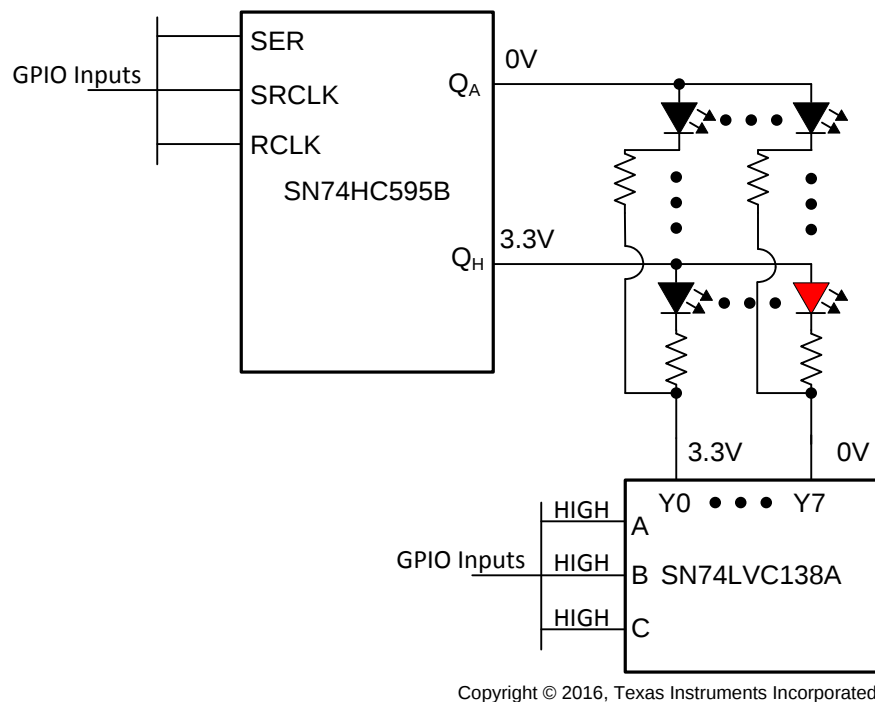
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC138A is useful as a scanning column selector for an LED Matrix display as it can be used for the low-side drive of the LED string. The decoder functionality ensures that no more than one output is pulled to a low-level logic voltage so that only a single column is enabled at any point in time.

9.2 Typical Application



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Figure 3. LED Matrix Driver Application

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For switch time specifications, see propagation delay times in [Switching Characteristics—SN74LVC138A](#).
 - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
2. Recommended Output Conditions
 - Outputs must not be pulled above V_{CC} or below GND.

Typical Application (continued)

9.2.3 Application Curve

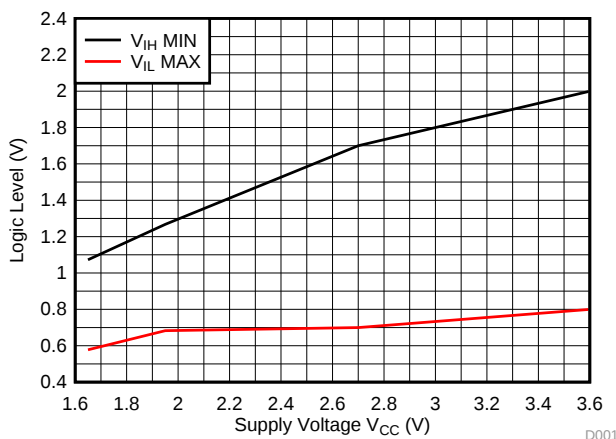


Figure 4. Input High and Input Low Thresholds vs Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F bypass capacitor is recommended to be placed close to the V_{CC} terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. [Figure 5](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

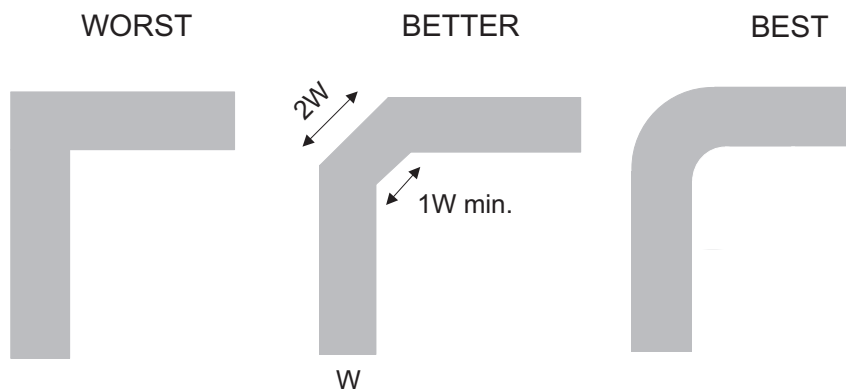


Figure 5. Trace Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC138A	Click here	Click here	Click here	Click here	Click here
SN74LVC138A	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9752601Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9752601Q2A SNJ54LVC 138AFK
5962-9752601QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601QE A SNJ54LVC138AJ
5962-9752601QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601QF A SNJ54LVC138AW
5962-9752601VFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601VF A SNV54LVC138AW
SN74LVC138AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138AD.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADBR.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADBRG4.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADBRG4.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADE4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADGVR.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADGVRG4	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADGVRG4.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADRE4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC138ADT	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ADT.B	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ANSR.B	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138ANSRG4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC138A
SN74LVC138APW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWG4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWT	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138APWT.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC138A
SN74LVC138ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC138A
SN74LVC138ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC138A
SN74LVC138ARGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC138A
SN74LVC138ARGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC138A
SN74LVC138ARSVR	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTP
SN74LVC138ARSVR.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTP
SN74LVC138ARSVRG4	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTP
SN74LVC138ARSVRG4.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTP
SNJ54LVC138AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601Q2A SNJ54LVC138AFK
SNJ54LVC138AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601QE A SNJ54LVC138AJ

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LVC138AW	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9752601QF A SNJ54LVC138AW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC138A, SN54LVC138A-SP, SN74LVC138A :

- Catalog : [SN74LVC138A](#), [SN54LVC138A](#)
- Automotive : [SN74LVC138A-Q1](#), [SN74LVC138A-Q1](#)

- Enhanced Product : [SN74LVC138A-EP](#), [SN74LVC138A-EP](#)
- Military : [SN54LVC138A](#)
- Space : [SN54LVC138A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC138ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC138ADBRG4	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC138ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC138ADGVRG4	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC138ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC138ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC138APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC138APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC138APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC138ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC138ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC138ADBRG4	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC138ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LVC138ADGVRG4	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LVC138ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LVC138ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LVC138APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC138APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC138APWT	TSSOP	PW	16	250	353.0	353.0	32.0
SN74LVC138ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

TUBE

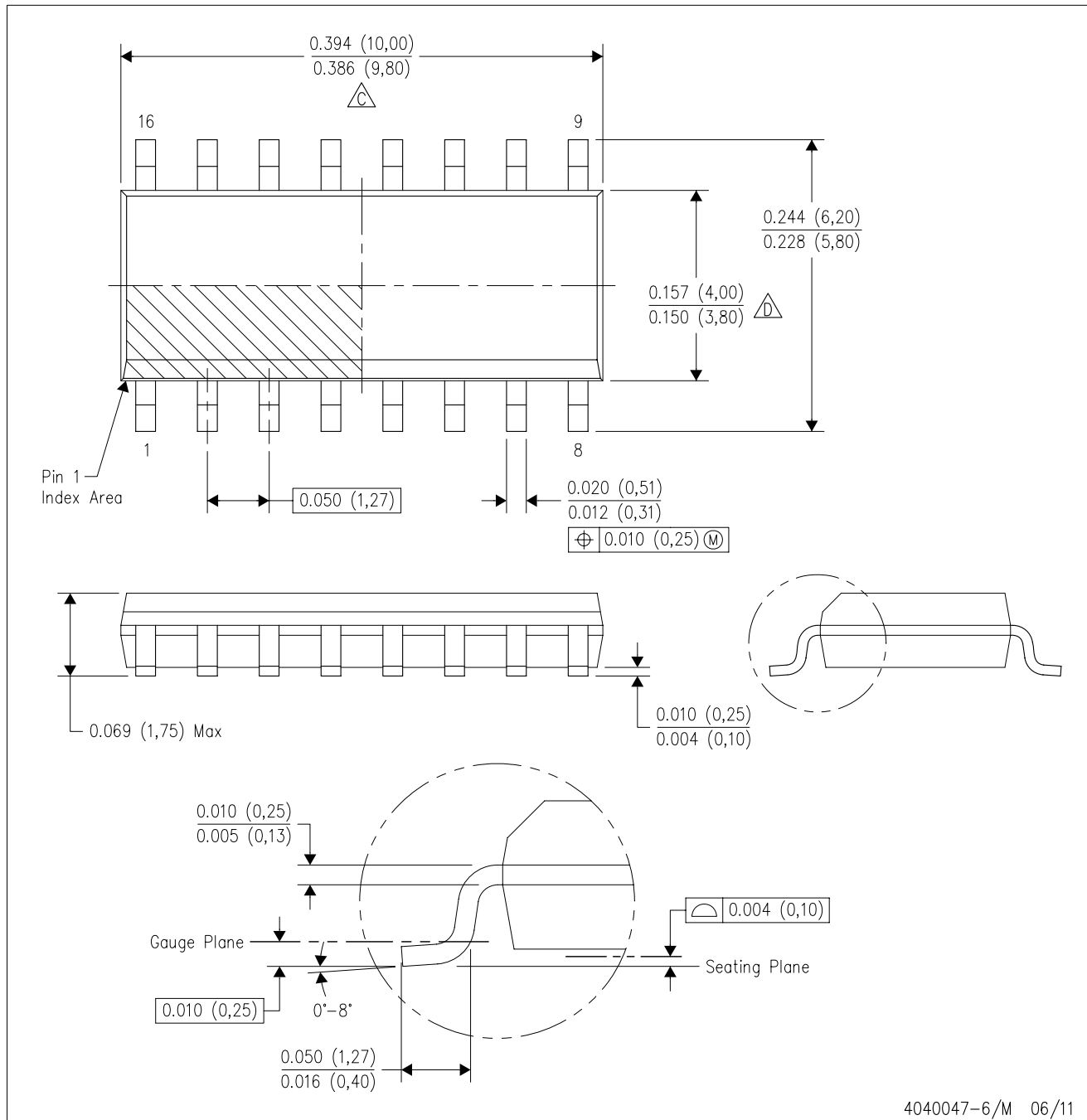


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9752601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9752601QFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-9752601VFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LVC138AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC138AD.B	D	SOIC	16	40	507	8	3940	4.32
SN74LVC138ADE4	D	SOIC	16	40	507	8	3940	4.32
SN74LVC138APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC138APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC138APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54LVC138AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC138AW	W	CFP	16	25	506.98	26.16	6220	NA

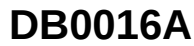
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



SSOP - 2 mm max height

Technical drawing of a 16-pin connector with three views: top, side, and detail A.

Top View:

- Overall width: 8.2 TYP, 7.4
- Overall height: 6.5, 5.9 (NOTE 3)
- Pin 1 Index Area: Circular feature on the left side.
- Pin 16: Located at the top right.
- Pin 8: Located at the bottom left.
- Pin 9: Located at the bottom right.
- Pin 14: Located at the top right, 14X 0.65
- Pin 2: Located at the top right, 2X 4.55
- Pin 16X: Located at the bottom right, 16X 0.38, 0.22
- Pin 5.6/5.0 (NOTE 4): Located at the bottom right.
- Feature A: Located at the top left, 0.1 (M) C A B

Side View:

- Seating Plane: Indicated by a vertical line.
- Feature C: Located at the top left, 0.1 C

Detail A (Typical):

- Feature A: Located at the top left, 0.25
- Feature B: Located at the top right, 0.09
- Feature C: Located at the top right, 0.25
- Feature D: Located at the bottom right, 0.95, 0.55
- Feature E: Located at the bottom right, 2 MAX
- Feature F: Located at the bottom right, 0.05 MIN
- Feature G: Located at the bottom right, 0°-8°
- Gage Plane: Indicated by a horizontal line.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

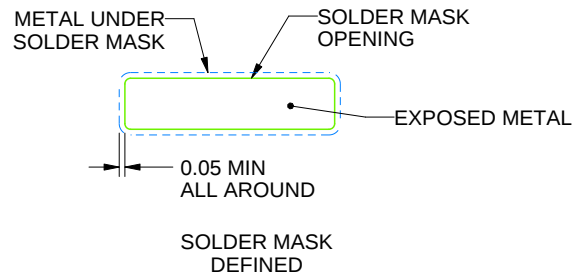
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

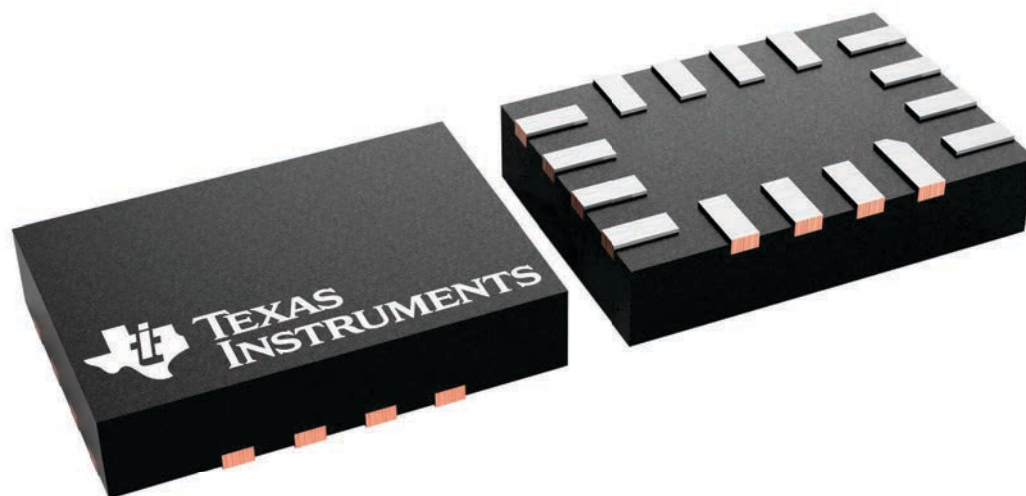
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



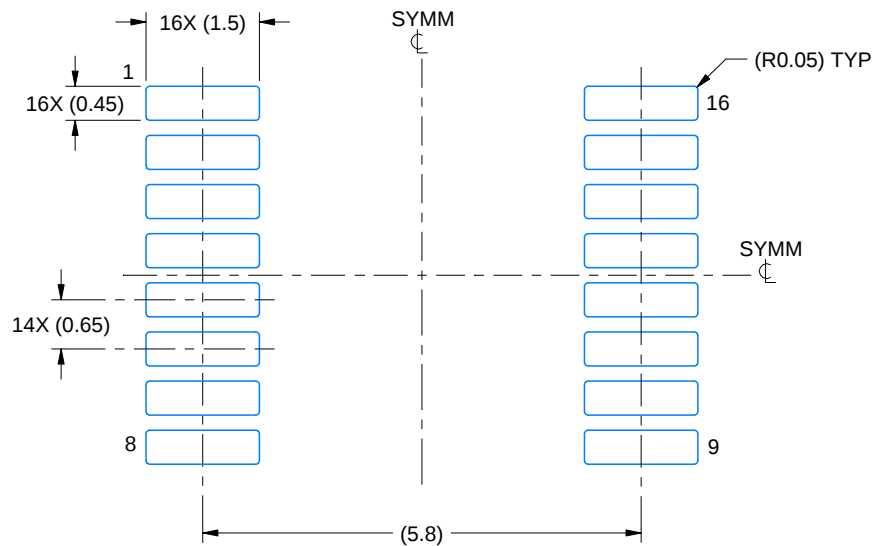
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

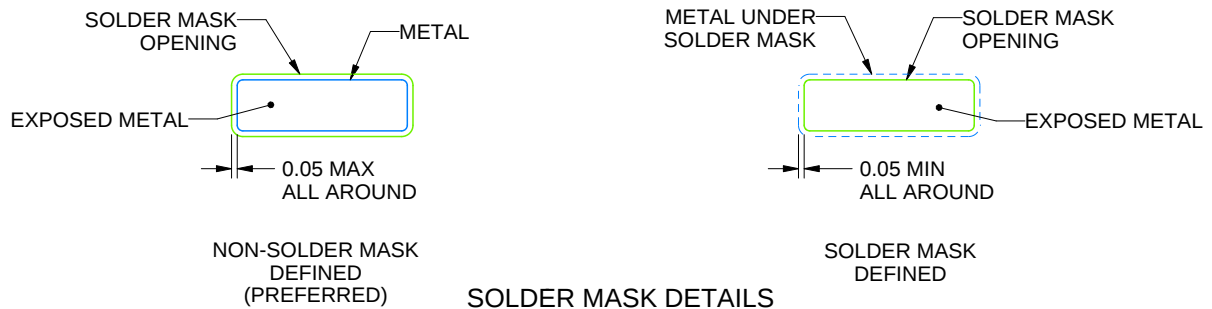
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

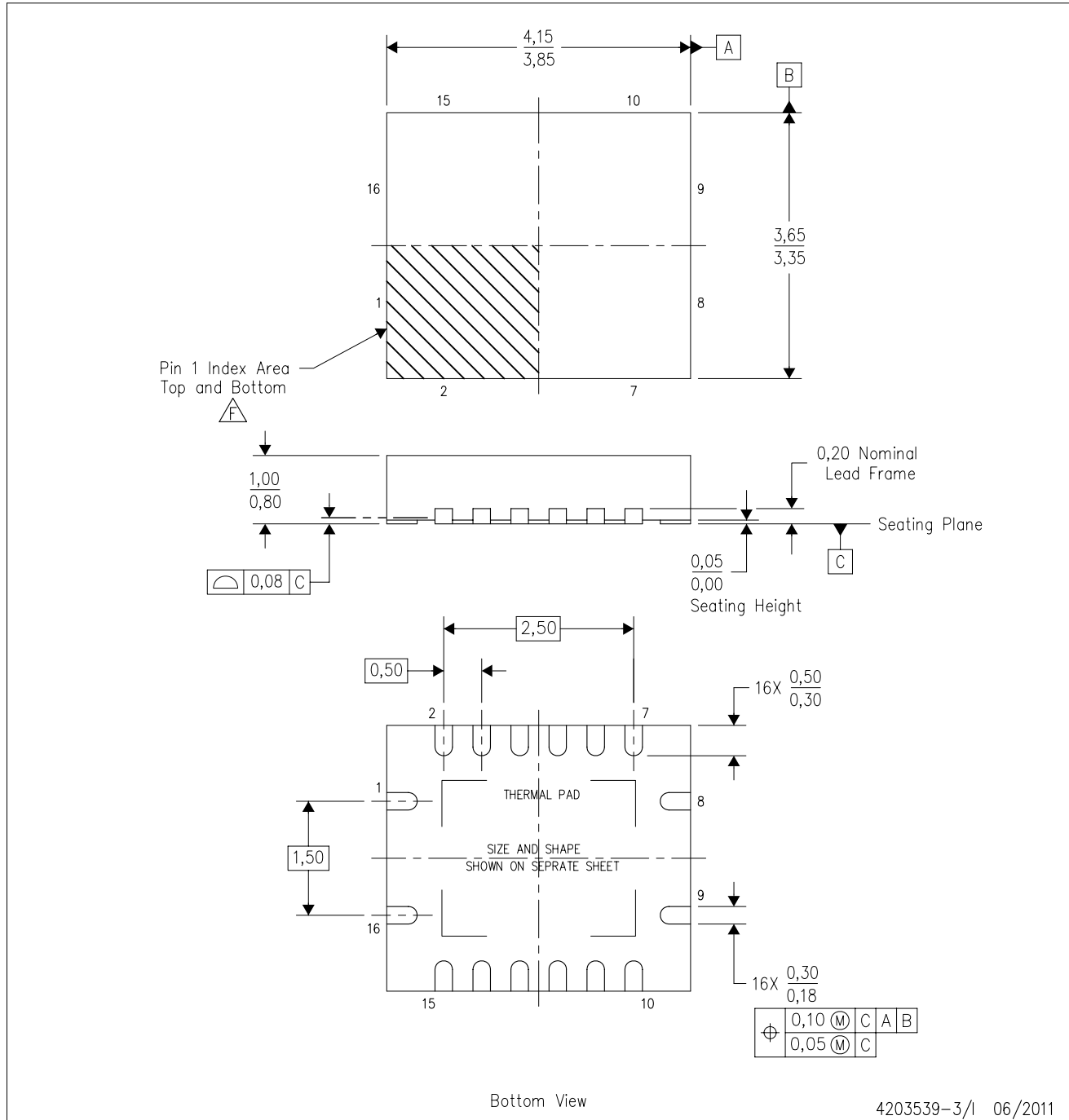
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

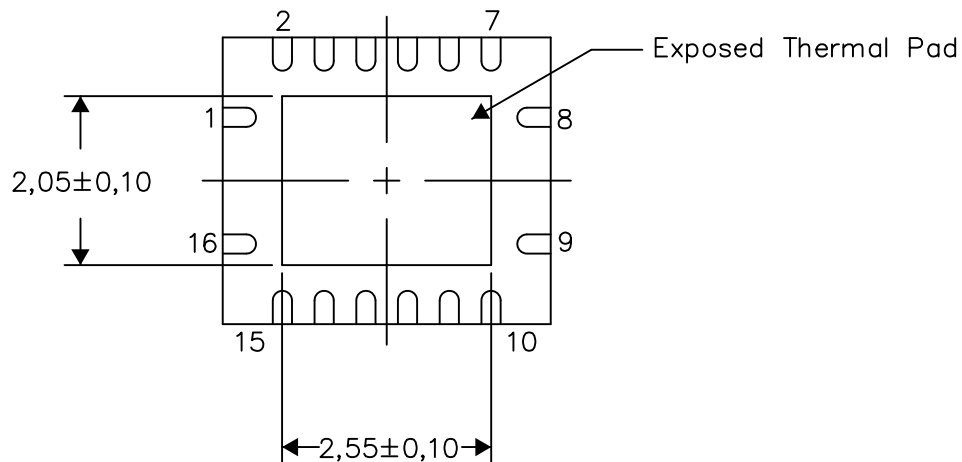
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

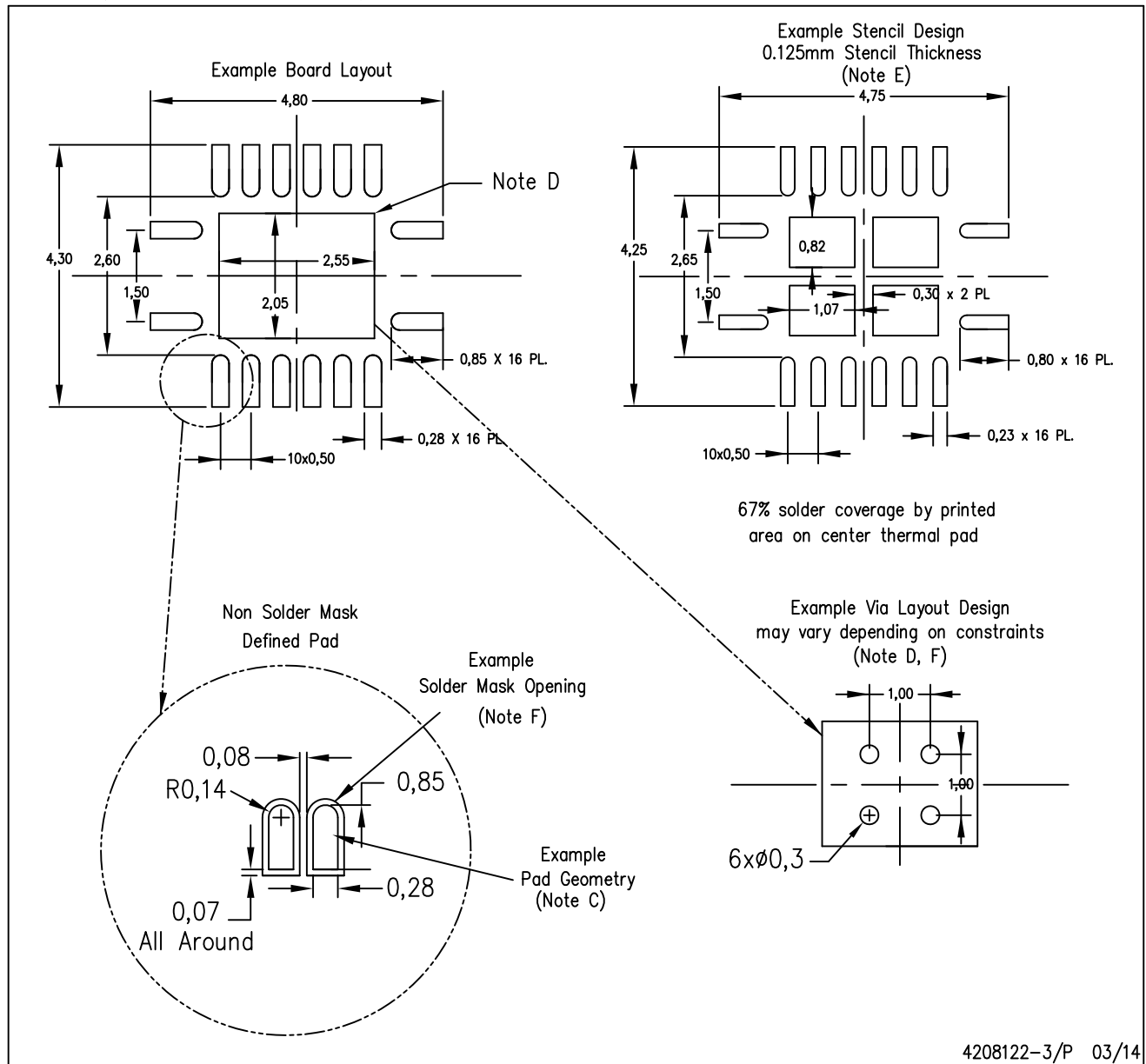
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

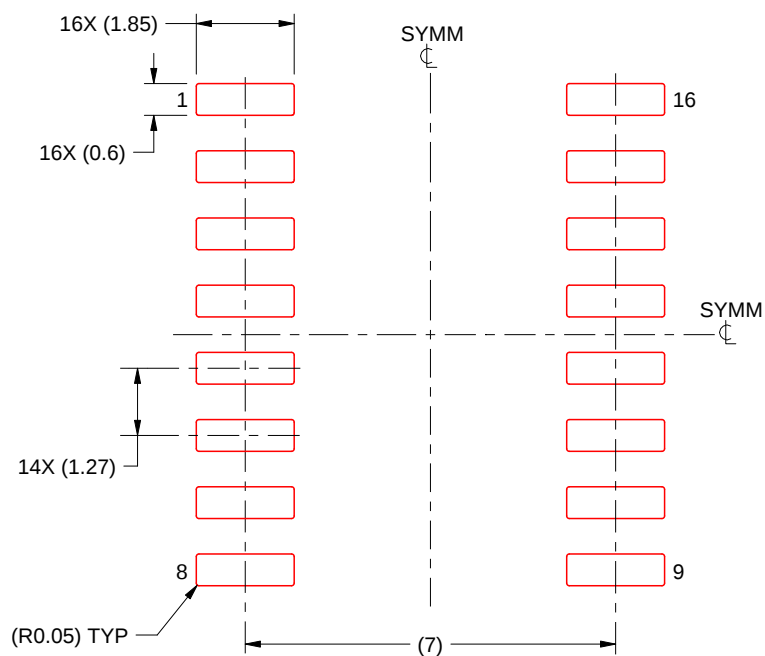
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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