

SN74LVC10A 三路 3 输入正与非门

1 特性

- 工作电压范围为 1.65V 至 3.6V
- 额定工作温度范围为 -40°C 至 85°C 以及 -40°C 至 125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时, t_{pd} 最大值为 4.9ns
- V_{OLP} (输出接地反弹) 典型值 $< 0.8V$ ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值 $> 2V$ ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)
- 闩锁性能超过 250mA, 符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)

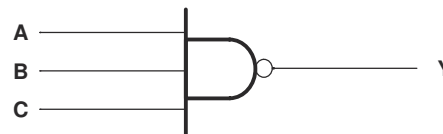
2 说明

该三路 3 输入正与非门可在 1.65V 至 3.6V V_{CC} 电压下运行。

封装信息

器件型号	封装尺寸 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74LVC10A	BQA (WQFN , 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC , 14)	8.65mm × 6mm	8.65mm × 3.9mm
	DB (SSOP , 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	NS (SOP , 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP , 14)	5mm × 6.4mm	5mm × 4.4mm
	RGY (VQFN , 14)	3.5mm × 3.5mm	3.5mm × 3.5mm

- 如需更多信息, 请参阅节 10。
- 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图, 每个逻辑门 (正逻辑)

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3 引脚配置和功能

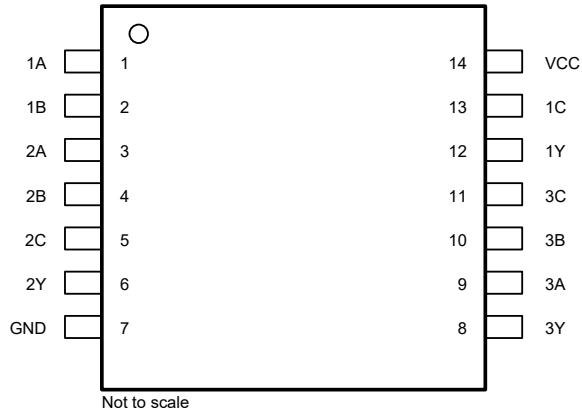


图 3-1. SN74LVC10A D、DB、NS 或 PW 封装；14 引脚 SOIC、SSOP、SOP 或 TSSOP (顶视图)

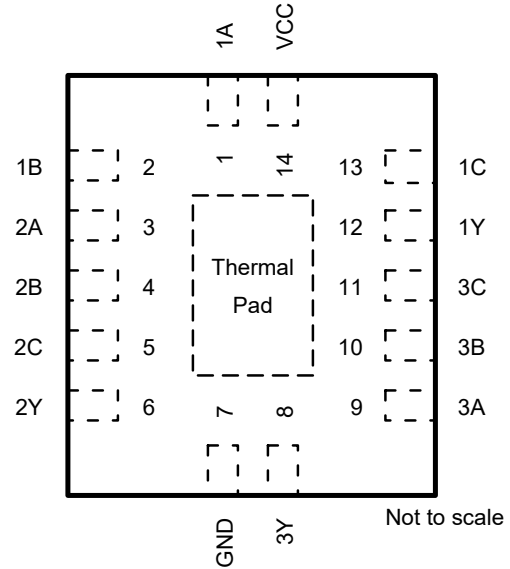


图 3-2. SN74LVC10A BQA 封装，14 引脚 WQFN (顶视图)

表 3-1. 引脚功能

引脚		I/O ⁽¹⁾	说明
名称	编号		
1A	1	输入	通道 1，输入 A
1B	2	输入	通道 1，输入 B
2A	3	输入	通道 2，输入 A
2B	4	输入	通道 2，输入 B
2C	5	输入	通道 2，输入 C
2Y	6	输出	通道 2，输出 Y
GND	7	—	接地
3Y	8	输出	通道 3，输出 Y
3A	9	输入	通道 3，输入 A
3B	10	输入	通道 3，输入 B
3C	11	输入	通道 3，输入 C
1Y	12	输出	通道 1，输出 Y
1C	13	输入	通道 1，输入 C
V _{CC}	14	—	正电源
散热焊盘		—	将 GND 引脚连接到裸露的散热焊盘以确保正确操作。使用多个过孔将散热焊盘连接到任何内部 PCB 接地平面，以获得良好的热性能。

(1) I = 输入、O = 输出、P = 电源、FB = 反馈、GND = 接地、N/A = 不适用

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）

		最小值	最大值	单位
V_{CC}	电源电压范围	-0.5	6.5	V
V_I	输入电压范围 ⁽¹⁾	-0.5	6.5	V
V_O	输出电压范围 ^{(1) (2)}	-0.5	$V_{CC} + 0.5$	V
I_{IK}	输入钳位电流	$V_I < 0$	-50	mA
I_{OK}	输出钳位电流	$V_O < 0$	-50	mA
I_O	持续输出电流		± 50	mA
	通过 V_{CC} 或 GND 的持续电流		± 100	mA
T_{stg}	贮存温度范围	-65	150	°C
P_{tot}	功率耗散	$T_A = -40^\circ\text{C}$ 至 125°C ^{(3) (4)}	500	mW

(1) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。

(2) V_{CC} 的值在建议运行条件表中提供。

(3) 对于 D 封装：在 70°C 以上时， P_{tot} 值以 8mW/K 的幅度线性降额。

(4) 对于 DB、NS 和 PW 封装：在 60°C 以上时， P_{tot} 值以 5.5mW/K 的幅度线性降额。

4.2 ESD 等级

		值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准 ⁽¹⁾	± 2000 V

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。

4.3 建议运行条件

		$T_A = 25^\circ\text{C}$		-40 至 85°C		-40 至 125°C		单位	
		最小值	最大值	最小值	最大值	最小值	最大值		
V_{CC}	电源电压	运行	1.65	3.6	1.65	3.6	1.65	3.6	V
	仅数据保留		1.5		1.5		1.5		
V_{IH}	高电平输入电压	$V_{CC} = 1.65\text{V}$ 至 1.95V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{V}$ 至 2.7V	1.7		1.7		1.7		
		$V_{CC} = 2.7\text{V}$ 至 3.6V	2		2		2		
V_{IL}	低电平输入电压	$V_{CC} = 1.65\text{V}$ 至 1.95V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{V}$ 至 2.7V		0.7		0.7		0.7	
		$V_{CC} = 2.7\text{V}$ 至 3.6V		0.8		0.8		0.8	
V_I	输入电压	0	5.5	0	5.5	0	5.5	V	
V_O	输出电压	0	V_{CC}	0	V_{CC}	0	V_{CC}	V	
I_{OH}	高电平输出电流	$V_{CC} = 1.65\text{V}$		-4		-4		-4	mA
		$V_{CC} = 2.3\text{V}$		-8		-8		-8	
		$V_{CC} = 2.7\text{V}$		-12		-12		-12	
		$V_{CC} = 3\text{V}$		-24		-24		-24	
I_{OL}	低电平输出电流	$V_{CC} = 1.65\text{V}$		4		4		4	mA
		$V_{CC} = 2.3\text{V}$		8		8		8	
		$V_{CC} = 2.7\text{V}$		12		12		12	
		$V_{CC} = 3\text{V}$		24		24		24	

4.4 热性能信息

热性能指标 ⁽¹⁾		SN74LVC10A					单位	
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)		RGY (VQFN)
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚		14 引脚
R _{θJA}	结至环境热阻	102.3	127.8	96	123.8	150.8	92.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅[半导体和 IC 封装热指标](#)应用报告。

4.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V _{CC}	T _A = 25°C			-40°C 至 85°C		-40°C 至 125°C		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V _{OH}	I _{OH} = -100 μA	1.65V 至 3.6V	V _{CC} - 0.2			V _{CC} - 0.2		V _{CC} - 0.3		V
	I _{OH} = -4mA	1.65V	1.29			1.2		1.05		
	I _{OH} = -8mA	2.3V	1.9			1.7		1.55		
	I _{OH} = -12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
V _{OL}	I _{OL} = 100 μA	1.65V 至 3.6V				0.1		0.2		V
	I _{OL} = 4mA	1.65V				0.24		0.45		
	I _{OL} = 8mA	2.3V				0.3		0.7		
	I _{OL} = 12mA	2.7V				0.4		0.4		
	I _{OL} = 24mA	3V				0.55		0.55		
I _I	V _I =5.5V 或 GND	3.6V				±1		±5		μA
I _{CC}	V _I = V _{CC} 或 GND, I _O = 0	3.6V				1		10		μA
ΔI _{CC}	一个输入电压为 V _{CC} - 0.6V, 其他输入电压为 V _{CC} 或 GND	2.7V 至 3.6V				500		500		μA
C _i	V _I = V _{CC} 或 GND	3.3V				5				pF

4.6 开关特性

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅[负载电路和电压波形](#)）

参数	从 (输入)	至 (输出)	V _{CC}	T _A = 25°C			-40°C 至 85°C		-40°C 至 125°C		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t _{pd}	A、B 或 C	Y	1.8V ± 0.15V	1	4.2	10.1	1	10.6	1	12.1	ns
			2.5V ± 0.2V	1	2.9	7.3	1	7.8	1	9.9	
			2.7V	1	3.1	5.6	1	5.8	1	7.4	
			3.3V ± 0.3V	1	2.7	4.7	1	4.9	1	6	
t _{sk(o)}			3.3V ± 0.3V				1		1.5	ns	

4.7 工作特性

$T_A = 25^\circ\text{C}$

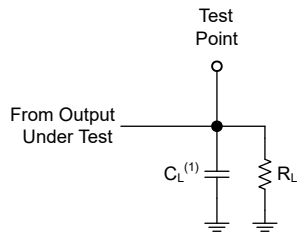
参数		测试条件	V _{CC}	典型值	单位
C _{pd}	每个栅极的功率耗散电容	f = 10MHz	1.8V	9	pF
			2.5V	10	
			3.3V	11	

5 参数测量信息

对于下表中列出的示例，波形之间的相位关系是任意选择的。所有输入脉冲均由具有以下特性的发生器提供：
PRR ≤ 1MHz，Z_O = 50Ω，t_r ≤ 2.5ns。

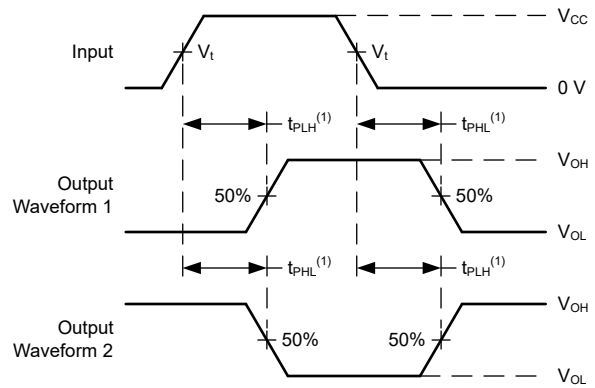
输出单独测量，每次测量一个输入转换。

V _{CC}	V _t	R _L	C _L	ΔV
1.8V ± 0.15V	V _{CC} /2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V _{CC} /2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



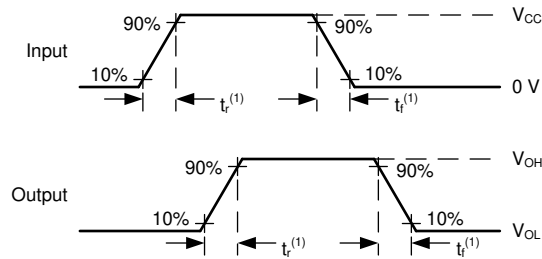
(1) C_L 包括探头和测试夹具电容。

图 5-1. 推挽输出的负载电路



(1) t_{PLH} 和 t_{PHL} 之间的较大者与 t_{pd} 相同。

图 5-2. 电压波形传播延迟



(1) t_r 和 t_f 之间的较大值与 t_t 相同。

图 5-3. 电压波形，输入和输出转换时间

6 详细说明

6.1 概述

SN74LVC10A 以正逻辑执行布尔函数 $Y = \overline{A \cdot B \cdot C}$ 或 $Y = \overline{A} + \overline{B} + \overline{C}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将该此类器件用作转换器。

6.2 功能方框图

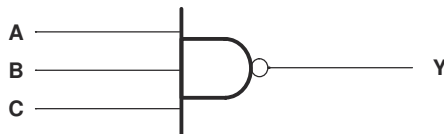


图 6-1. 逻辑图，每个逻辑门（正逻辑）

6.3 器件功能模式

表 6-1. 功能表（每个逻辑门）

输入			输出 Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 电源相关建议

电源可以是 [建议运行条件](#) 中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 引脚必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 $0.1\mu\text{F}$ ；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 $0.01\mu\text{F}$ 或 $0.022\mu\text{F}$ 。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\mu\text{F}$ 和 $1\mu\text{F}$ 通常并联使用。为了获得更佳效果，旁路电容器必须尽可能靠近电源引脚安装。

7.2 布局

7.2.1 布局指南

使用多输入和多通道逻辑器件时，输入不得悬空。在许多情况下，未使用数字逻辑器件的功能或部分功能；例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时。此类未使用的输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的操作状态。数字逻辑器件的所有未使用输入必须连接到由输入电压规范定义的逻辑高电平电压或逻辑低电平电压，以防止其悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，输入连接到 GND 或 VCC，以对逻辑功能更有意义或更方便者为准。

7.2.2 布局示例

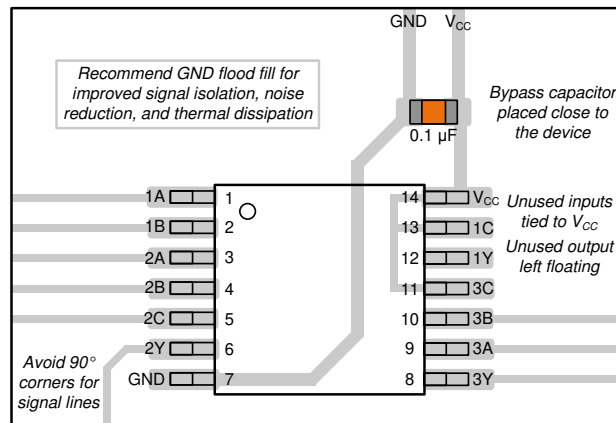


图 7-1. SN74LVC10A 的示例布局

8 器件和文档支持

8.1 文档支持 (模拟)

8.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 8-1. 相关链接

器件	产品文件夹	立即订购	技术文档	工具 & 软件	支持 & 社区
SN74LVC10A	点击此处	点击此处	点击此处	点击此处	点击此处

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision P (May 2024) to Revision Q (August 2024)	Page
• 更新了 R _{θJA} 值：D 封装从 86 更新为 127.8，NS 封装从 76 更新为 123.8，PW 封装从 113 更新为 150.8，RGY 封装从 47 更新为 92.1，所有值均以 °C/W 为单位.....	5

Changes from Revision O (July 2005) to Revision P (May 2024)	Page
• 向 封装信息表 、 引脚配置和功能 部分以及 热性能信息表 中添加了 BQA 封装.....	1
• 添加了 应用 部分、 封装信息表 、 ESD 等级表 、 热性能信息表 、 器件功能模式 、 应用和实施 部分、 器件和文档支持 部分以及 机械 、 封装和可订购信息 部分.....	1
• 删除了 特性 中的机器放电模型.....	1

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC10ABQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ABQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10AD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10AD.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADT.B	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ANSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10APW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWT.B	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A
SN74LVC10ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A
SN74LVC10ARGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC10ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC10ADBDR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC10ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC10ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC10ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC10APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC10ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC10ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC10ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC10ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC10ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC10ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC10APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC10APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC10APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC10ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0
SN74LVC10ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVC10AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC10APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

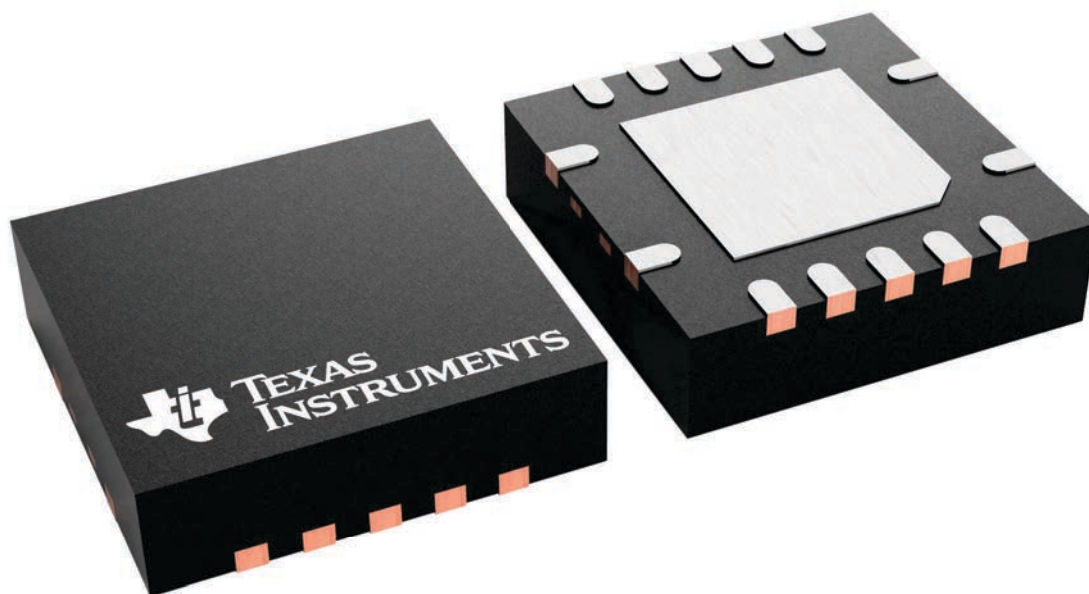
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

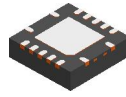
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

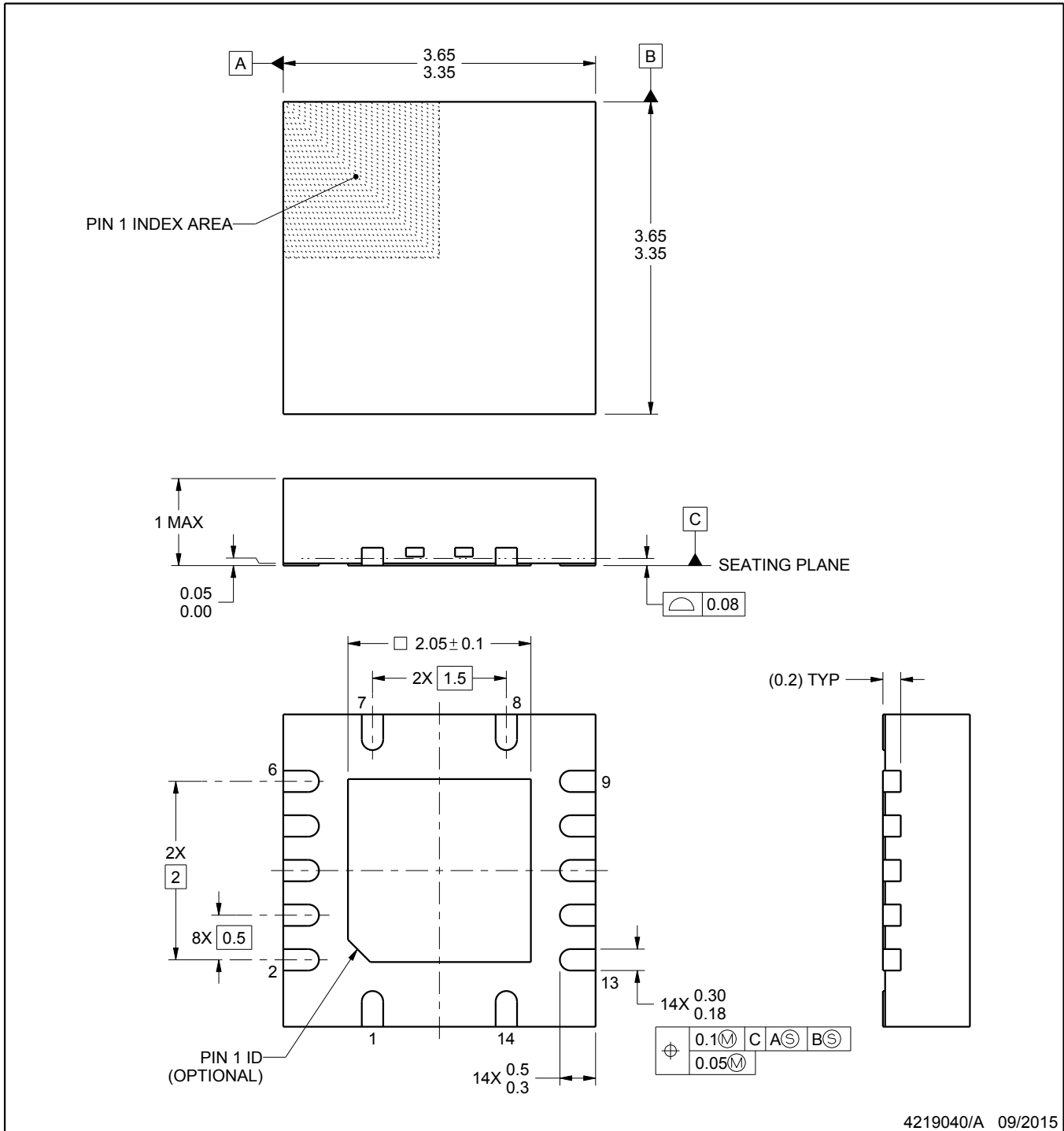
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

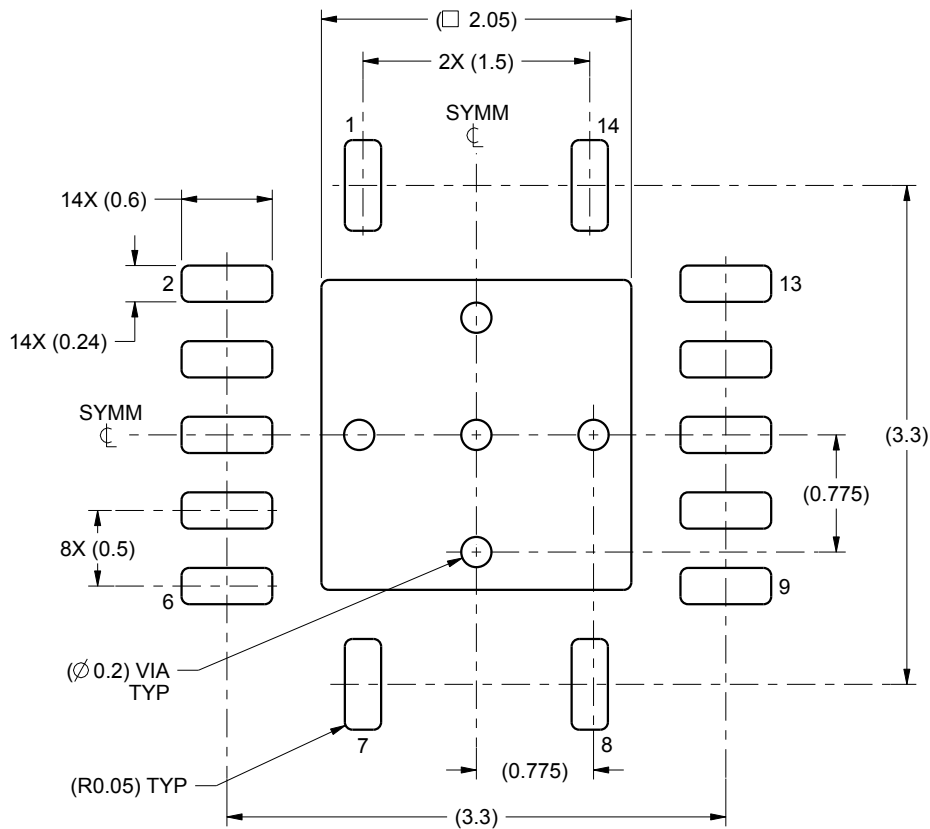
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

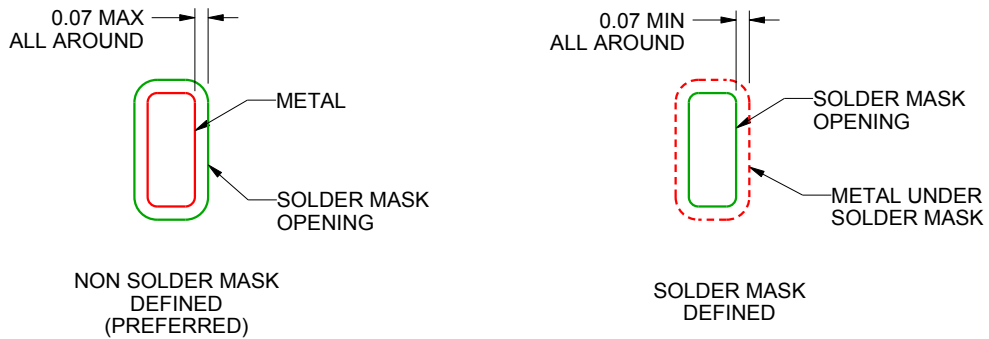
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

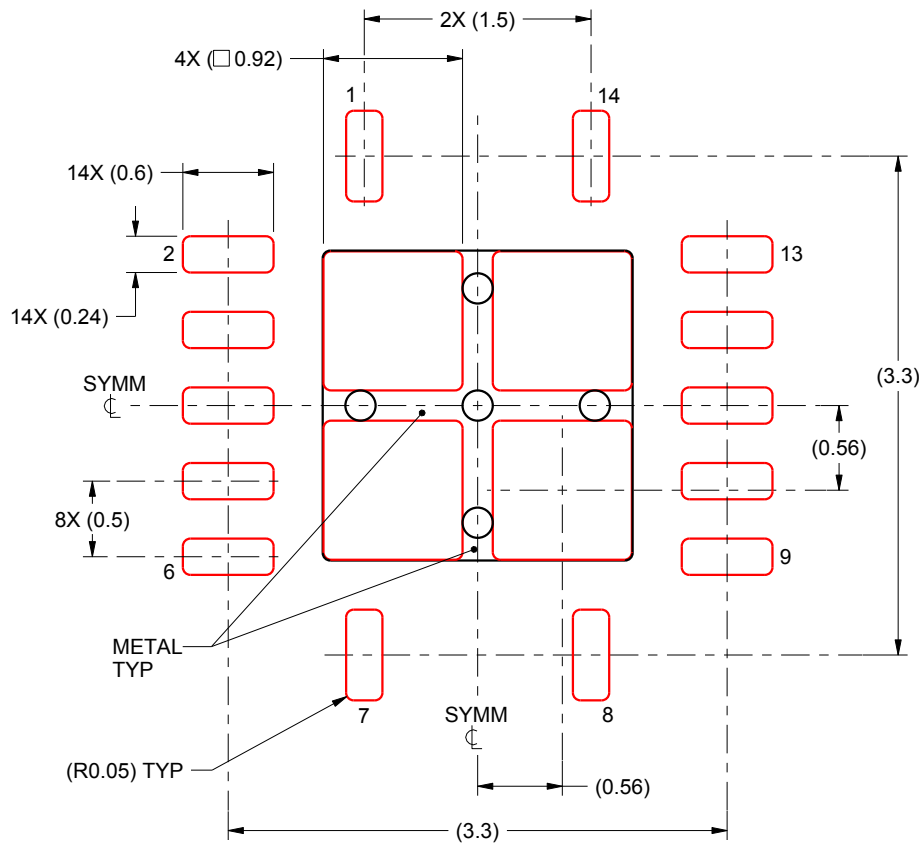
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

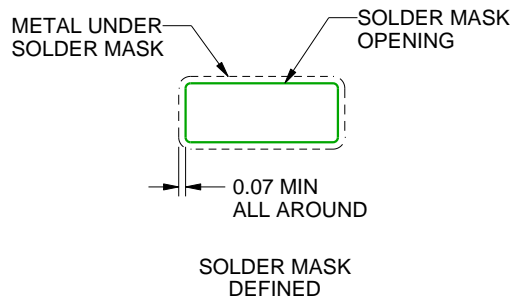
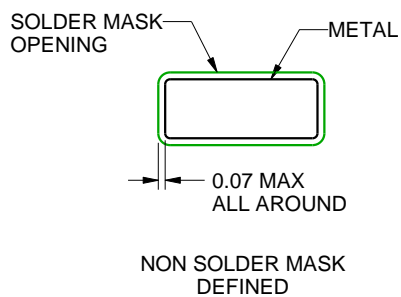
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

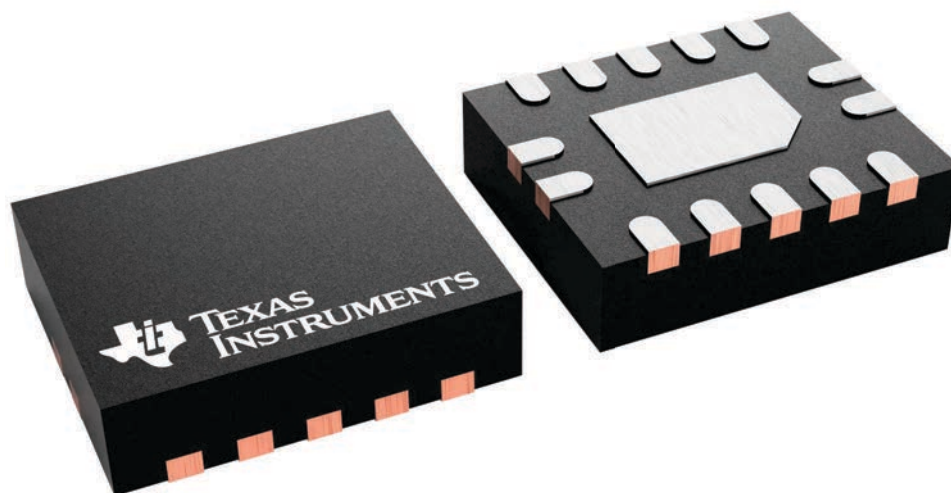
BQA 14

WQFN - 0.8 mm max height

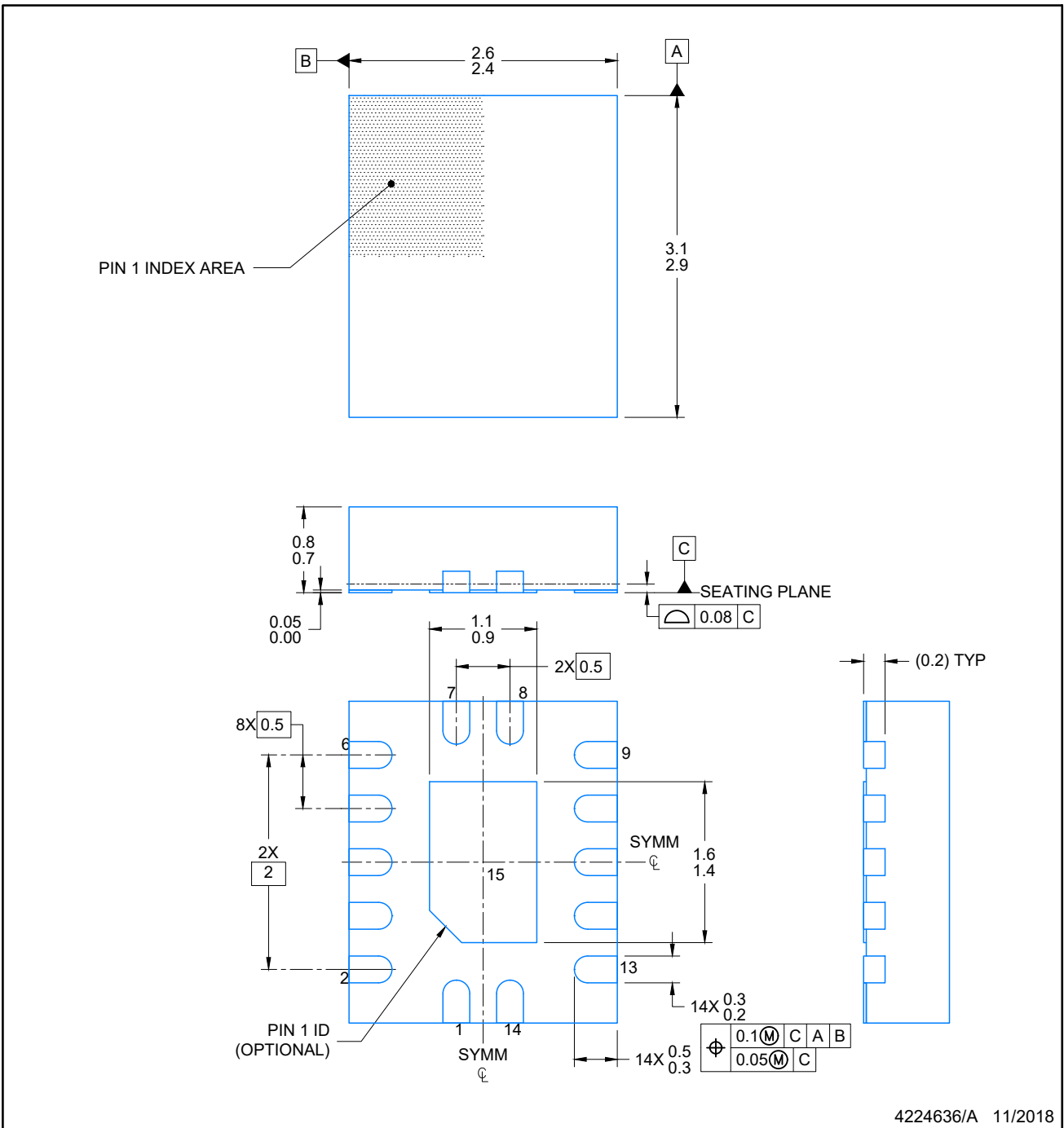
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

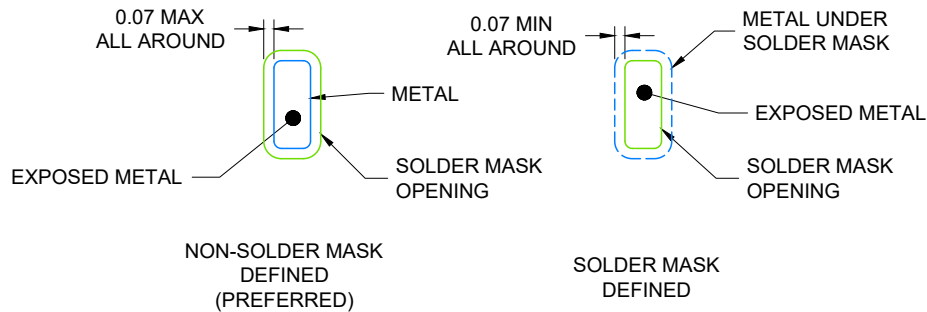
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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