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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2015) to Revision B	Page
• Changed body size in Device Information table	1
• Changed body size in Device Information table	1
• Corrected typo 'active-low' to active-low in the Pin Functions table.	3

Changes from Original (August 2004) to Revision A	Page
• Added <i>Pin Configuration and Functions</i> section, <i>Storage Conditions</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed <i>Ordering Information</i> table	1

5 Pin Configuration and Functions

**N or PW Package
20-Pin PDIP or TSSOP
Top View**

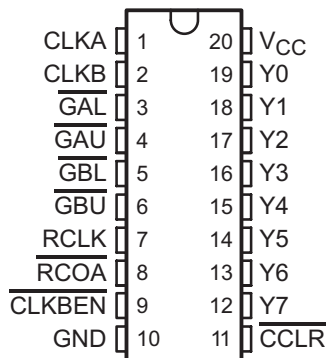


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CCLR}}$	11	I	Clock clear, asynchronous active-low clear for both counters
CLKA	1	I	Clock A, rising edge count clock
CLKB	2	I	Clock B, rising edge count clock
$\overline{\text{CLKBEN}}$	9	I	Clock B enable, active-low allows clocking for counter B; connect to $\overline{\text{RCOA}}$ for 32-bit counter.
$\overline{\text{GAL}}$	3	I	Gate A lower byte, active-low puts lower byte of stored counter A on the Y bus.
$\overline{\text{GAU}}$	4	I	Gate A upper byte, active-low puts upper byte of stored counter A on the Y bus.
$\overline{\text{GBL}}$	5	I	Gate B lower byte, active-low puts lower byte of stored counter B on the Y bus.
$\overline{\text{GBU}}$	6	I	Gate B upper byte, active-low puts upper byte of stored counter B on the Y bus.
GND	10	—	Ground
RCLK	7	I	Register Clock, rising edge stores counters into an internal storage register.
$\overline{\text{RCOA}}$	8	O	Ready case overflow A, active low when counter A is full count and ready to overflow on next clock A.
V _{CC}	20	—	Power supply pin
Y0	19	O	Data output bit 0 (LSB)
Y1	18	O	Data output bit 1
Y2	17	O	Data output bit 2
Y3	16	O	Data output bit 3
Y4	15	O	Data output bit 4
Y5	14	O	Data output bit 5
Y6	13	O	Data output bit 6
Y7	12	O	Data output bit 7 (MSB)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.5	7	V
V _I	Input voltage ⁽²⁾	−0.5	7	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	7	V
V _O	Output voltage ⁽²⁾⁽³⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−20	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±35	mA
	Continuous current through V _{CC} or GND		±70	mA
T _J	Junction Temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

		V _{CC}	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	2 V	1.5		V
		3 V to 3.6 V	V _{CC} × 0.7		
		4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	2 V		0.5	V
		3 V to 3.6 V		V _{CC} × 0.3	
		4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	2 V		−50	μA
		3 V to 3.6 V		−6	mA
		4.5 V to 5.5 V		−12	
I _{OL}	Low-level output current	2 V		50	μA
		3 V to 3.6 V		6	mA
		4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise and fall rate	3 V to 3.6 V		100	ns/V
		4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV8154N	SN74LV8154PW	UNIT
		N (PDIP)	PW (TSSOP)	
		20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	54.9	100.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46.5	30.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	35.9	47.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	23.5	1.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	35.7	46.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH} Output high voltage	I _{OH} = –50 μA	2 V	1.9			V
	I _{OH} = –6 mA	3 V	2.48			
	I _{OH} = –12 mA	4.5 V	3.8			
V _{OL} Output low voltage	I _{OL} = 50 μA	2 V			0.1	V
	I _{OL} = 6 mA	3 V			0.44	
	I _{OL} = 12 mA	4.5 V			0.55	
I _I Input current	V _I = 5.5 V or GND	0 to 5.5 V			±1	μA
I _{OZ} Output off current	V _O = V _{CC} or GND	5.5 V			±5	μA
I _{CC} Supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	μA
I _{off} Off current	V _I or V _O = 0 to 5.5 V	0			5	μA
C _I Input capacitance	V _I = V _{CC} or GND	5 V		3		pF
C _O Output capacitance	V _O = V _{CC} or GND	5 V		5		pF
C _{pd} Power dissipation capacitance	C _L = No load, CCLK = 10 MHz RCLK = 1 MHz	5 V		56		pF

6.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

		MIN	UNIT
t _w Pulse duration	CLKA, CLKB, RCLK high or low	10	ns
	$\overline{\text{CCLR}}$ low	20	
t _{su} Set-up time	$\overline{\text{CLKBEN}}$ low before CLKB↑	10	ns
	$\overline{\text{CCLR}}$ high (inactive) before CLKA↑ or CLKB↑	10	
	CLKA↑ or CLKB↑ before RCLK↑	10	
	RCLK↑ before $\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ low	10	
	$\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ high (inactive) before RCLK↑	10	
t _h Hold time	$\overline{\text{CLKBEN}}$ low after CLKB↑	0	ns
	CLKA or CLKB after RCLK	0	
t _z ⁽¹⁾ Z-period	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$ all high before one of them switches low	200	ns

(1) t_z condition: C_L = 50 pF, R_L = 1 kΩ

6.7 Switching Characteristics - $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
f_{MAX}			$C_L = 15\text{ pF}$	40			MHz
			$C_L = 50\text{ pF}$	25			
t_{pd}	RCLK	Y	$C_L = 15\text{ pF}$	1	22	38	ns
	CLKA	\overline{RCOA}		1	26	44	
t_{PLH}	\overline{CCLR}	\overline{RCOA}		1	18	32	ns
t_{en}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	27	46	ns
t_{dis}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	12	21	ns
t_{pd}	RCLK	Y	$C_L = 50\text{ pF}$	1	25	42	ns
	CLKA	\overline{RCOA}		1	28	46	
t_{PLH}	\overline{CCLR}	\overline{RCOA}		1	20	35	ns
t_{en}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	30	50	ns
t_{dis}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	14	24	ns

6.8 Switching Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
f_{MAX}			$C_L = 15\text{ pF}$	40			MHz
			$C_L = 50\text{ pF}$	25			
t_{pd}	RCLK	Y	$C_L = 15\text{ pF}$	1	14	25	ns
	CLKA	\overline{RCOA}		1	16	27	
t_{PLH}	\overline{CCLR}	\overline{RCOA}		1	12	20	ns
t_{en}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	16	28	ns
t_{dis}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	8	15	ns
t_{pd}	RCLK	Y	$C_L = 50\text{ pF}$	1	16	27	ns
	CLKA	\overline{RCOA}		1	17	28	
t_{PLH}	\overline{CCLR}	\overline{RCOA}		1	13	21	ns
t_{en}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	18	30	ns
t_{dis}	$\overline{GAL}, \overline{GAU}, \overline{GBL}, \overline{GBU}$	Y		1	9	16	ns

6.9 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.75		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.4		V

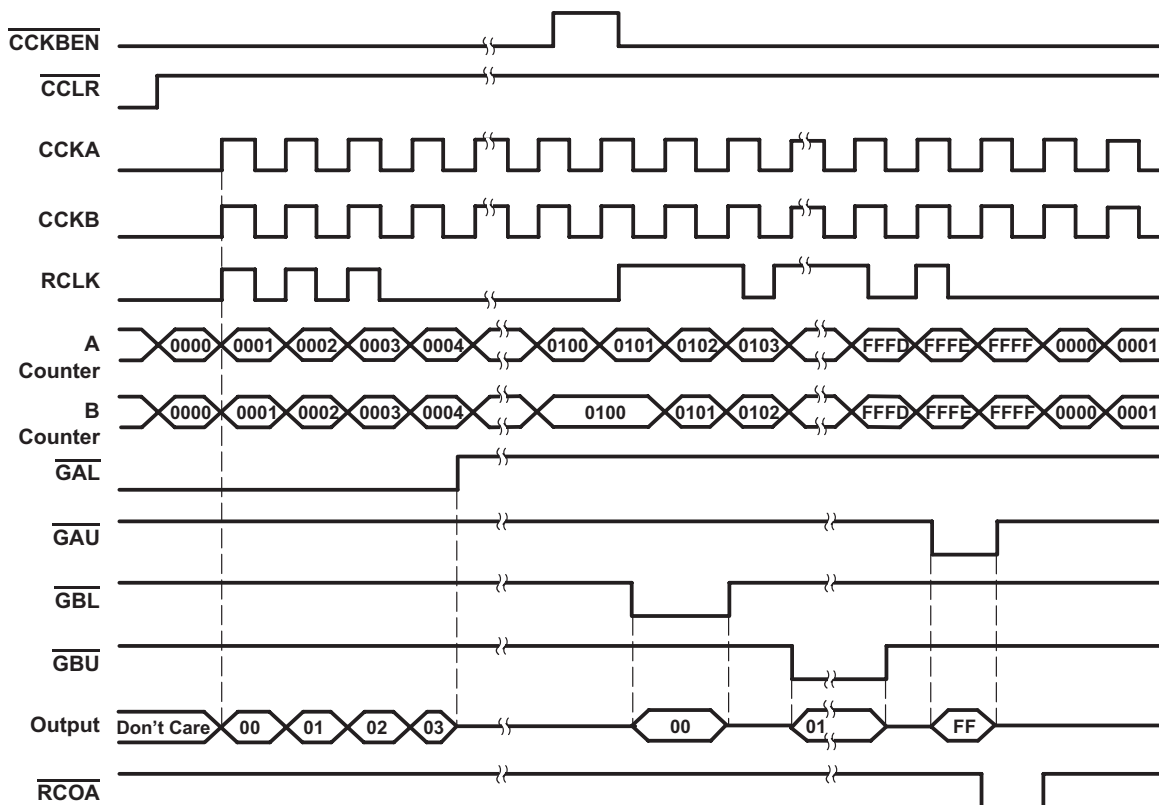


Figure 1. Timing Diagram

6.10 Typical Characteristics

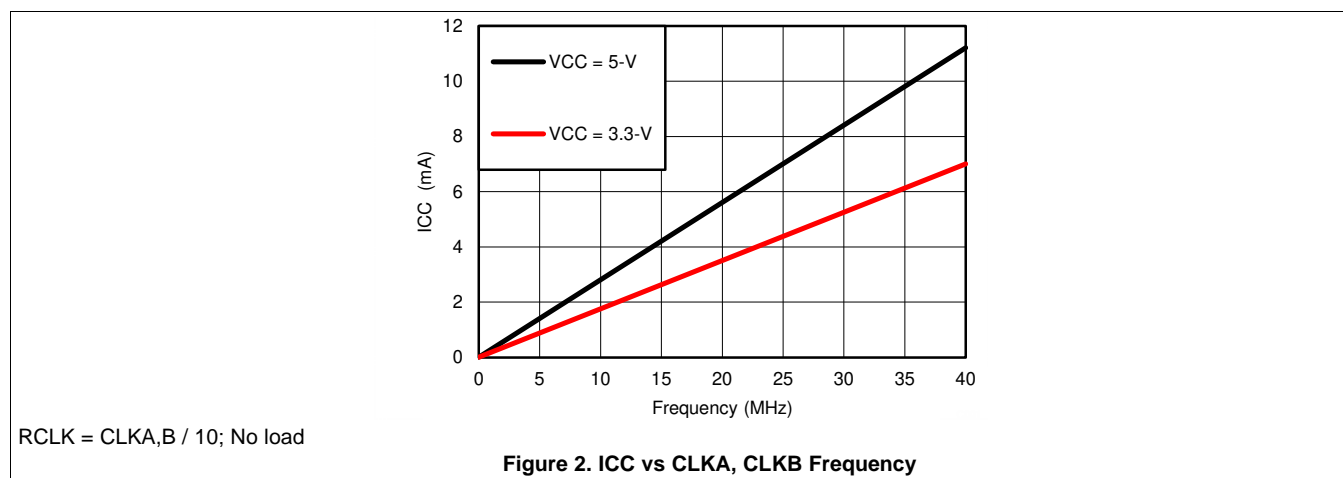
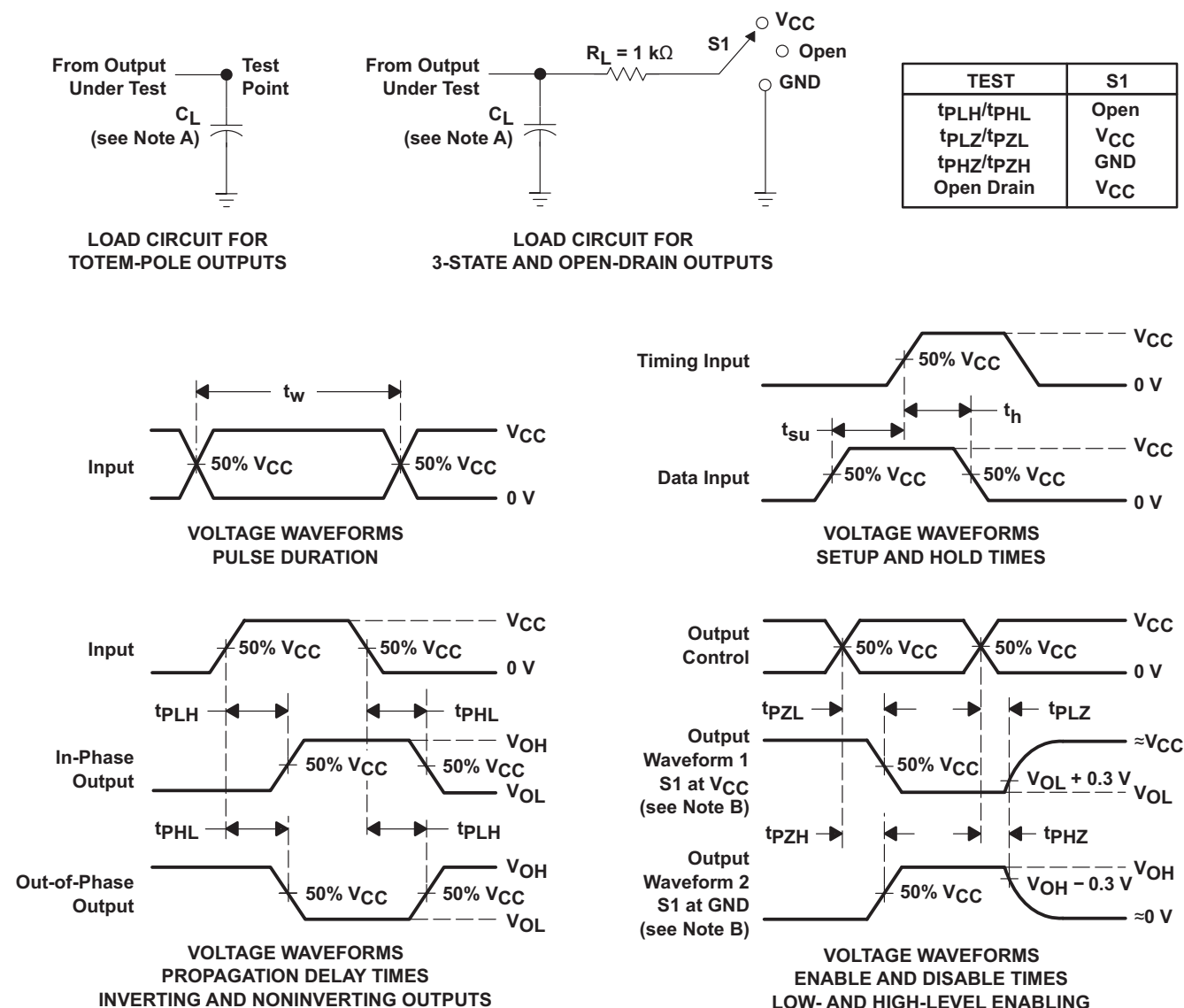


Figure 2. ICC vs CLKA, CLKB Frequency

7 Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV8154 device is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V V_{CC} operation. The counters have dedicated clock inputs. The counters share a storage register clock and an asynchronous clear input. The 32-bit storage register can be mapped on the output bus 8-bit at a time. Four bus reads are needed to access the contents of both counters. The two counters can be chained by connecting CLKBEN to RCOA.

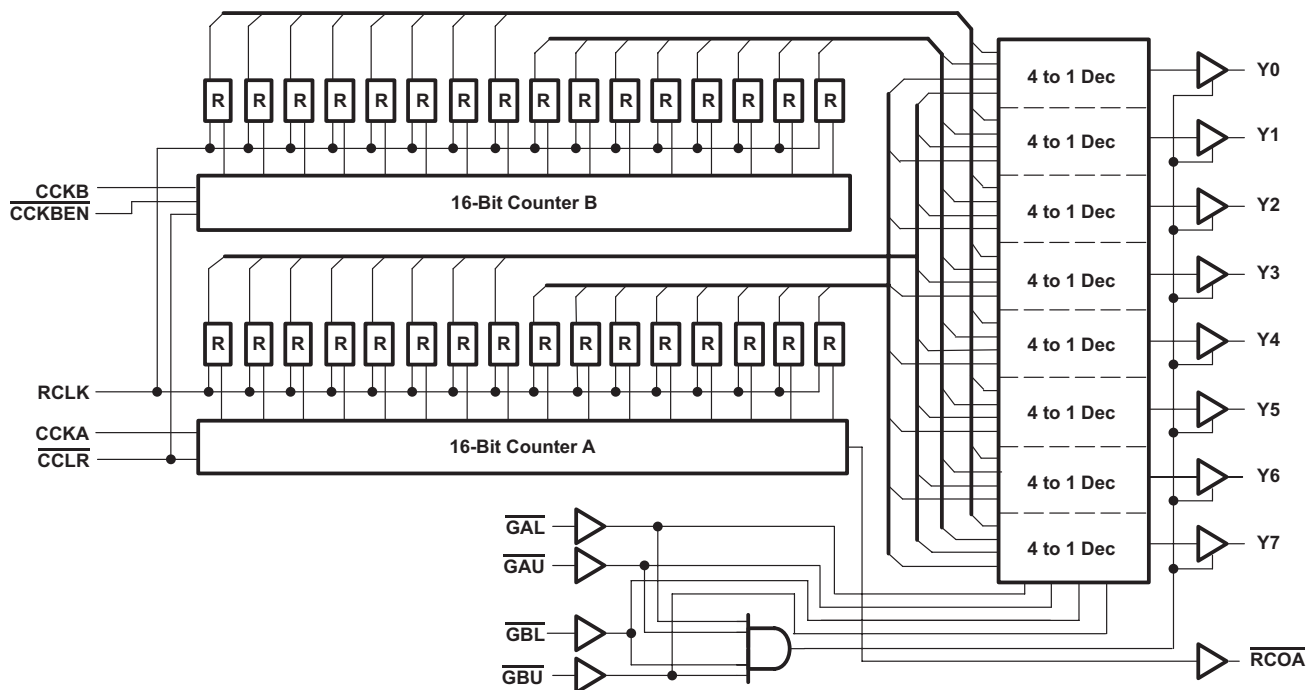
This 16-bit counter (A or B) feeds a 16-bit storage register, and each storage register is further divided into an upper byte and lower byte. The \overline{GAL} , \overline{GAU} , \overline{GBL} , \overline{GBU} inputs are used to select the byte that needs to be output at Y0–Y7. CLKA is the clock for A counter, and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32-bit counter can be realized by connecting CLKA and CLKB together and by connecting \overline{RCOA} to \overline{CLKBEN} .

To ensure the high-impedance state during power up or power down, \overline{GAL} , \overline{GAU} , \overline{GBL} , and \overline{GBU} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

Two 16-bit counters count up on each positive edge of the respective clock input. \overline{RCOA} is set low when counter A is full count. Counter B clock is gated by the CCKBEN input. Connecting \overline{RCOA} to CCKBEN together chains the counters to make one 32-bit counter.

Asynchronous \overline{CCLR} input resets both counter to zero.

One 32-bit storage register records the contents of both counters on the rising edge of RCLK. The contents of the storage register are saved until the next rising edge of the RCLK.

Mapped output bus can be set to high impedance or output 8-bits of the 32-bit storage register.

8.4 Device Functional Modes

[Table 2](#) lists the functional modes of the SN74LV8154.

Table 2. Function Table

INPUTS				OUTPUT Y _n
$\overline{\text{GAL}}$	$\overline{\text{GAU}}$	$\overline{\text{GBL}}$	$\overline{\text{GBU}}$	
L	H	H	H	Lower byte in A storage register
H	L	H	H	Upper byte in A storage register
H	H	L	H	Lower byte in B storage register
H	H	H	L	Upper byte in B storage register
H	H	H	H	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV8154 can count any two events up to a count of 65,535 per storage register read. It can also count one event up to a count of 4,294,967,295 per storage register read.

9.2 Typical Application

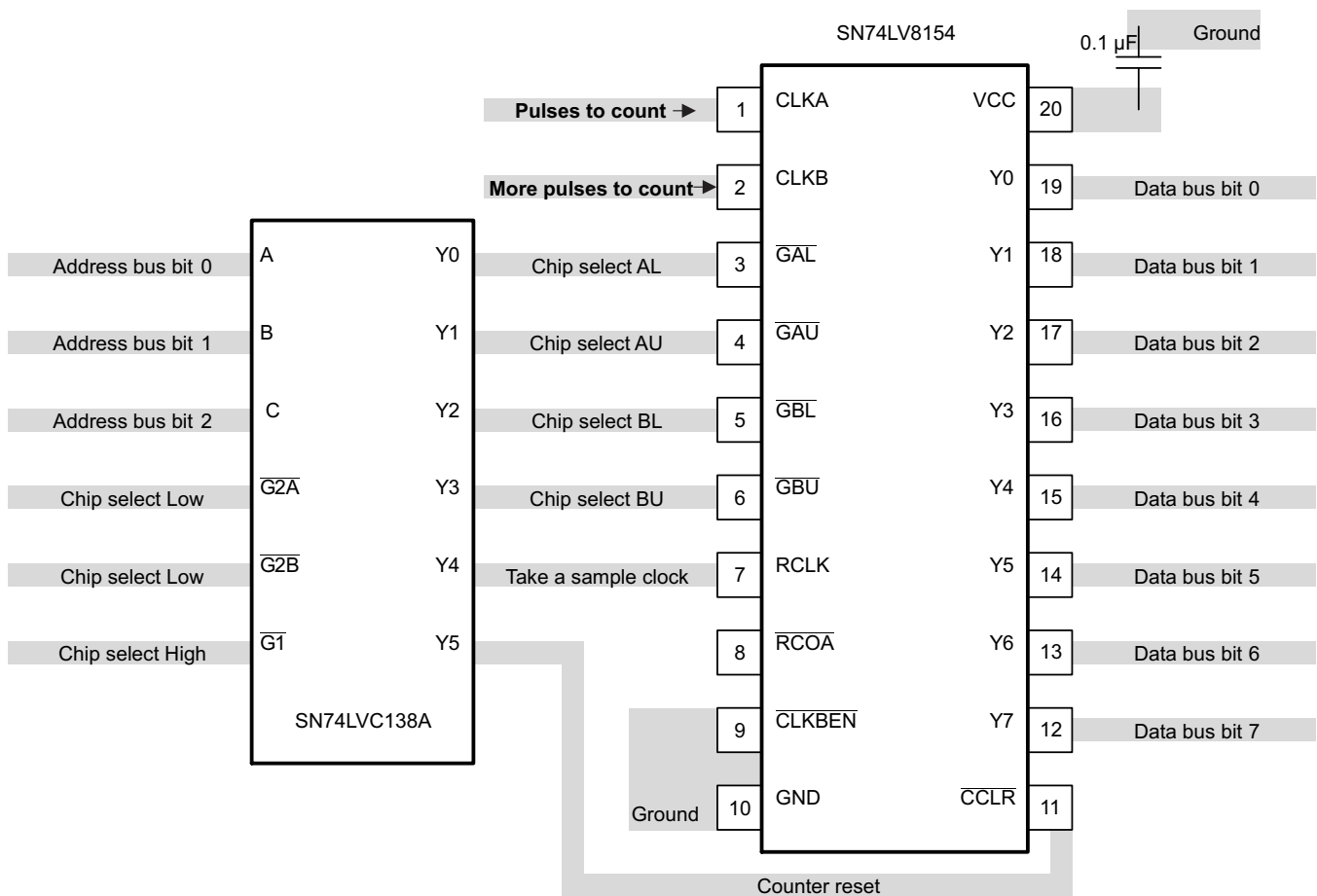


Figure 4. Dual Counter With Address Mapping

9.2.1 Design Requirements

- V_{CC} must be acceptable for both SN74LV8154 and SN74LVC138A.
- \overline{CCLR} low time must be greater than 20 ns.
- 8 bytes of unique address space are needed.
- CLKA and CLKB inputs must have input transition rate specified in [Recommended Operating Conditions](#).
- RCLK and \overline{CCLR} inputs must be free of glitches to prevent accidental register saves or counter clears.

Typical Application (continued)

9.2.2 Detailed Design Procedure

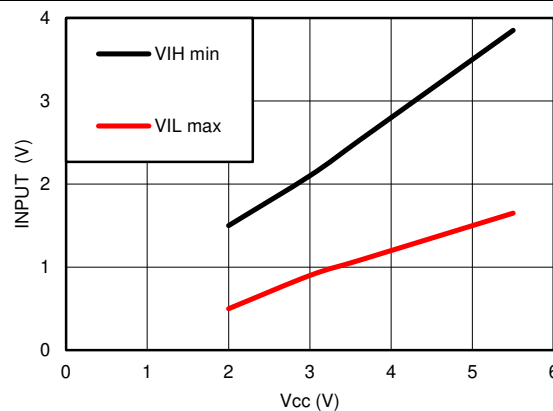
- Connect Y0 through Y7 to the data bus.
- Connect A, B, and C to lower address bus lines.
- Connect $\overline{G2A}$, $\overline{G2B}$, and G1 to decoded addresses to provide 8 or more unique memory locations.
- Connect two pulse sources to CLKA and CLKB inputs. If sources have noise or slow edges then pass the signal through a Schmitt trigger buffer first.
- If only one counter is needed, connect the single pulse source to both CLKA and CLKB.
- Also connect CLKBEN to RCOA instead of ground.

Table 3. Function Table

INPUTS ⁽¹⁾						OUTPUT ⁽¹⁾	RESULT
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Yn	
L	X	X	X	X	X	Z	No action
X	H	X	X	X	X	Z	No action
X	X	H	X	X	X	Z	No action
H	L	L	L	L	L	A lower byte	Read lower byte of counter A storage register
H	L	L	L	L	H	A upper byte	Read upper byte of counter A storage register
H	L	L	L	H	L	B lower byte	Read lower byte of counter B storage register
H	L	L	L	H	H	B upper byte	Read upper byte of counter B storage register
H	L	L	H	L	L	Z	Save counters into storage register after changing any input
H	L	L	H	L	H	Z	Reset both counters to zero
H	L	L	H	H	L	Z	No action
H	L	L	H	H	H	Z	No action

(1) L = low, H = high, X = don't care, Z = high Impedance.

9.2.3 Application Curve


Figure 5. Input Voltage Range vs VCC

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended. If there are multiple V_{CC} terminals then 0.01- μ F or 0.022- μ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example

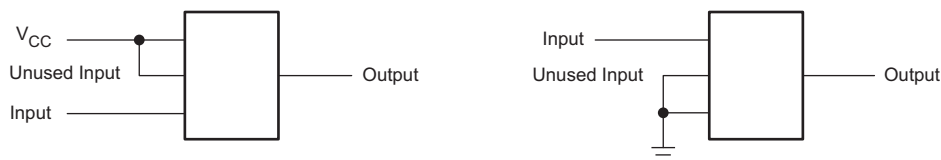


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

12.2 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV8154N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV8154N
SN74LV8154N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV8154N
SN74LV8154NE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV8154N
SN74LV8154PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	LV8154
SN74LV8154PW.B	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	LV8154
SN74LV8154PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8154
SN74LV8154PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8154

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV8154 :

- Enhanced Product : [SN74LV8154-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8154PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

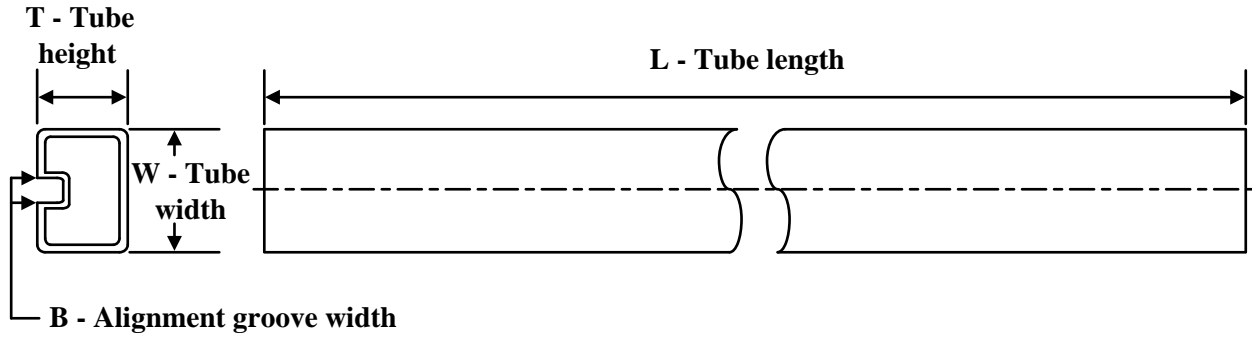
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8154PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV8154N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LV8154N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LV8154NE4	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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