SN74LV74A-Q1 汽车类双路正边沿触发式 D 型触发器

1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V V_{CC}
- 电压为 5V 时，t_{pd} 最大值为 13ns
- V_{OLP}（输出接地反弹）典型值小于 0.8V（V_{CC} = 3.3V、T_A = 25°C 时）
- V_{OHV}（输出 V_{OH} 下冲）典型值大于 2.3V（V_{CC} = 3.3V、T_A = 25°C 时）
- 所有端口上均支持混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

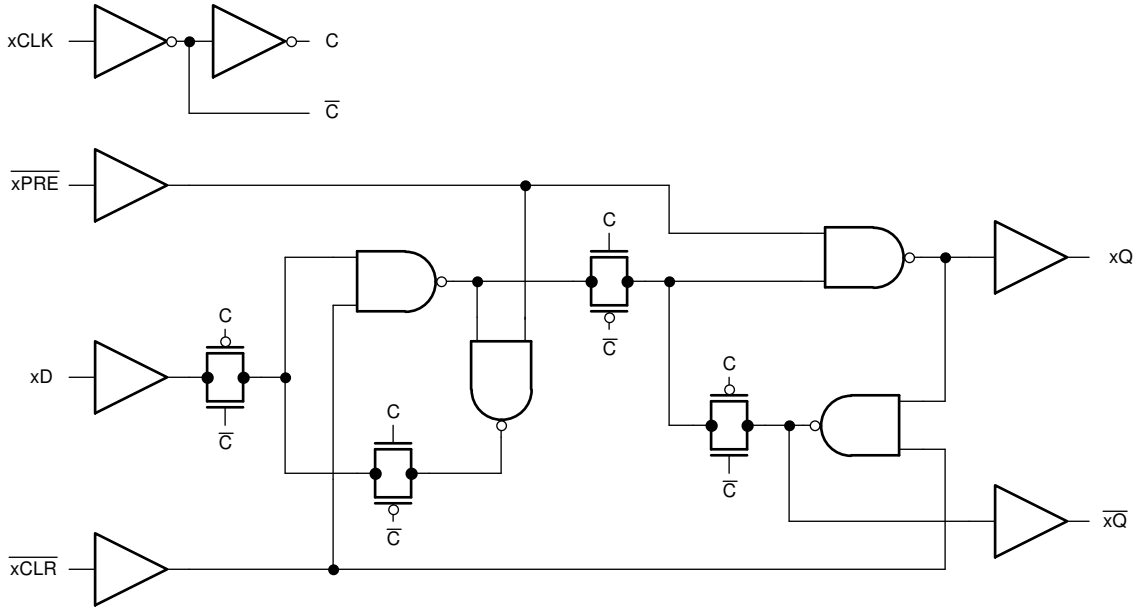
2 说明

这款双路上升沿触发 D 类触发器需在 2V 至 5.5V V_{CC} 下运行。

封装信息

器件型号	封装 [1]	封装尺寸 [2]
SN74LV74A-Q1	PW（TSSOP，14）	5.00 mm x 6.4 mm
	D（SOIC，14）	8.65 mm x 6 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



展示各触发器的逻辑图（正逻辑）

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3 Revision History

Changes from Revision B (April 2008) to Revision C (August 2023)	Page
• 添加了*封装信息*表、*引脚功能*表、*ESD 等级*表、*热信息*表、*器件功能模式*、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1

4 Pin Configuration and Functions

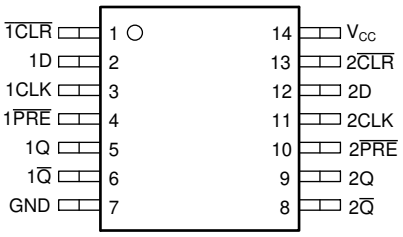


图 4-1. D and PW Package 14-Pin SOIC and TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	1 $\overline{CLR}$	I	1 clear
2	1D	I	1D input
3	1CLK	I	1 clock
4	1 $\overline{PRE}$	I	1 preset
5	1Q	O	1Q output
6	1 $\overline{Q}$	O	1 $\overline{Q}$ output
7	GND	–	GND
8	2 $\overline{Q}$	O	2 $\overline{Q}$ output
9	2Q	O	2Q output
10	2 $\overline{PRE}$	I	2 preset
11	2CLK	I	2 clock
12	2D	I	2D input
13	2 $\overline{CLR}$	I	2 clear
14	Vcc	–	Supply voltage input

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	7	V
V_I	Input voltage range(2)		– 0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		– 0.5	7	V
V_O	Output voltage range(2) (3)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 20	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	– 25	25	mA
	Continuous current through V_{CC} or GND		– 50	50	mA
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5-V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} x 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} x 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} x 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} x 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} x 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	µA
		V_{CC} = 2.3 V to 2.7 V		– 2	mA
		V_{CC} = 3 V to 3.6 V		– 6	
		V_{CC} = 4.5 V to 5.5 V		– 12	

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		D	PW	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –50 μA	2 to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			
		I_{OH} = –6 mA	3 V	2.48			
		I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	Low level output voltage	I_{OL} = 50 μA	2 to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I	Input leakage current	V_I = 5.5 V or GND	0 to 5.5 V			±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	μA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5 V	0			5	μA
C_i	Input Capacitance	V_I = V_{CC} or GND	3.3 V		2		pF
			5 V		2		

5.6 Timing Requirements, V_{CC} = 2.5 V ±0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ±0.2 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	8		9		ns
		CLK	8		9		
t_{su}	Setup time before CLK ↑	Data	8		9		ns
		$\overline{PRE}$ or $\overline{CLR}$ low	7		7		
t_h	Hold time, data after CLK ↑		0.5		0.5		ns

5.7 Timing Requirements, V_{CC} = 3.3 V ±0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	6		7		ns
		CLK	6		7		
t_{su}	Setup time before CLK ↑	Data	6		7		ns
		$\overline{PRE}$ or $\overline{CLR}$ low	5		5		
t_h	Hold time, data after CLK ↑		0.5		0.5		ns

5.8 Timing Requirements, V_{CC} = 5 V ±0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		ns
		CLK	5		5		
t_{su}	Setup time before CLK ↑	Data	5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ low	3		3		
t_h	Hold time, data after CLK ↑		0.5		0.5		ns

5.9 Switching Characteristics, V_{CC} = 2.5 V ±0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ±0.2 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 50 pF	30	70		25		MH_Z
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		13	17.4	1	20	ns
	CLK				14.2	20	1	23	

5.10 Switching Characteristics, V_{CC} = 3.3 V ±0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 50 pF	50	90		45		MH_Z
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		9.2	15.8	1	18	ns
	CLK				10.2	15.4	1	18	

5.11 Switching Characteristics, V_{CC} = 5 V ±0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 50 pF	90	140		75		MH_Z
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		6.6	9.7	1	12	ns
	CLK				7.2	9.3	1	13	

5.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.1	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	–0.8	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	

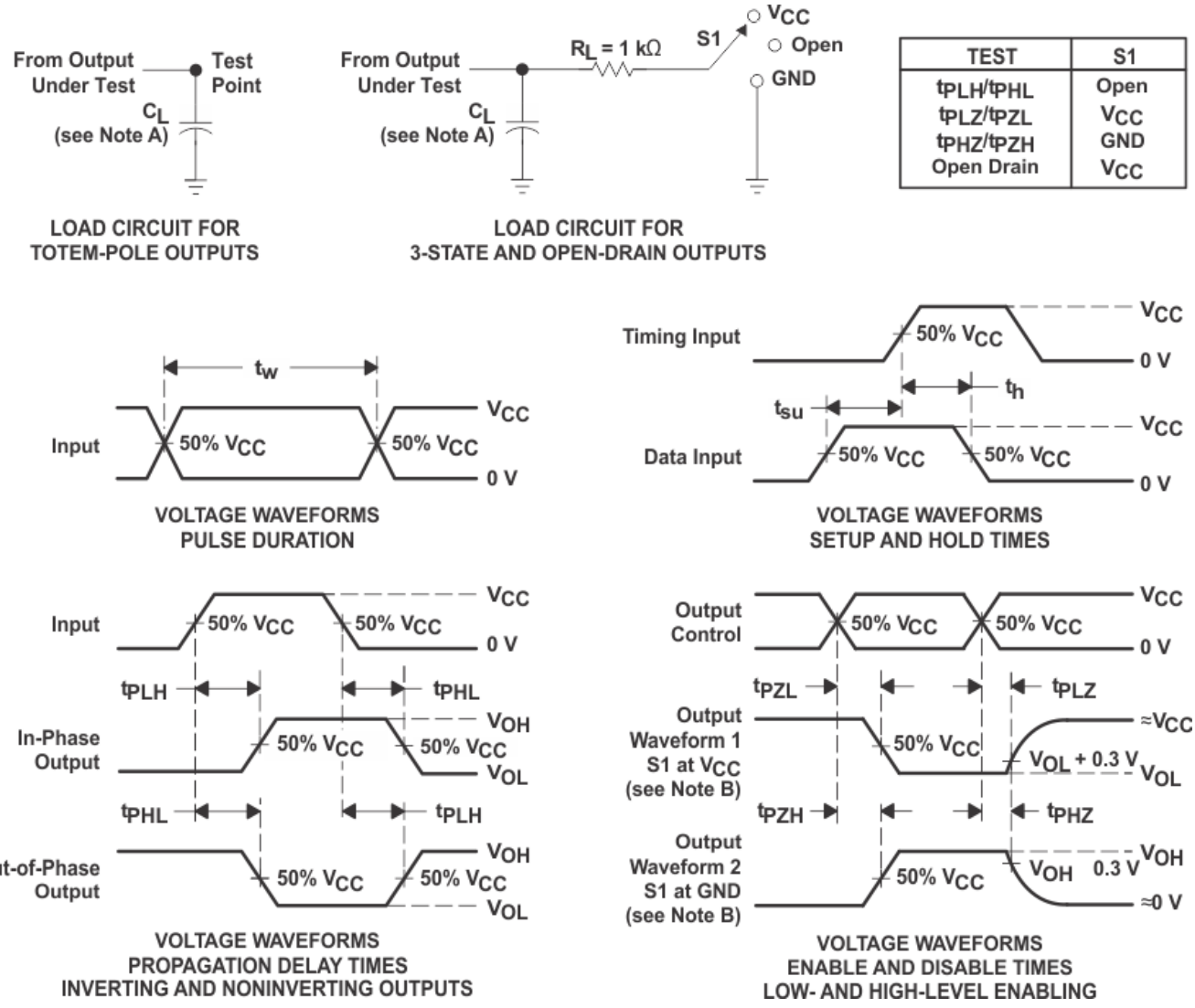
(1) Characteristics are for surface-mount packages only.

5.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	21	pF
			5 V	23	

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽ 3 ns, t_f ⩽ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and tPZH are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This dual positive-edge-triggered D-type flip-flop is designed for 2-V to 5.5-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

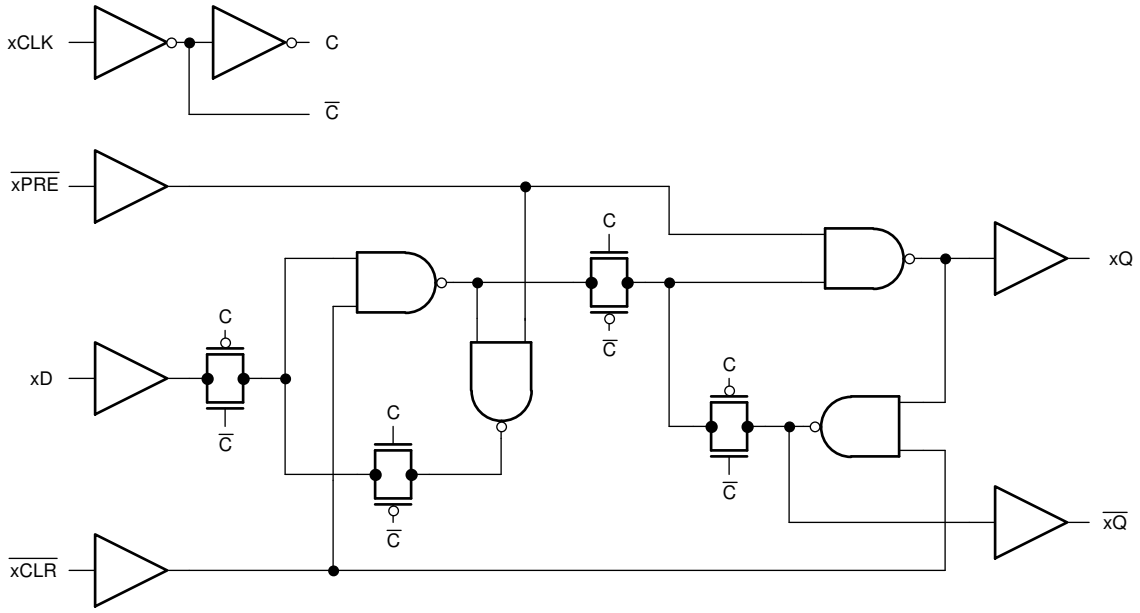


图 7-1. Logic Diagram, Each Flip-flop (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS(1)				OUTPUTS(2)	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(3)	H(3)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State
(3) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV74A-Q1	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV74AQDRG4Q1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A
SN74LV74AQDRG4Q1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A
SN74LV74AQDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A
SN74LV74AQDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A
SN74LV74AQPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A
SN74LV74AQPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV74A-Q1 :

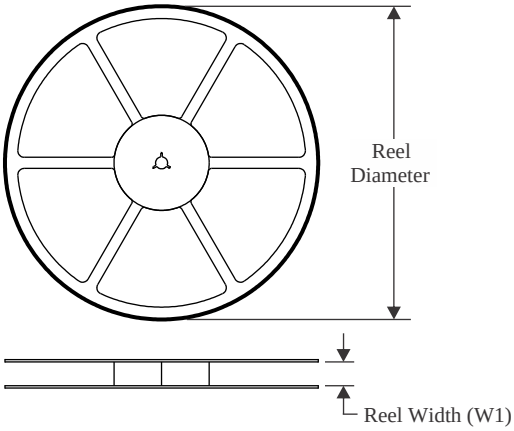
- Catalog : SN74LV74A
- Enhanced Product : SN74LV74A-EP

NOTE: Qualified Version Definitions:

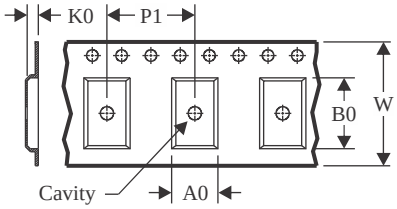
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

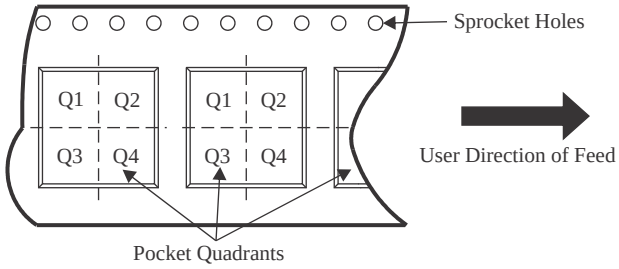


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

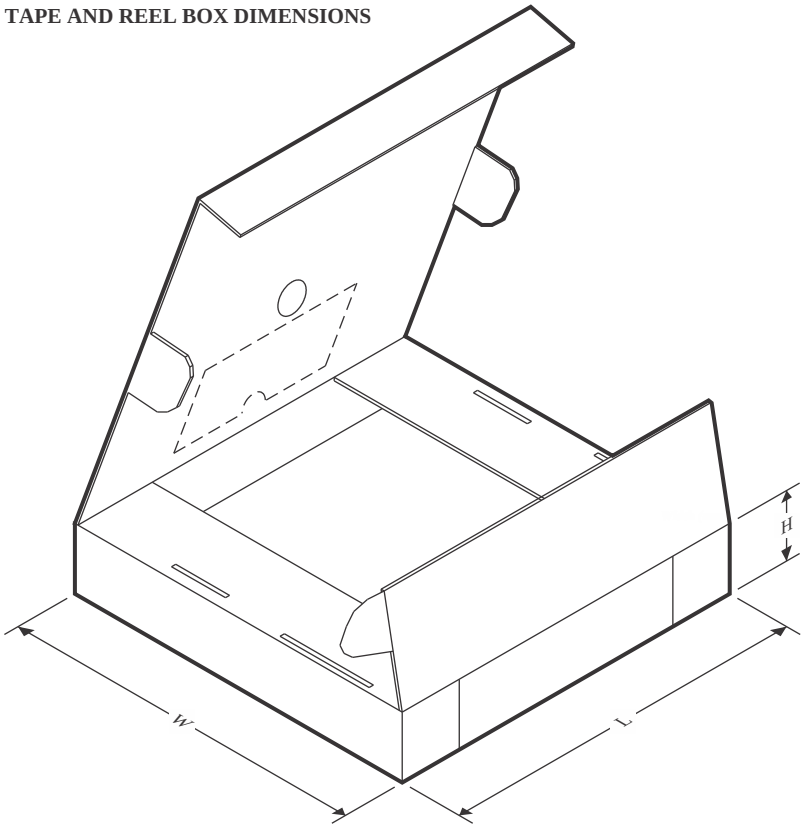
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

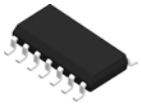
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0

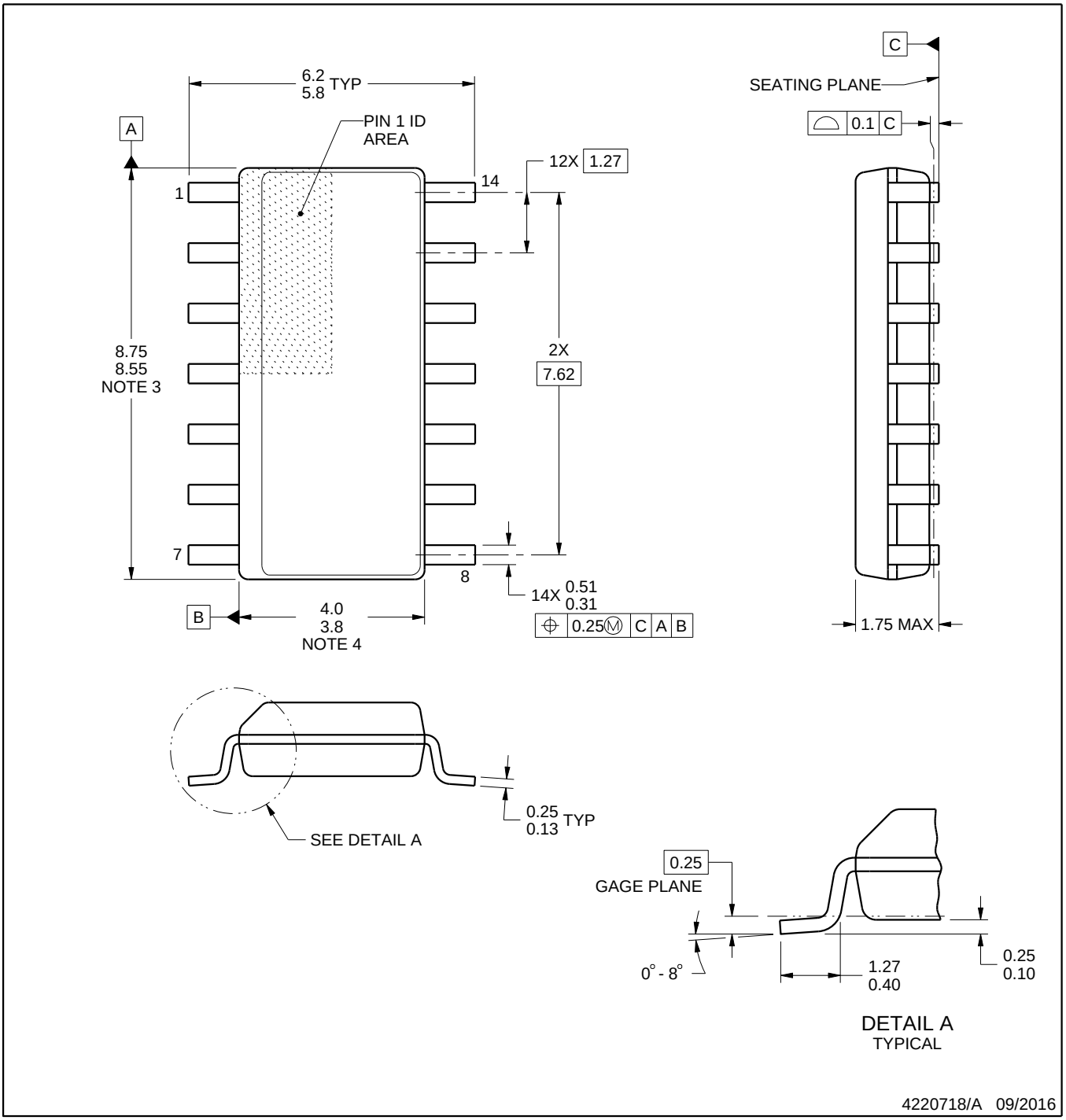


PACKAGE OUTLINE

D0014A

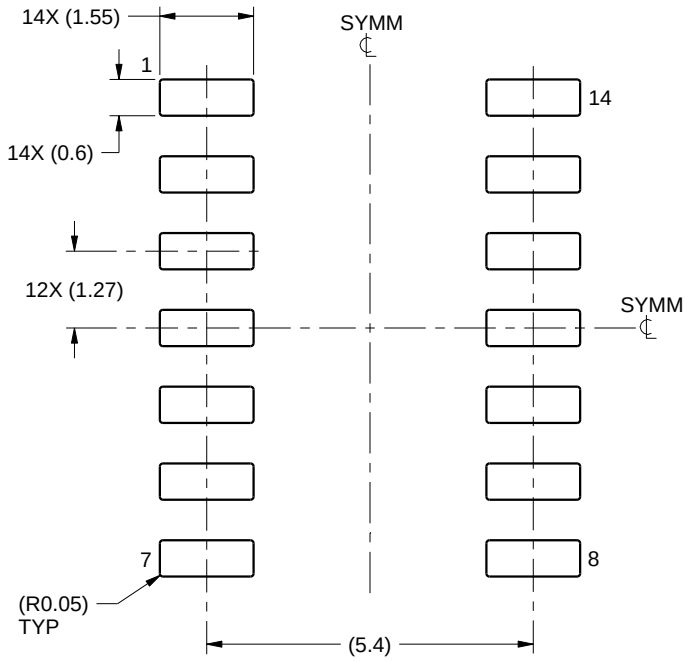
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

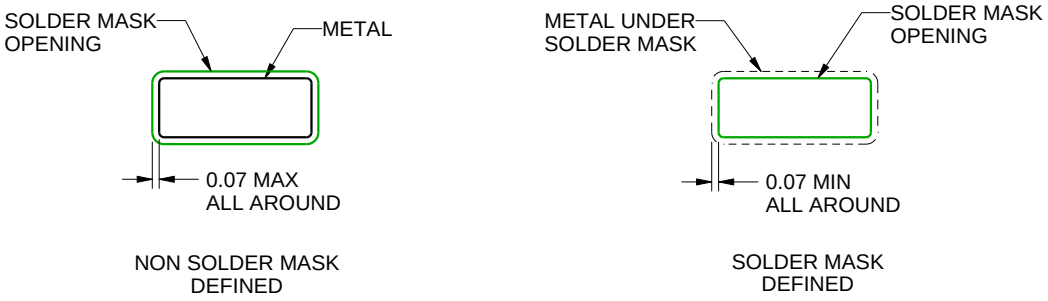


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

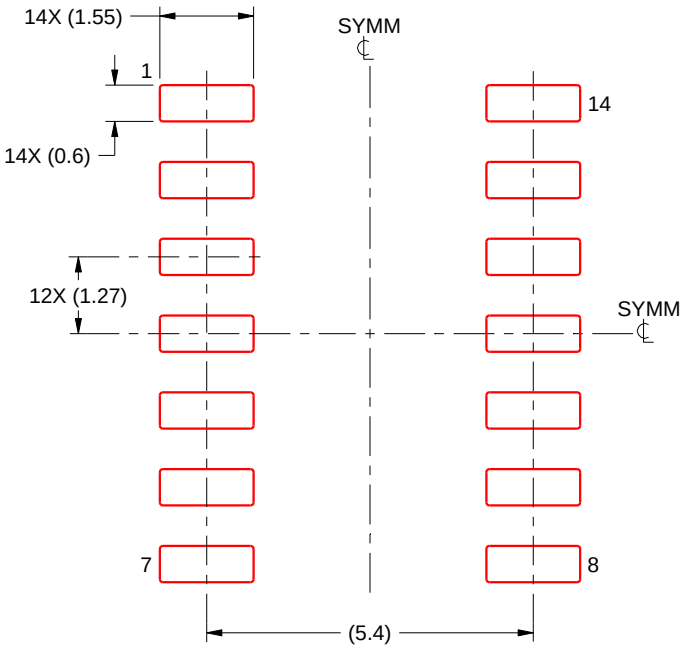
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

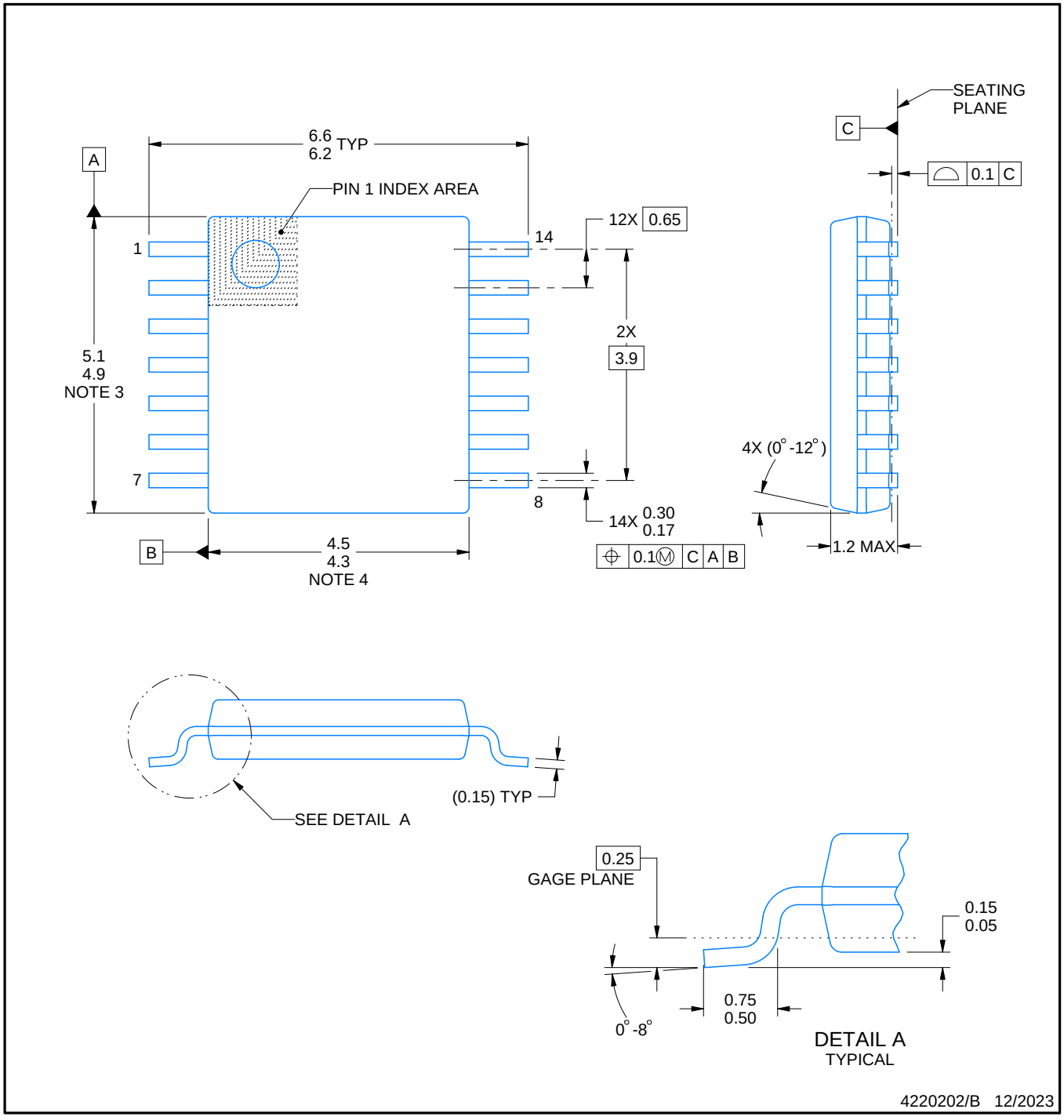
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

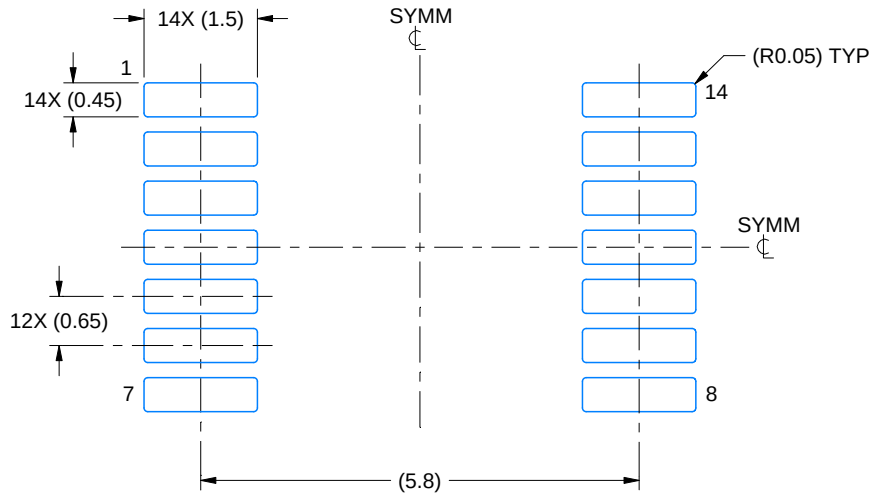
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

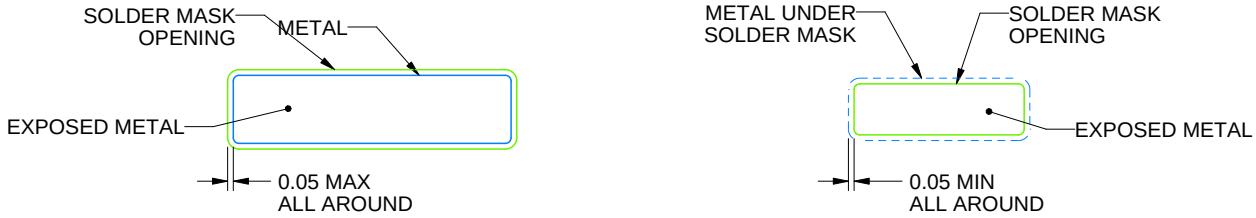


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

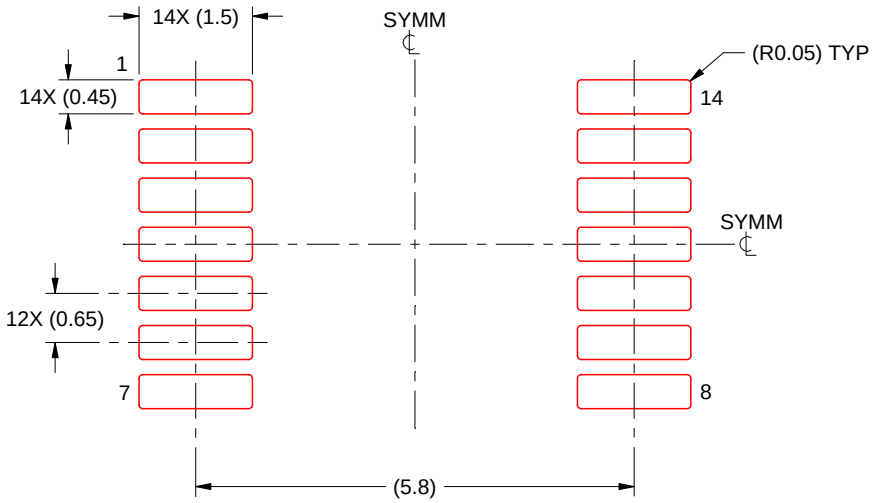


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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