具有三态输出的 SN74LV4T125-Q1 汽车类四路缓冲器转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：-40°C 至 +125°C
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 1.8V 至 5.5V 的宽工作电压范围
- 单电源电压转换器（参阅 *LVxT 增强输入电压*）：
  - 上行转换：
    - 1.2 V 至 1.8 V
    - 1.5 V 至 2.5 V
    - 1.8V 至 3.3V
    - 3.3 V 至 5.0 V
  - 下行转换：
    - 5.0V、3.3V、2.5V 至 1.8V
    - 5.0V、3.3V 至 2.5V
    - 5.0 V 至 3.3 V
- 5.5V 容限输入引脚
- 支持标准引脚排列
- 速率高达 150 Mbps，具有 5V 或 3.3V V_{CC}
- 闩锁性能超过 250 mA，符合 JESD 17 规范

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

3 说明

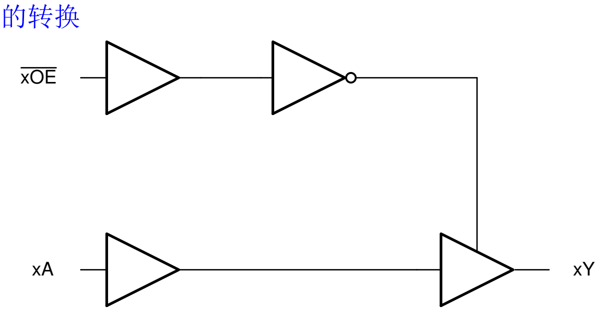
SN74LV4T125-Q1 包含四个具有三态输出的独立缓冲器且支持扩展电压运行，可实现电平转换。每个缓冲器以正逻辑执行布尔函数 Y = A。通过对 $\overline{OE}$ 引脚施加高电平，可以将输出置于高阻态 (Hi-Z)。输出电平以电源电压 (V_{CC}) 为基准，并且支持 1.8V、2.5V、3.3V 和 5V CMOS 电平。

该输入经设计，具有较低阈值电路，支持较低电压 CMOS 输入的上行转换（例如 1.2V 输入转换为 1.8V 输出或 1.8V 输入转换为 3.3V 输出）。此外，5V 容限输入引脚可实现下行转换（例如 3.3V 至 2.5V 输出）。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
SN74LV4T125-Q1	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化逻辑图（正逻辑）

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4 Revision History

Changes from Revision * (March 2022) to Revision A (June 2022)	**Page**
• 将数据表的状态从*预告信息* 更改为*量产数据*	1

5 Pin Configuration and Functions

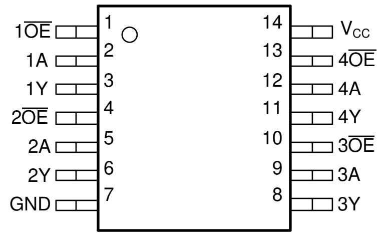


图 5-1. PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1$\overline{OE}$	1	I	Channel 1, output enable, active low
1A	2	I	Channel 1, input A
1Y	3	O	Channel 1, output Y
2$\overline{OE}$	4	I	Channel 2, output enable, active low
2A	5	I	Channel 2, input A
2Y	6	O	Channel 2, output Y
GND	7	G	Ground
3Y	8	I	Channel 3, output Y
3A	9	I	Channel 3, input A
3$\overline{OE}$	10	I	Channel 3, output enable, active low
4Y	11	O	Channel 4, output Y
4A	12	I	Channel 4, input A
4$\overline{OE}$	13	I	Channel 4, output enable, active low
V_{CC}	14	P	Positive supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state [2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the HIGH or LOW state [2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < –0.5 V		-20	mA
I_{OK}	Output clamp current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous output current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

PARAMETER		CONDITION	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	3-state (Hi-Z)	0	V_{CC}	V
		HIGH or LOW state	0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 2 V	1.1		V
		V_{CC} = 2.25 V to 2.75 V	1.28		
		V_{CC} = 3 V to 3.6 V	1.45		
		V_{CC} = 4.5 V to 5.5 V	2.00		
V_{IL}	Low-Level input voltage	V_{CC} = 1.65 V to 2 V		0.51	V
		V_{CC} = 2.25 V to 2.75 V		0.65	
		V_{CC} = 3 V to 3.6 V		0.75	
		V_{CC} = 4.5 V to 5.5 V		0.8	
I_O	Output Current	V_{CC} = 1.65 V to 2.0 V		±8	mA
		V_{CC} = 2.25 V to 2.75 V		±15	
		V_{CC} = 3.3 V to 5.0 V		±25	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.6 V to 5.0 V		20	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or FLoating CMOS Inputs.

6.4 Thermal Information

THERMAL METRIC[(1)]		SN74LV4T125-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.0	°C/W
Y_{JB}	Junction-to-board characterization parameter	93.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH}= – 50 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH}= – 2 mA	1.65 V	1.4	1.7[(1)]		1.35			
	I_{OH}= – 3 mA	2.3 V	2.05	2.4[(1)]		2			
	I_{OH}= – 5 mA	3 V	2.7	3.08[(1)]		2.6			
	I_{OH} = – 16 mA	4.5 V	3.7	4.65[(1)]		3.6			
V_{OL}	I_{OL}= 50 µA	1.65 V to 5.5 V			0.1			0.1	V
	I_{OL}= 2 mA	1.65 V		0.1[(1)]	0.2			0.3	
	I_{OL}= 3 mA	2.3 V		0.1[(1)]	0.2			0.3	
	I_{OL} = 5 mA	3 V		0.2[(1)]	0.35			0.4	
	I_{OL}= 16 mA	4.5 V		0.3[(1)]	0.55			0.55	
I_I	V_I = 0 V or V_{CC}	0 V to 5.5 V			±0.1			±1	µA
I_{CC}	V_I = 0 V or V_{CC}, I_O = 0; open on loading	1.8 V to 5.5 V			2			20	µA
ΔI_{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V_{CC}, I_O = 0	5.5 V			1.35			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V_{CC}, I_O = 0	1.8 V			10			10	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25			±2.5	µA
I_{OFF}	V_O or V_I = 0 V to 5.5 V	0 V			0.5			5	µA
C_I	V_I = V_{CC} or GND	3.3 V		1.6		1.6			pF
C_O	V_O = V_{CC} or GND	3.3 V		4.8		4.8			pF
C_{PD} [(2)] [(3)]	C_L = 50 pF, F = 10 Mhz	5 V		16					pF

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) P_D= V_{CC} ^{2}xF_Ix(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage.

6.6 Switching Characteristics 1.8-V V_{CC}

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF		9.1	13.1			20.2	nS
			C_L = 50 pF		12.6	17.9			25	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF		7.6	16.2			23.8	nS
			C_L = 50 pF		14.5	21			23.8	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF		8.6	15.2			17.9	nS
			C_L = 50 pF		12.1	18			22.6	
$t_{sk(o)}$			C_L = 50 pF						1	nS

6.7 Switching Characteristics 2.5-V V_{CC}

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF		6.9	9.9			15.3	nS
			C_L = 50 pF		9.6	13.5			19	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF		5.8	12.3			18.1	nS
			C_L = 50 pF		11	15.9			18.1	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF		6.5	9.2			13.5	nS
			C_L = 50 pF		9.2	12.8			17.1	
$t_{sk(o)}$			C_L = 50 pF						1	nS

6.8 Switching Characteristics 3.3-V V_{CC}

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF		5.5	7.9			12.2	nS
			C_L = 50 pF		7.6	10.8			15.1	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF		4.6	9.8			14.4	nS
			C_L = 50 pF		8.8	12.7			14.4	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.3			10.8	nS
			C_L = 50 pF		7.3	10.2			13.7	
$t_{sk(o)}$			C_L = 50 pF						1	nS

6.9 Switching Characteristics 5.0-V V_{CC}

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF		3.8	5.5			8.5	nS
			C_L = 50 pF		5.3	7.5			10.5	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF		3.2	6.8			10	nS
			C_L = 50 pF		6.1	8.8			10	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1			7.5	nS
			C_L = 50 pF		5.1	7.1			9.5	
$t_{sk(o)}$			C_L = 50 pF						1	nS

6.10 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C [(1)]

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only

6.11 Typical Characteristics

T_A = 25°C (unless otherwise noted)

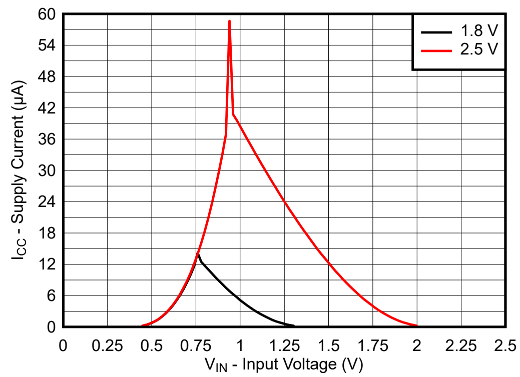


图 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

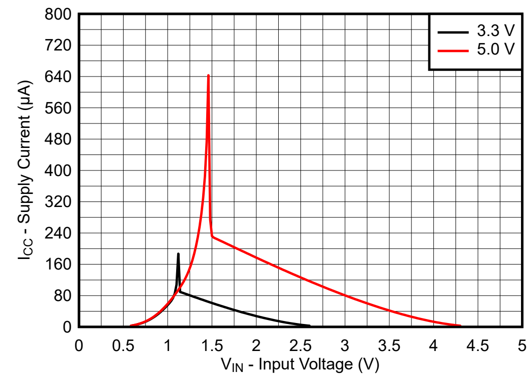


图 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

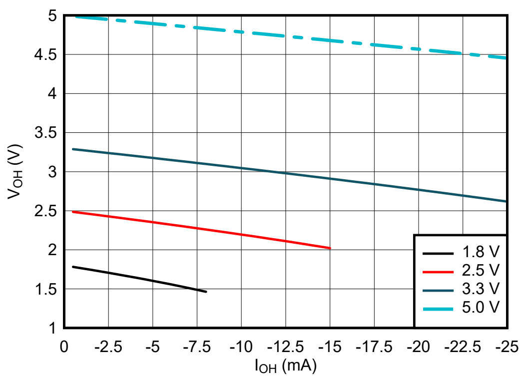


图 6-3. Output Voltage vs Current in HIGH State

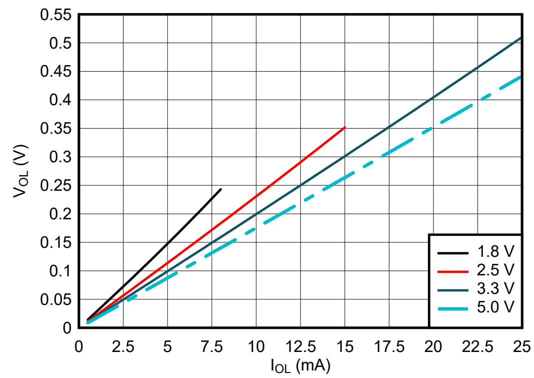


图 6-4. Output Voltage vs Current in LOW State

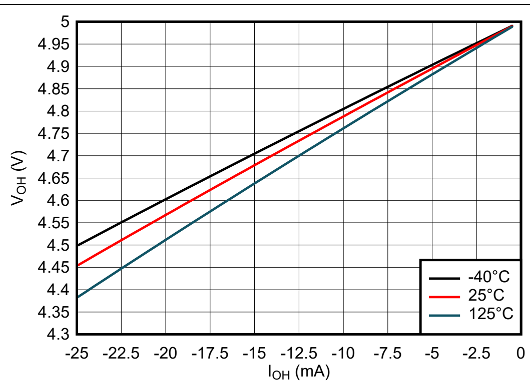


图 6-5. Output Voltage vs Current in HIGH State; 5-V Supply

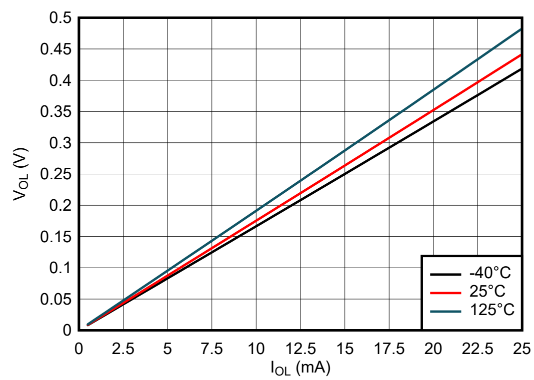


图 6-6. Output Voltage vs Current in LOW State; 5-V Supply

6.11 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

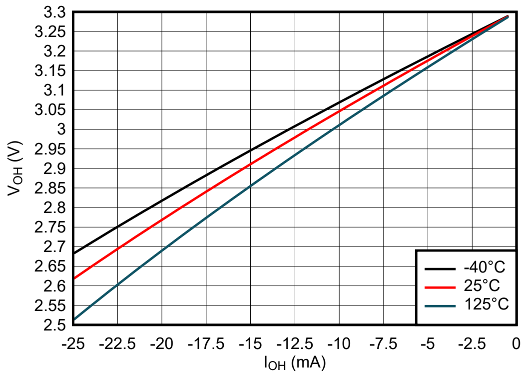


图 6-7. Output Voltage vs Current in HIGH State; 3.3-V Supply

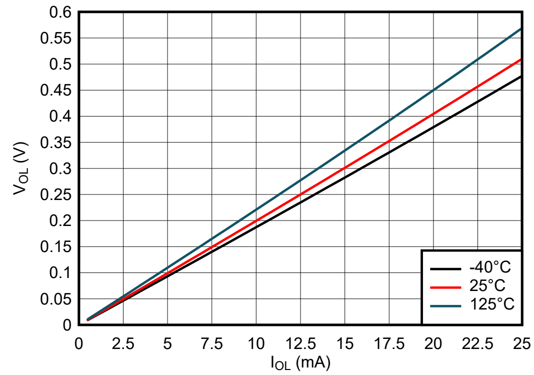


图 6-8. Output Voltage vs Current in LOW State; 3.3-V Supply

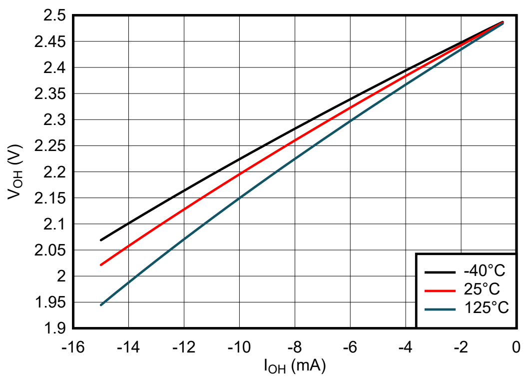


图 6-9. Output Voltage vs Current in HIGH State; 2.5-V Supply

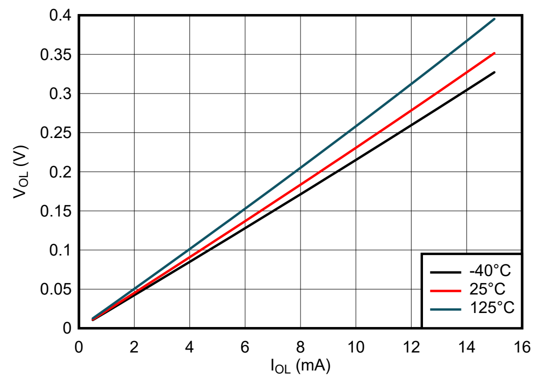


图 6-10. Output Voltage vs Current in LOW State; 2.5-V Supply

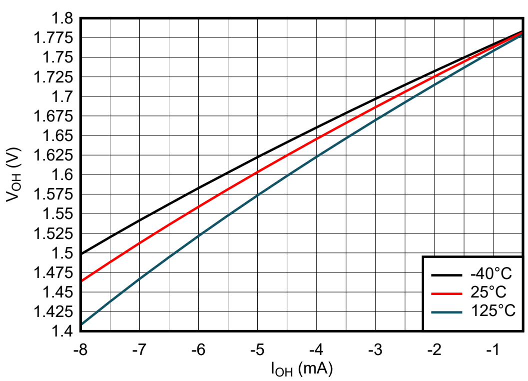


图 6-11. Output Voltage vs Current in HIGH State; 1.8-V Supply

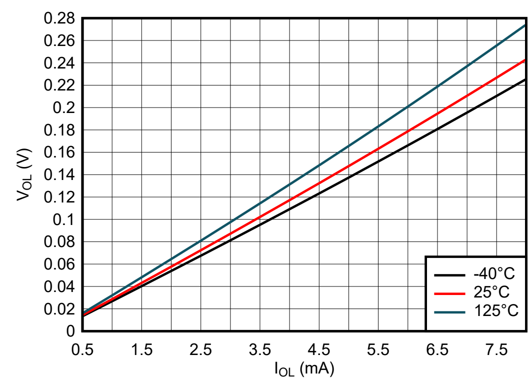


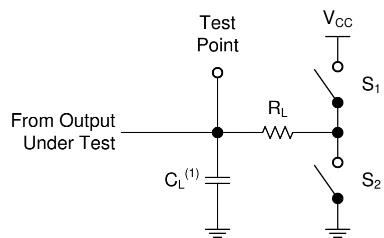
图 6-12. Output Voltage vs Current in LOW State; 1.8-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω.

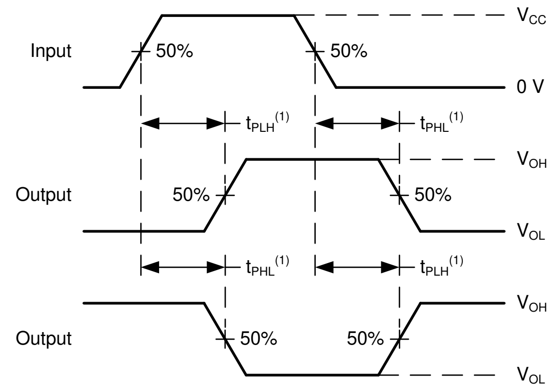
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



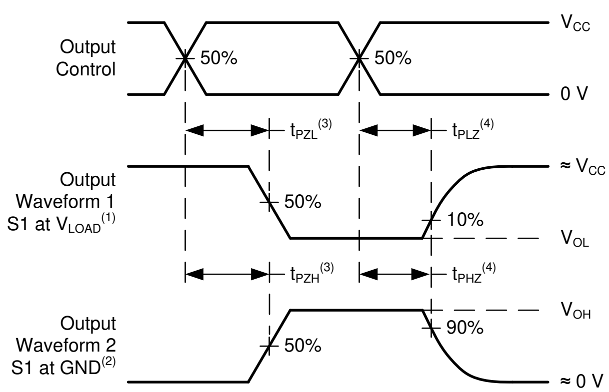
(1) C_L includes probe and test-fixture capacitance.

图 7-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 7-2. Voltage Waveforms Propagation Delays



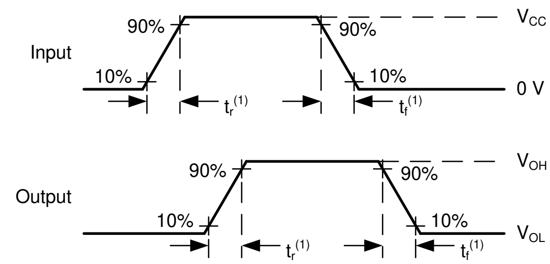
(1) S1 = CLOSED, S2 = OPEN.

(2) S1 = OPEN, S2 = CLOSED.

(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

图 7-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

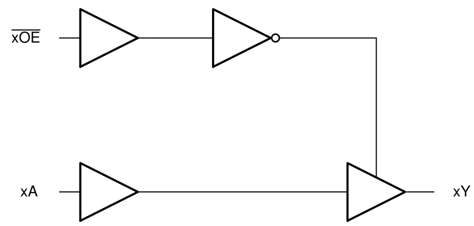
图 7-4. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

The SN74LV4T125-Q1 contains four independent buffers with 3-state outputs and extended voltage operation to allow for level translation. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a Hi-Z state by applying a High on the $\overline{OE}$ pin. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as depicted in 图 8-1.

> **CAUTION**
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

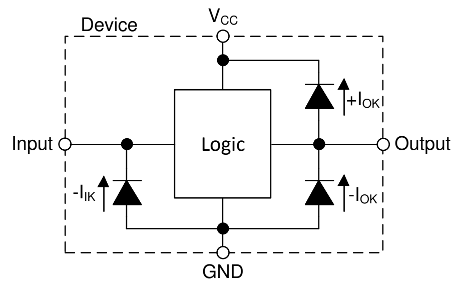


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.3 LVxT Enhanced Input Voltage

The SN74LV4T125-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. To ensure proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 图 8-2 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

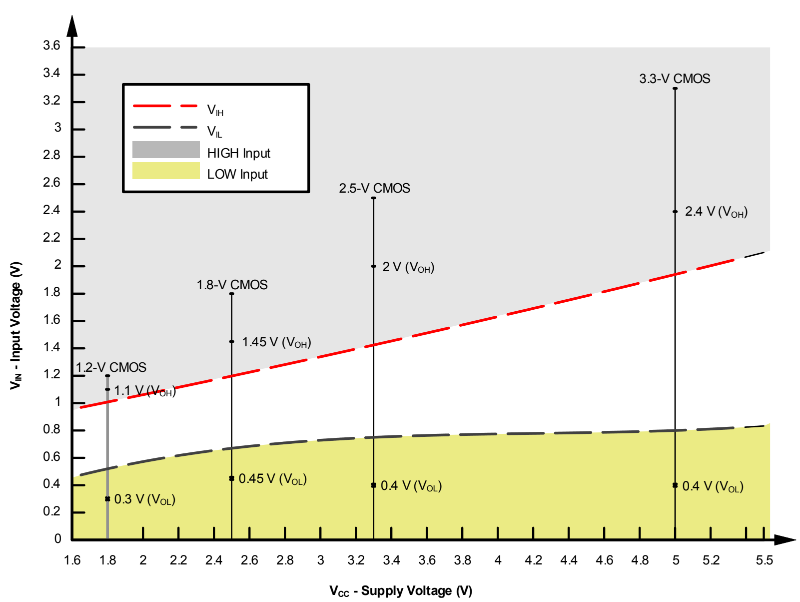


图 8-2. LVxT Input Voltage Levels

8.3.3.1 Down Translation

Signals can be translated down using the SN74LV4T125-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in 图 8-2.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC}. See 图 8-3.

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V V_{CC} – Inputs from 3.3 V and 5.0 V
- 3.3-V V_{CC} – Inputs from 5.0 V

8.3.3.2 Up Translation

Input signals can be up translated using the SN74LV4T125-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV4T125-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in 图 8-3.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2 V
- 2.5-V V_{CC} – Inputs from 1.8 V
- 3.3-V V_{CC} – Inputs from 1.8 V and 2.5 V
- 5.0-V V_{CC} – Inputs from 2.5 V and 3.3 V

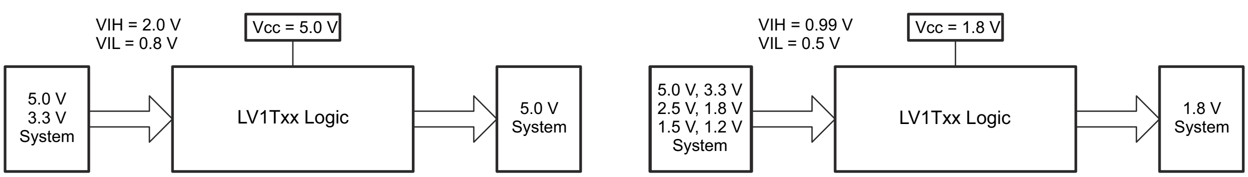


图 8-3. LVxT Up and Down Translation Example

8.4 Device Functional Modes

Function Table lists the functional modes of the SN74LV4T125-Q1.

表 8-1. Function Table

INPUTS(1)		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, a buffer with a 3-state output is used to disable a data signal as shown in 图 9-1. The remaining three buffers can be used for signal conditioning in other places in the system, or the inputs can be grounded and the channels left unused.

9.2 Typical Application

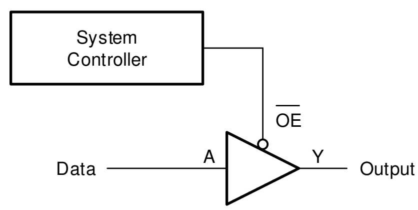


图 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV4T125-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV4T125-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV4T125-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV4T125-Q1 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV4T125-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV4T125-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Application Curves

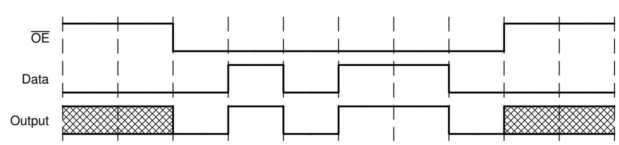


图 9-2. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

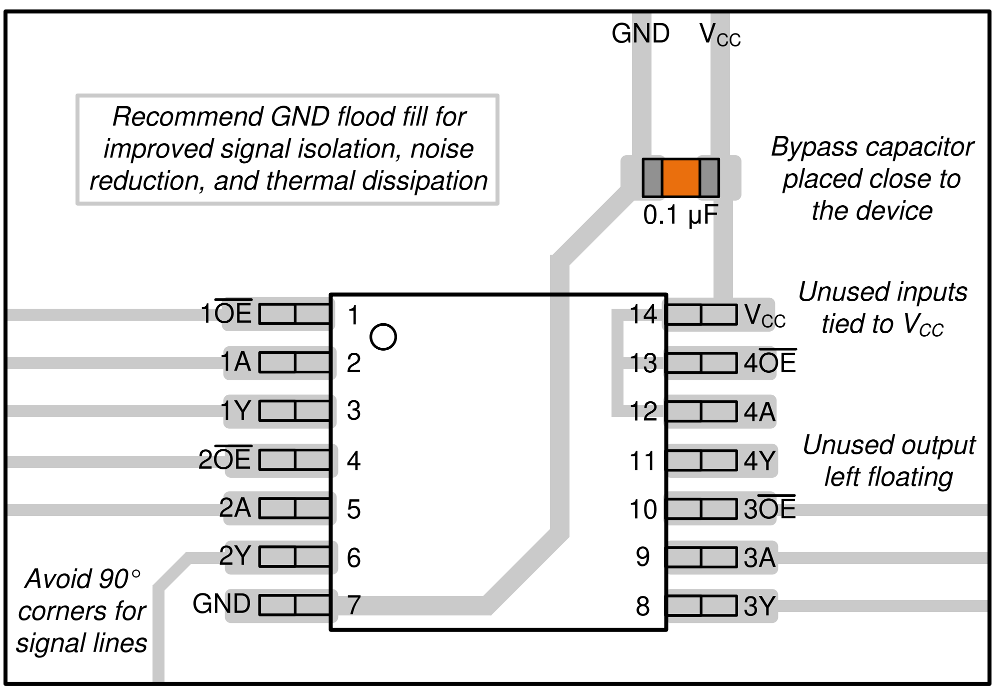


图 11-1. Example Layout for the SN74LV4T125-Q1

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *HCMOS Design Considerations* data sheet

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4T125QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4125Q
SN74LV4T125QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4125Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4T125-Q1 :

- Catalog : SN74LV4T125

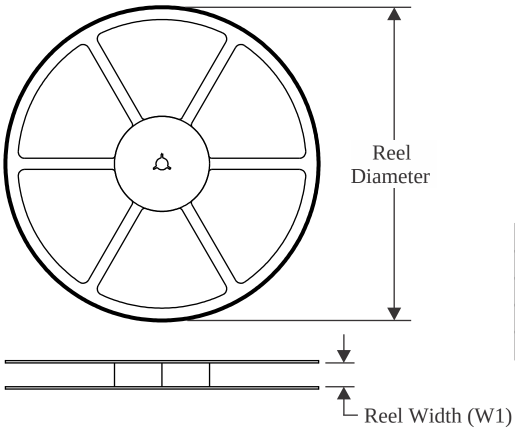
- Enhanced Product : SN74LV4T125-EP

NOTE: Qualified Version Definitions:

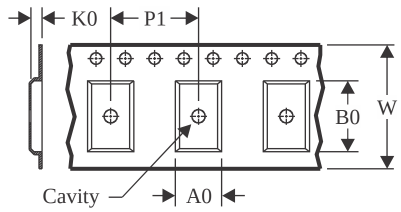
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

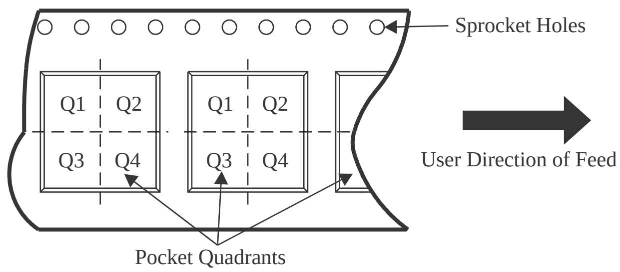


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

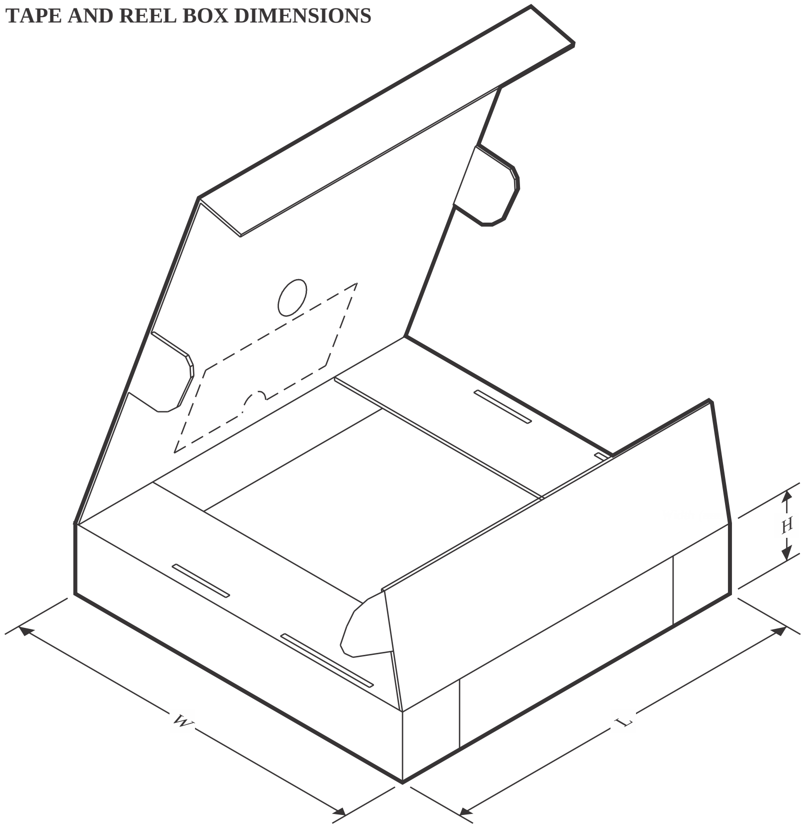
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

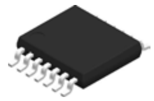
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4T125QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

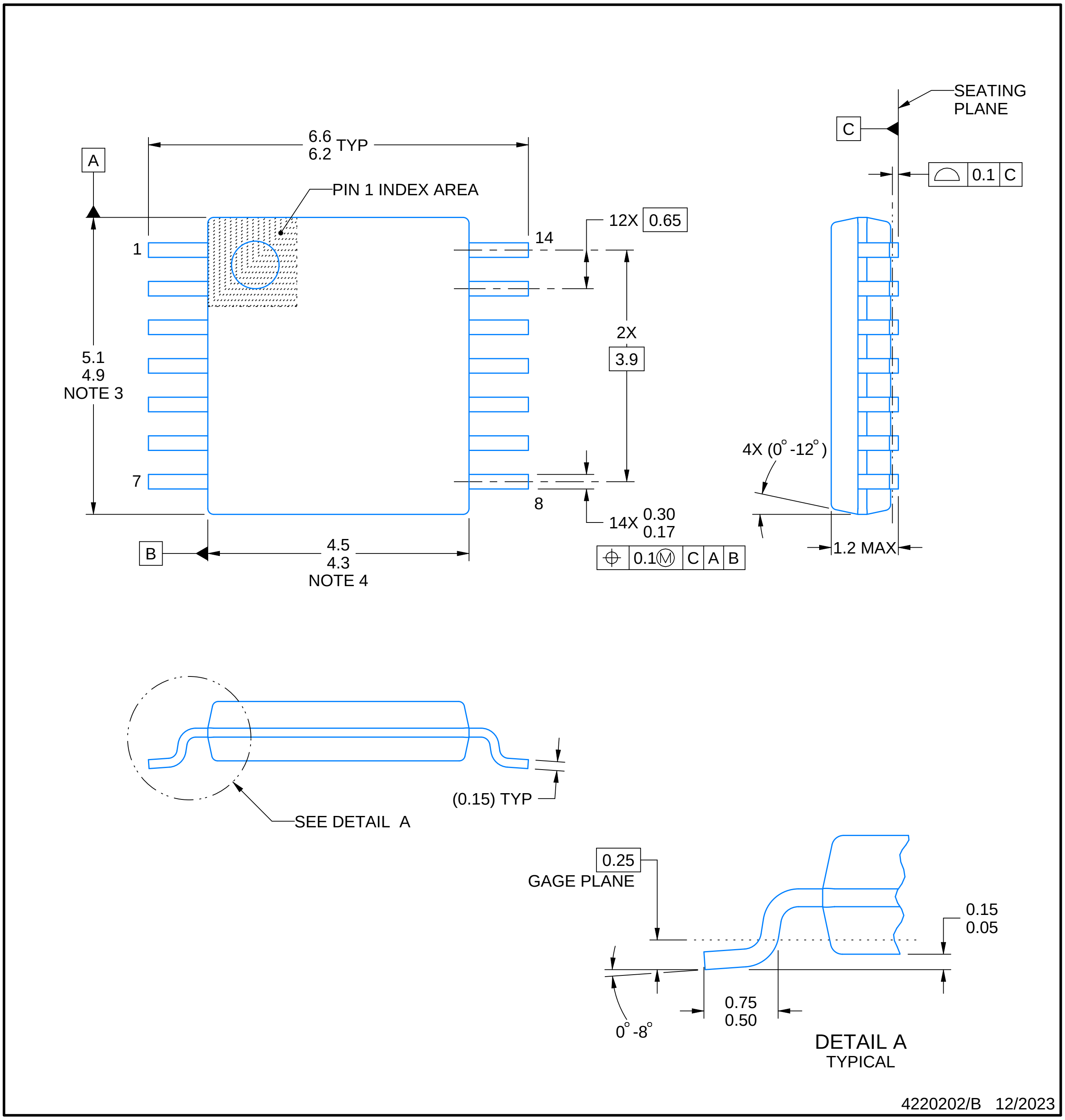
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4T125QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0



PACKAGE OUTLINE

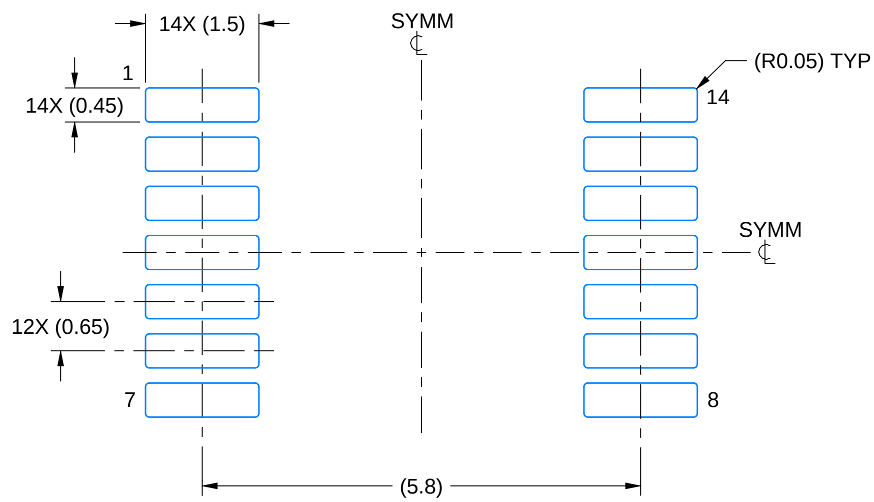
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

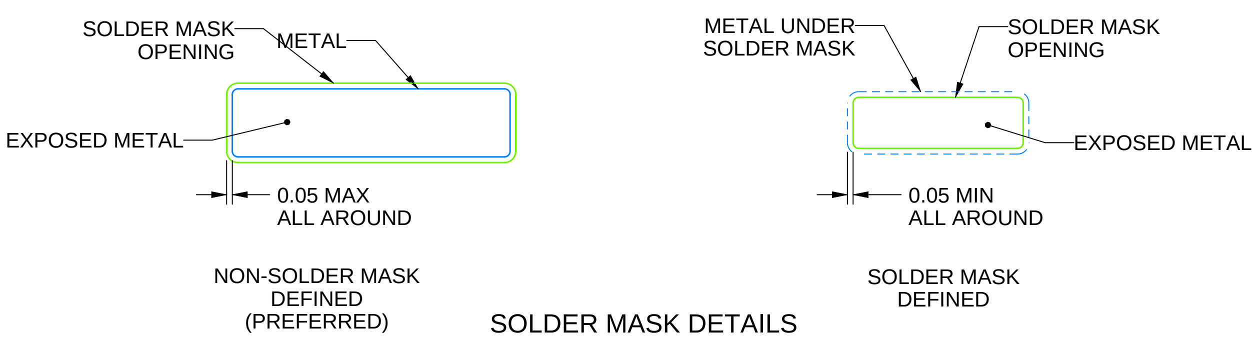


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

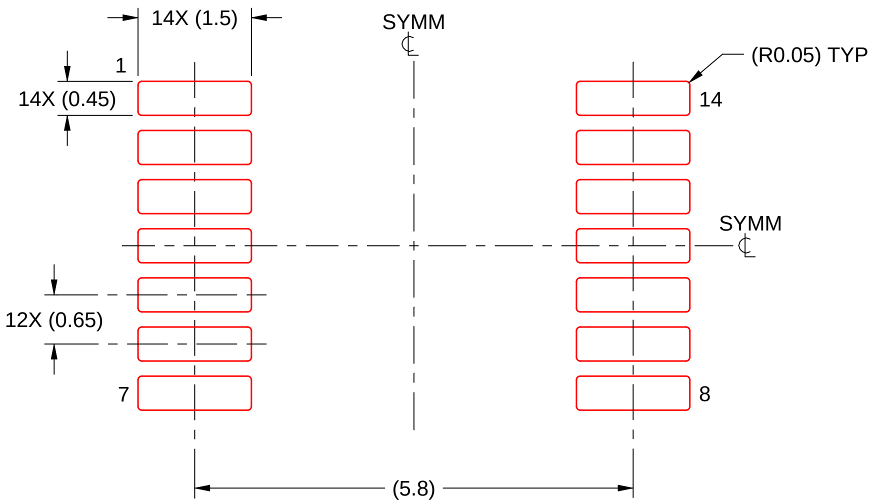


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265