SN74LV4066A 四路双边模拟开关

1 特性

- 1.65V 至 5.5V V_{CC} 运行
- 所有端口上均支持混合模式电压运行
- 高开关输出电压比
- 低开关间串扰
- 单独的开关控制
- 极低输入电流
- ESD 保护性能超过 JESD 22 规范要求：
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 750V 充电器件模型 (C101)

2 应用

- 电信
- 紧急呼叫
- 信息娱乐系统

3 说明

这款四路硅栅 CMOS 模拟开关可在 1.65V 至 5.5V V_{CC} 下运行。

这些开关能够处理模拟和数字信号。每个开关允许在任意方向传输振幅高达 5.5V（峰值）的信号。

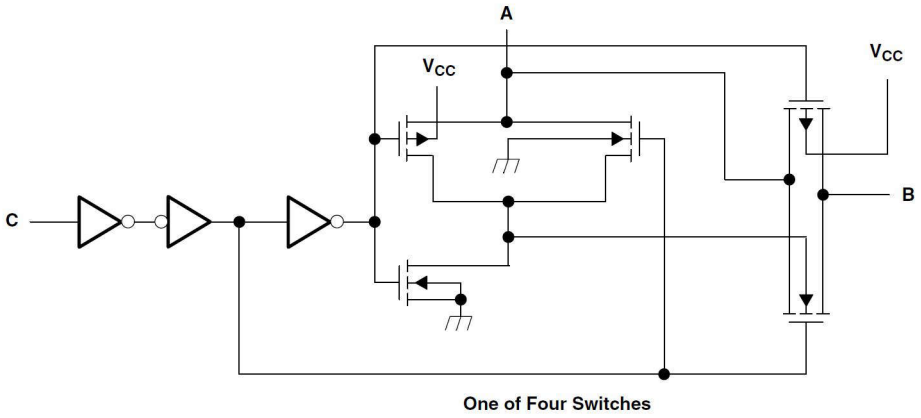
每个开关部分有其自己的输入使能控制 (C)。应用到 C 上的一个高电平电压开启相关开关部分。

应用包括用于模数和数模转换系统的信号选通、斩波、调制或者解调 (modem)，以及信号多路复用。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN74LV4066A	D（SOIC，14）	8.65mm x 6mm
	PW（TSSOP，14）	5mm × 6.4mm
	RGY（QFN，14）	3.5mm × 3.5mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

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4 Pin Configuration and Functions

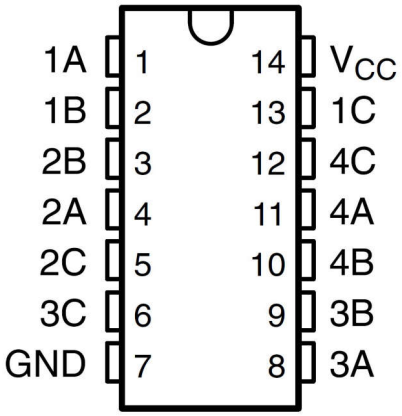


图 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

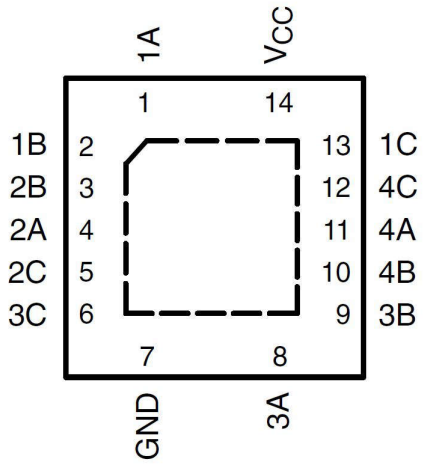


图 4-2. RGY Package, 14- Pin QFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I/O	Input/Output to switch channel 1
1B	2	I/O	Input/Output to switch channel 1
2B	3	I/O	Input/Output to switch channel 2
2A	4	I/O	Input/Output to switch channel 2
2C	5	I	Control line for channel 2. Switch is ON when control pin is high.
3C	6	I	Control line for channel 3. Switch is ON when control pin is high.
GND	7	—	Ground (0V) reference
3A	8	I/O	Input/Output to switch channel 3
3B	9	I/O	Input/Output to switch channel 3
4B	10	I/O	Input/Output to switch channel 4
4A	11	I/O	Input/Output to switch channel 4
4C	12	I	Control line for channel 4. Switch is ON when control pin is high.
1C	13	I	Control line for channel 1. Switch is ON when control pin is high.
V_{CC}	14	—	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VDD and GND.
Thermal pad		—	It is recommended to tie the pad to GND for the best performance.

(1) Signal types: I = input, O = output, I/O = input or output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7.0	V
V_I	Logic input voltage range		– 0.5	7.0	V
V_{IO}	Switch I/O voltage range(2) (3)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Logic input clamp current	V_I < 0	– 20		mA
I_{IOK}	Switch path diode clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	– 50	50	mA
I_T	Switch continuous current	V_{IO} = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) This value is limited to 5.5V maximum

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information: SN74LV4066A

THERMAL METRIC(1)		SN74LV4066A			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.8	150.6	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.65		5.5	V
V_{IH}	High-level input voltage, logic control inputs	V_{CC} = 2V	1.5		5.5	V
		V_{CC} = 2.3V to 2.7V	V_{CC} x 0.7		5.5	
		V_{CC} = 3V to 3.6V	V_{CC} x 0.7		5.5	
		V_{CC} = 4.5V to 5.5V	V_{CC} x 0.7		5.5	
V_{IL}	Low-level input voltage, logic control inputs	V_{CC} = 2V	0		0.5	V
		V_{CC} = 2.3V to 2.7V	0		V_{CC} x 0.3	
		V_{CC} = 3V to 3.6V	0		V_{CC} x 0.3	
		V_{CC} = 4.5V to 5.5V	0		V_{CC} x 0.3	
V_I	Logic control input voltage		0		5.5	V
V_{IO}	Switch input or output voltage		0		V_{CC}	V
$\Delta t/\Delta V$	Logic input transition rise or fall rate	V_{CC} = 2.3V to 2.7V			200	ns/V
		V_{CC} = 3V to 3.6V			100	
		V_{CC} = 4.5V to 5.5V			20	
T_A	Ambient temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.5 Electrical Characteristics (LV)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
r_{ON}	ON-state switch resistance	I_T = 2mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see 图 6-1)	25°C	1.65V		60	150	Ω
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	2.3V		38	180	
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	3V		29	150	Ω
			–40°C to 85°C				190	
			–40°C to 125°C				190	
			25°C	4.5V		21	75	Ω
			–40°C to 85°C				100	
			–40°C to 125°C				100	

5.5 Electrical Characteristics (LV)（续）

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65V		130	600	Ω
			– 40°C to 85°C				700	
			– 40°C to 125°C				700	
			25°C	2.3V		143	500	
			– 40°C to 85°C				600	
			– 40°C to 125°C				600	
			25°C	3V		57	180	Ω
			– 40°C to 85°C				225	
			– 40°C to 125°C				225	
			25°C	4.5V		31	100	Ω
			– 40°C to 85°C				125	
			– 40°C to 125°C				125	
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65V		2.5		Ω
			– 40°C to 85°C			3		
			– 40°C to 125°C			3		
			25°C	2.3V		3	30	
			– 40°C to 85°C	2.3V			40	
			– 40°C to 125°C	2.3V			40	
			25°C	3V		3	20	Ω
			– 40°C to 85°C				30	
			– 40°C to 125°C				30	
			25°C	4.5V		2	15	Ω
			– 40°C to 85°C				20	
			– 40°C to 125°C				20	
I_{IH} I_{IL}	Control input current	V_I = 5.5V or GND	25°C	0 to 5.5V			0.1	μA
			– 40°C to 85°C				1	
			– 40°C to 125°C				1	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} (see 图 6-2)	25°C	5.5V			±0.1	μA
			– 40°C to 85°C				±1	
			– 40°C to 125°C				±1	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see 图 6-3)	25°C	5.5V			±0.1	μA
			– 40°C to 85°C				±1	
			– 40°C to 125°C				±1	
I_{CC}	Supply current	V_I = V_{CC} or GND V_{INH} = 0V	25°C	5.5V		0.01		μA
			– 40°C to 85°C				20	
			– 40°C to 125°C				20	
C_{IC}	Control input capacitance	f = 10MHz	25°C	3.3V		4		pF
C_{IS}	Switch terminal capacitance	f = 10MHz	25°C	3.3V		5.5		pF
$C_{OS(on)}$	Common terminal ON-capacitance	f = 10MHz	25°C	3.3V		5.5		pF

5.5 Electrical Characteristics (LV)（续）

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
C_F	Feedthrough capacitance	f = 10MHz	25°C	3.3V		0.5		pF
C_{PD}	Power dissipation capacitance	C_L = 50pF, f = 10MHz	25°C	3.3V		4.5		pF

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted)
V_{cc} = 2V ± 0.2V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15pF (see 图 6-4)	25°C		1.2	10	ns
					– 40°C to 85°C			16	
					– 40°C to 125°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		3.3	15	ns
					– 40°C to 85°C			20	
					– 40°C to 125°C			20	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		6	15	ns
					– 40°C to 85°C			23	
					– 40°C to 125°C			23	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50pF (see 图 6-4)	25°C		2.6	12	ns
					– 40°C to 85°C			18	
					– 40°C to 125°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		4.2	25	ns
					– 40°C to 85°C			32	
					– 40°C to 125°C			32	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		9.6	25	ns
					– 40°C to 85°C			32	
					– 40°C to 125°C			32	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)
V_{cc} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15pF (see 图 6-4)	25°C		0.8	6	ns
					– 40°C to 85°C			10	
					– 40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		2.3	11	ns
					– 40°C to 85°C			15	
					– 40°C to 125°C			15	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		4.5	11	ns
					– 40°C to 85°C			15	
					– 40°C to 125°C			15	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V（续）

over recommended operating free-air temperature range (unless otherwise noted)
V_{cc} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50pF (see 图 6-4)	25°C		1.5	9	ns
					– 40°C to 85°C			12	
					– 40°C to 125°C			12	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		8	18	ns
					– 40°C to 85°C			22	
					– 40°C to 125°C			22	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		7.2	18	ns
					– 40°C to 85°C			22	
					– 40°C to 125°C			22	

5.8 Timing Characteristics V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range (unless otherwise noted)
V_{cc} = 5V ± 0.5V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15pF (see 图 6-4)	25°C		0.6	4	ns
					– 40°C to 85°C			7	
					– 40°C to 125°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		3.5	8	ns
					– 40°C to 85°C			10	
					– 40°C to 125°C			11	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15pF (see 图 6-5)	25°C		4.4	8	ns
					– 40°C to 85°C			10	
					– 40°C to 125°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50pF (see 图 6-4)	25°C		0.8	6	ns
					– 40°C to 85°C			8	
					– 40°C to 125°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		7	13	ns
					– 40°C to 85°C			16	
					– 40°C to 125°C			16	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50pF (see 图 6-5)	25°C		6.2	13	ns
					– 40°C to 85°C			16	
					– 40°C to 125°C			16	

5.9 AC Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	4066	C_L = 50pF, R_L = 50 Ω, F_{in} = 1MHz (sine wave) (see 图 6-6)(1)	V_{CC} = 2.3V		60		MHz
					V_{CC} = 3V		75		
					V_{CC} = 4.5V		100		

5.9 AC Characteristics（续）

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Charge Injection (control input to signal output)	INH	COM or Yn	ALL	C_L = 50pF F_{in} = 1MHz (sine wave) (see 图 6-7)	V_{CC} = 2.3V		15		mV
					V_{CC} = 3V		20		
					V_{CC} = 4.5V		50		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	C_L = 50pF, R_L = 50 Ω, F_{in} = 1MHz (sine wave) (see 图 6-8(2)	V_{CC} = 2.3V		–40		dB
					V_{CC} = 3V		–40		
					V_{CC} = 4.5V		–40		
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	C_L = 50pF, R_L = 50 Ω, F_{in} = 1MHz (sine wave) (see 图 6-9(2)	V_{CC} = 2.3V		–45		dB
					V_{CC} = 3V		–45		
					V_{CC} = 4.5V		–45		
Sine-wave distortion	COM or Yn	Yn or COM	ALL	C_L = 50pF, R_L = 10k Ω, F_{in} = 1kHz (sine wave) (see 图 6-10)	V_I = $2V_{p-p}$ V_{CC} = 2.3V		0.1		%
					V_I = $2.5V_{p-p}$ V_{CC} = 3V		0.1		
					V_I = $4V_{p-p}$ V_{CC} = 4.5V		0.1		

6 Parameter Measurement Information

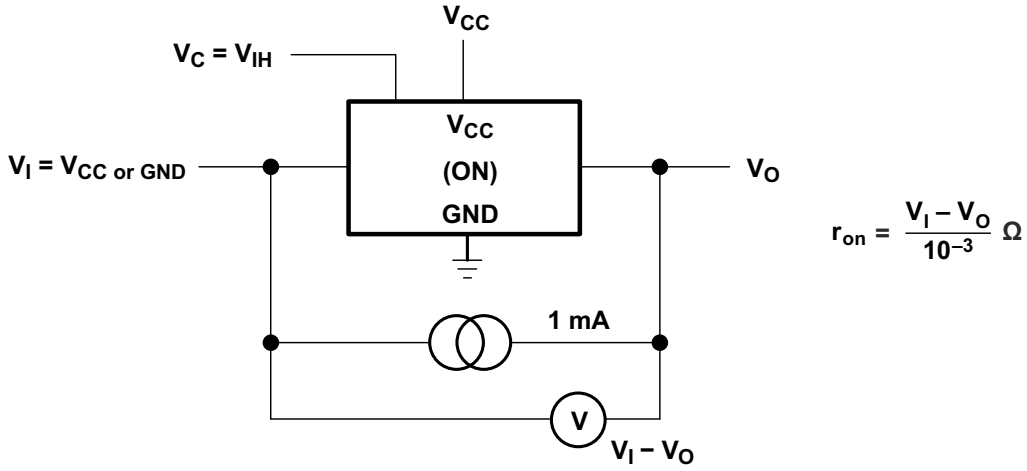
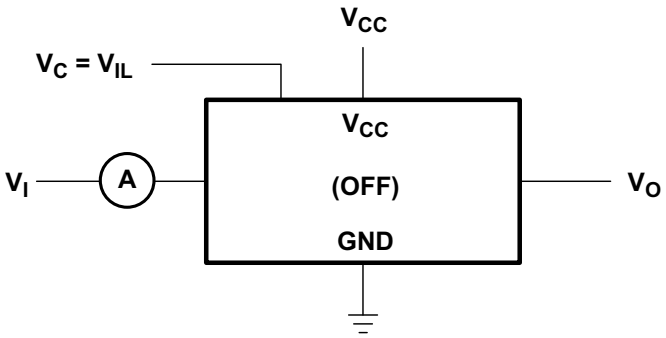
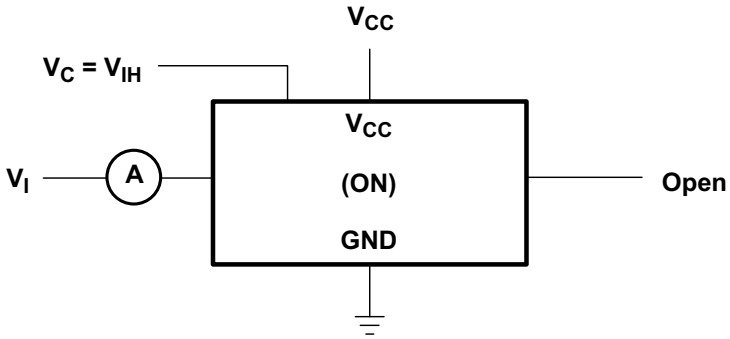


图 6-1. ON-State Resistance Test Circuit



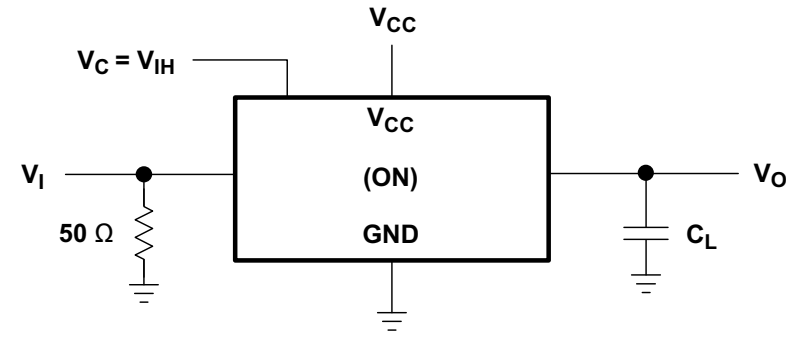
Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

图 6-2. OFF-State Switch Leakage-Current Test Circuit

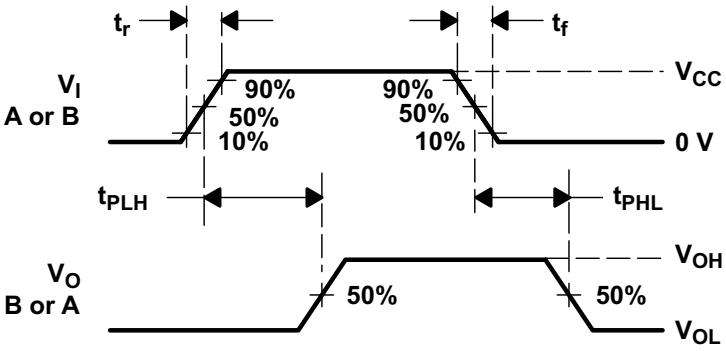


$V_I = V_{CC}$ or GND

图 6-3. ON-State Leakage-Current Test Circuit

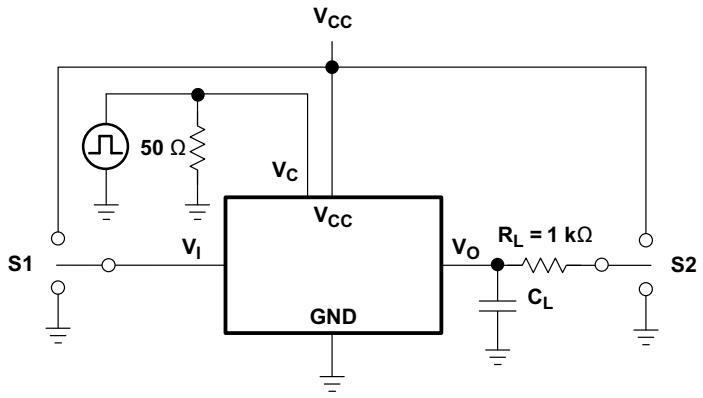


TEST CIRCUIT



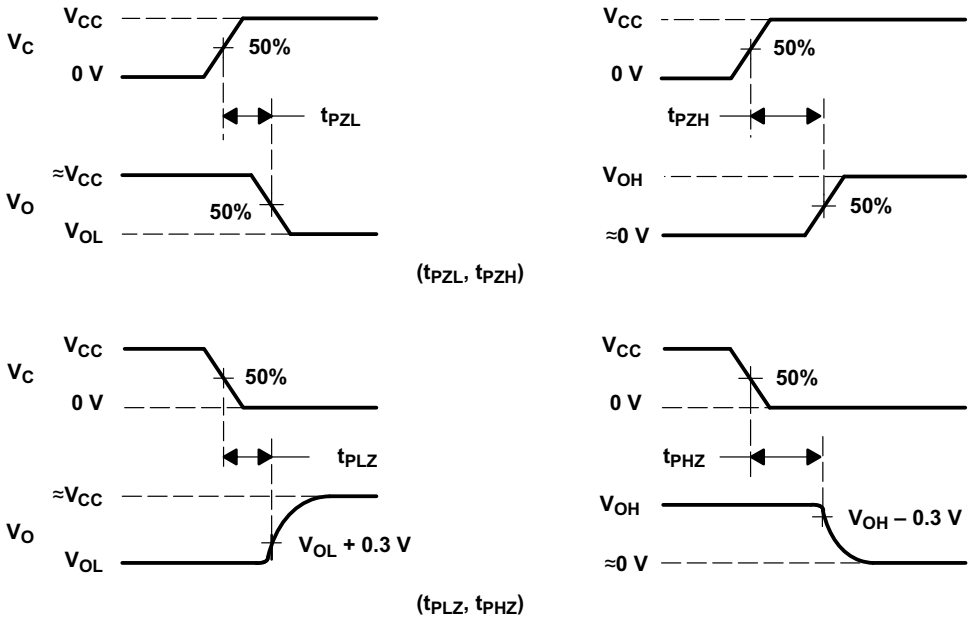
VOLTAGE WAVEFORMS

图 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

图 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

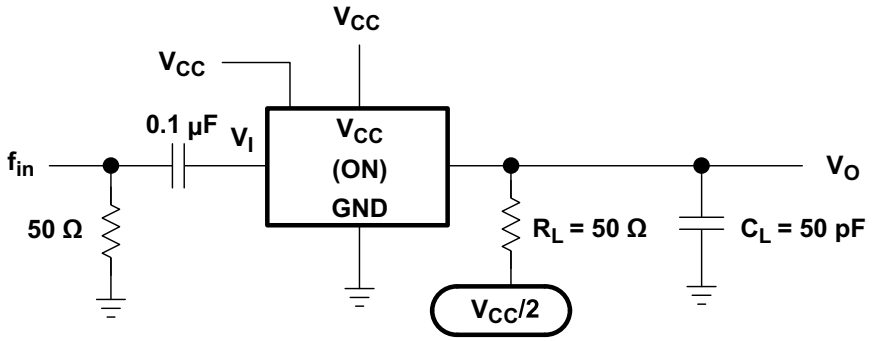


图 6-6. Frequency Response (Switch ON)

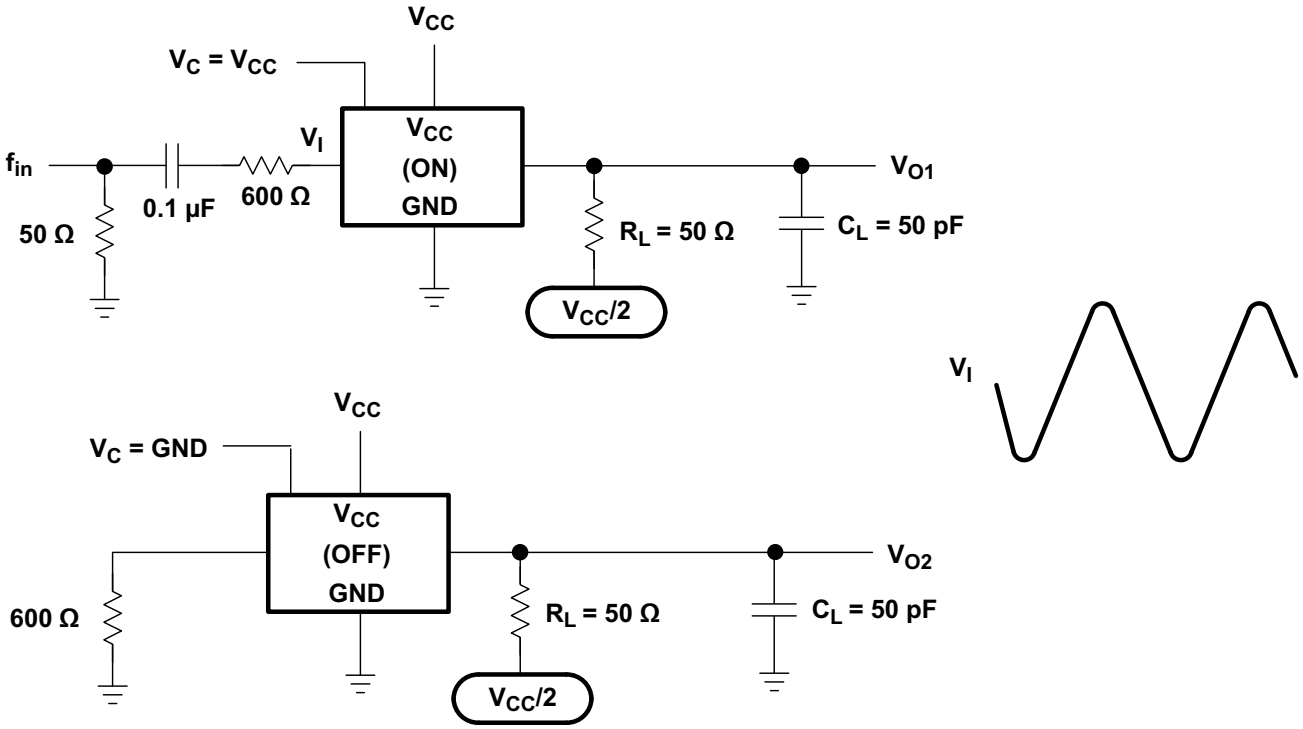


图 6-7. Crosstalk Between Any Two Switches

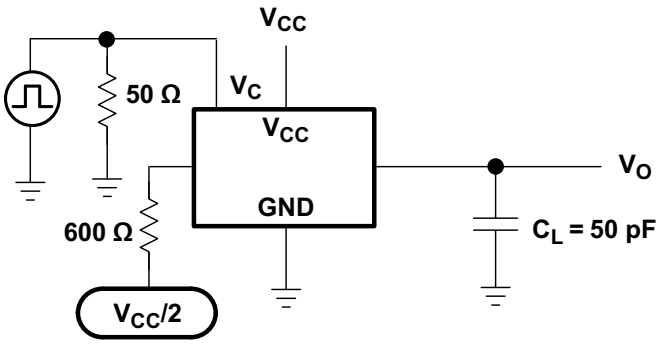


图 6-8. Crosstalk (Control Input − Switch Output)

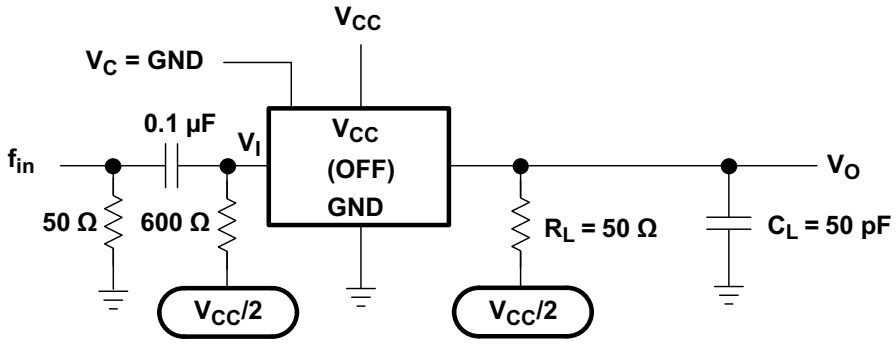


图 6-9. Feed-Through Attenuation (Switch OFF)

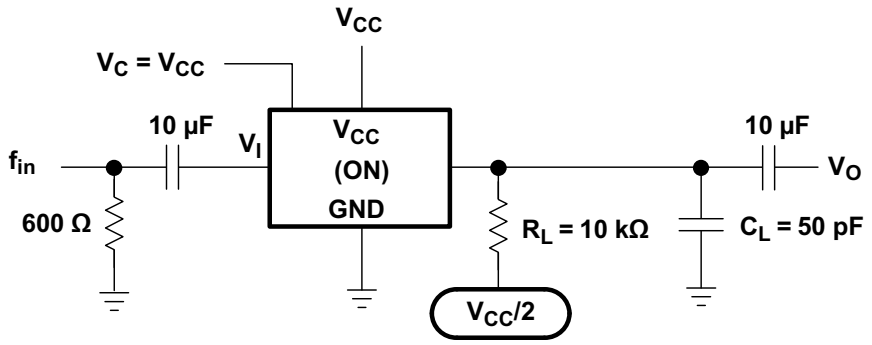


图 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Functional Block Diagram

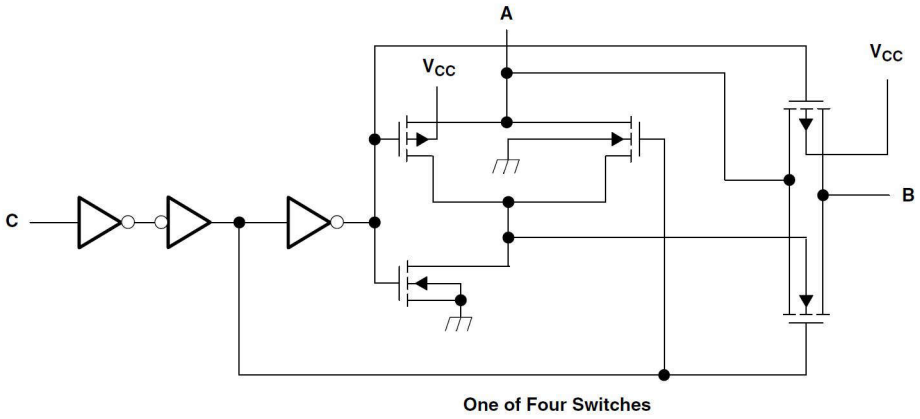


图 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table

Input Control (C)	Switch
L	OFF
H	ON

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (April 2006) to Revision J (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 删除了数据表中的 SN54LV4066A 信息	1
• 将 V_{CC} 工作电压从 *2V 至 5.5V* 扩展为 *1.65V 至 5.5V*，并相应地更新了 r_{ON}、$r_{ON(p)}$、Δr_{ON} 等规格	1
• Changed RL value from: *600 Ω* to: *50 Ω* for frequency response, crosstalk, and feed-through attenuation, and their associated figures	10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4066AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LV4066A
SN74LV4066ADBR	NRND	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADBR.A	NRND	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066ADGVR	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADGVR.A	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066AN	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4066AN
SN74LV4066AN.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LV4066AN
SN74LV4066ANSR	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4066A
SN74LV4066ANSR.A	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV4066A
SN74LV4066APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW066A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

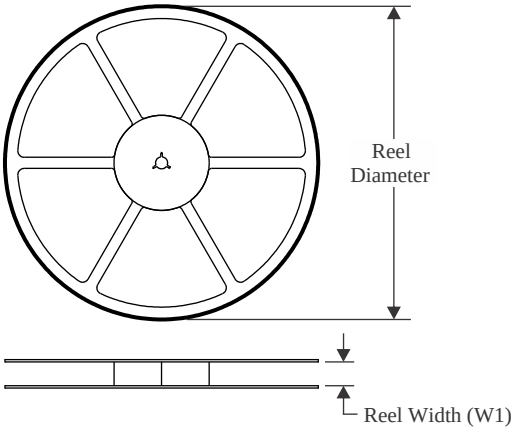
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

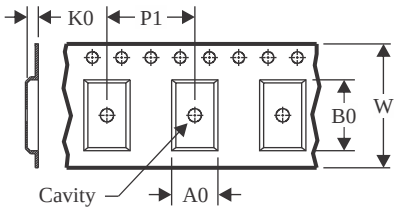
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

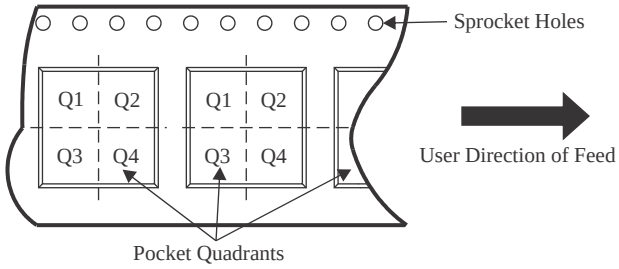


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

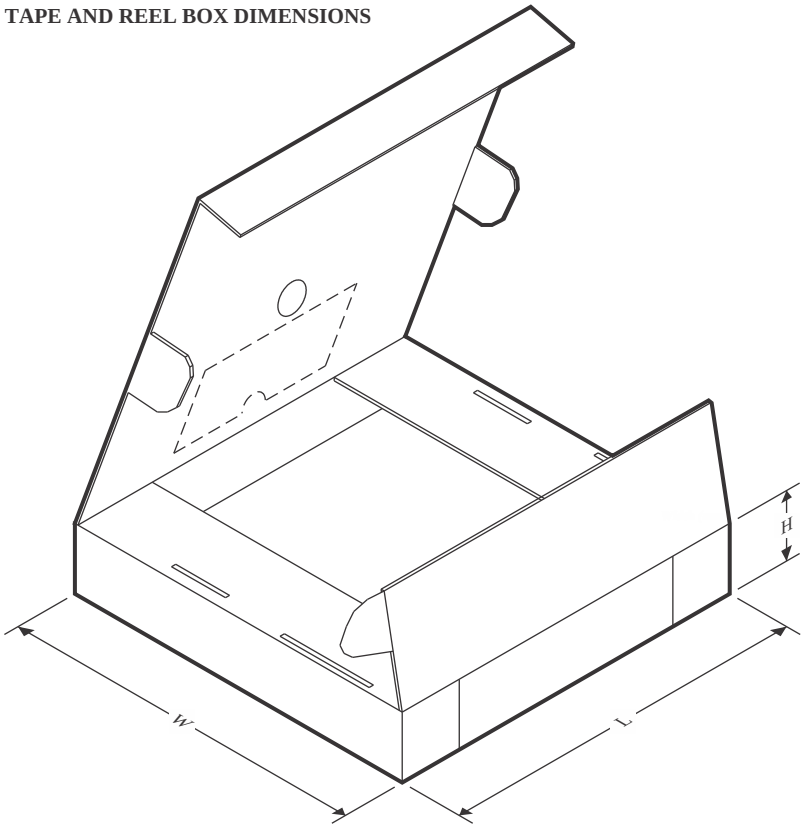
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4066ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4066ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4066ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV4066ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV4066ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV4066APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4066APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4066ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

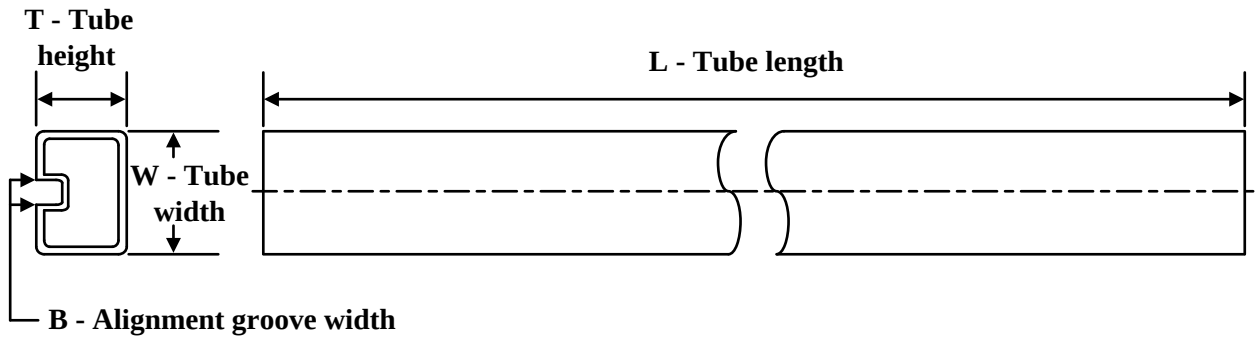
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

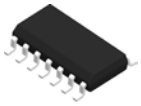
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4066ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV4066ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV4066ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV4066ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV4066ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LV4066APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV4066APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV4066ARGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32

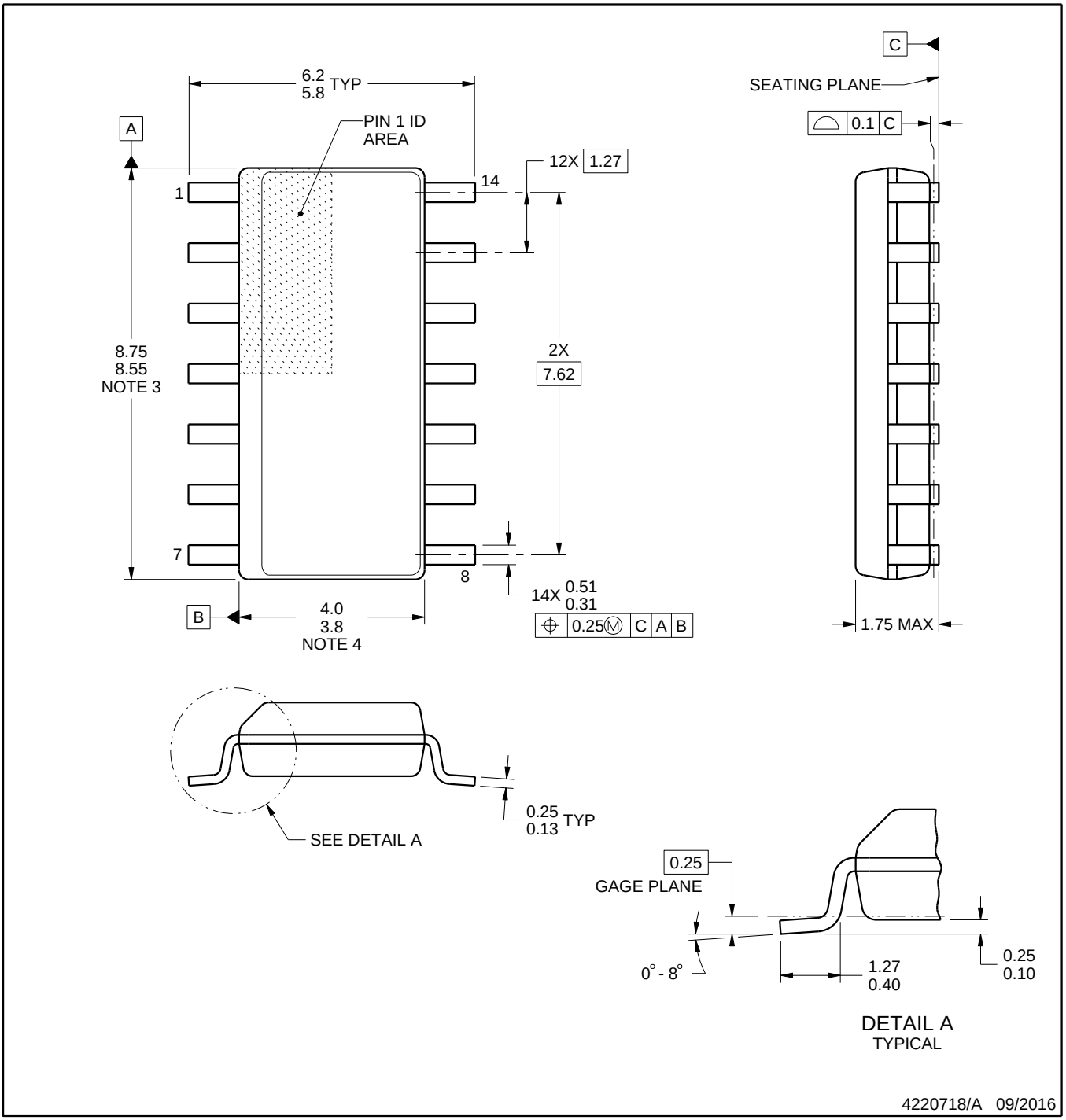


PACKAGE OUTLINE

D0014A

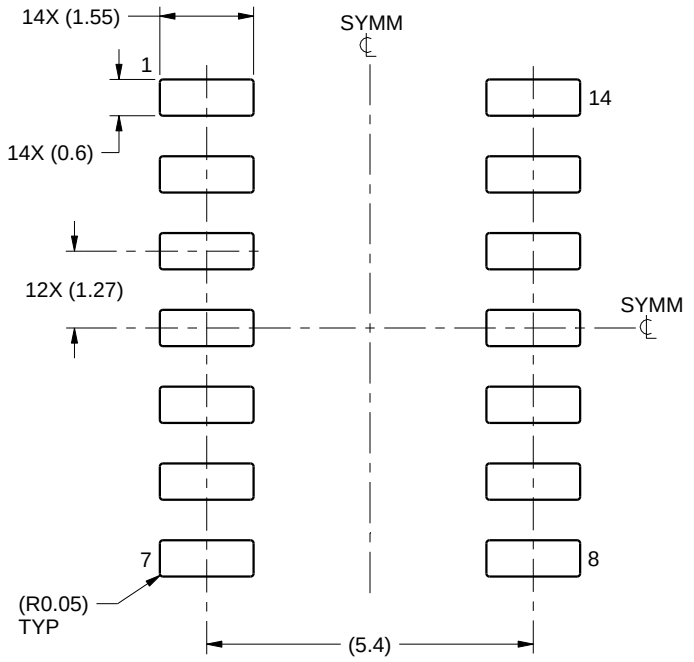
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

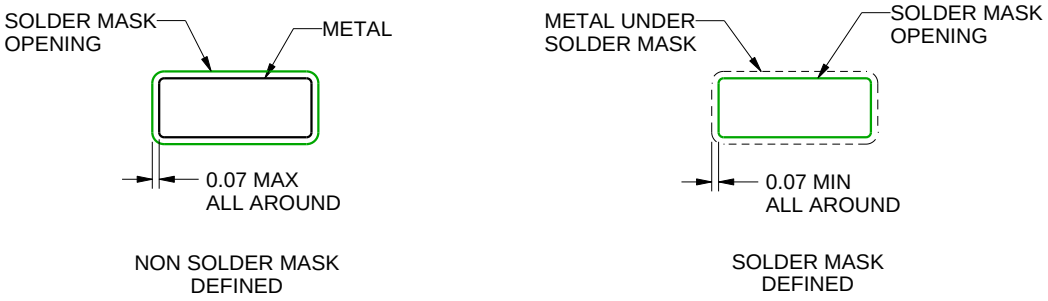


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

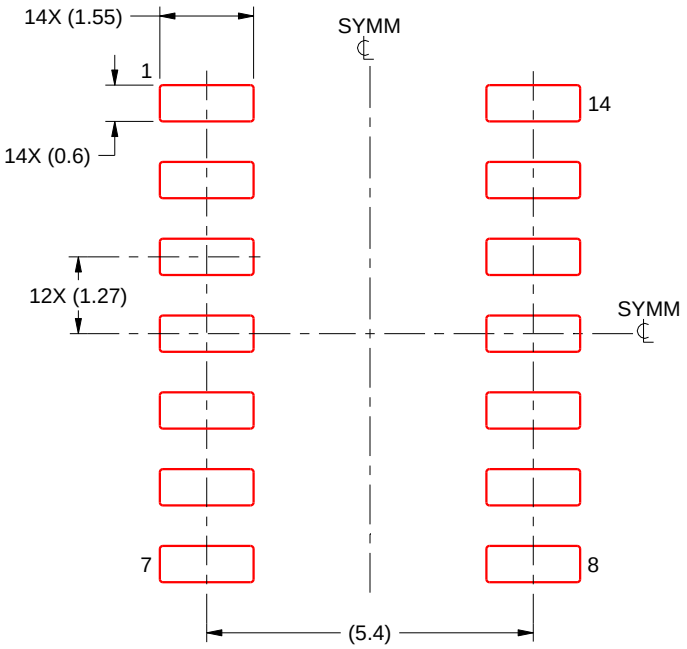
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

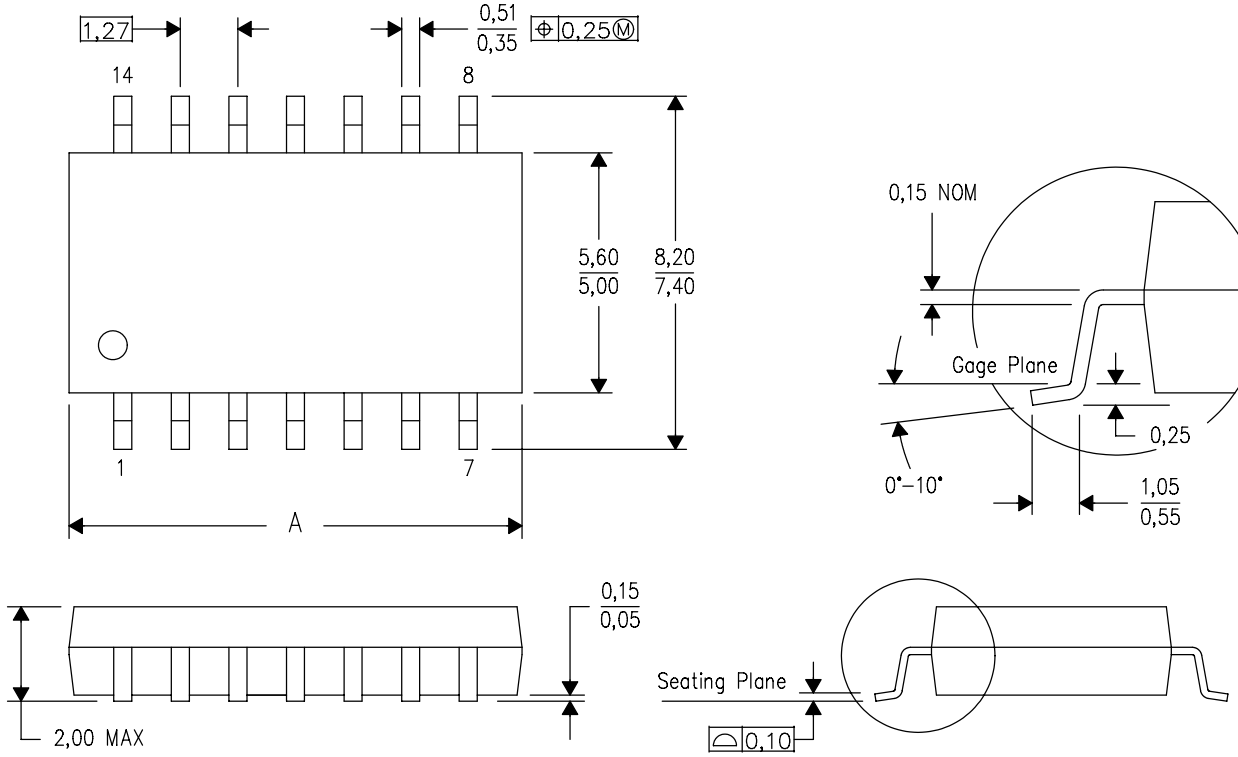
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



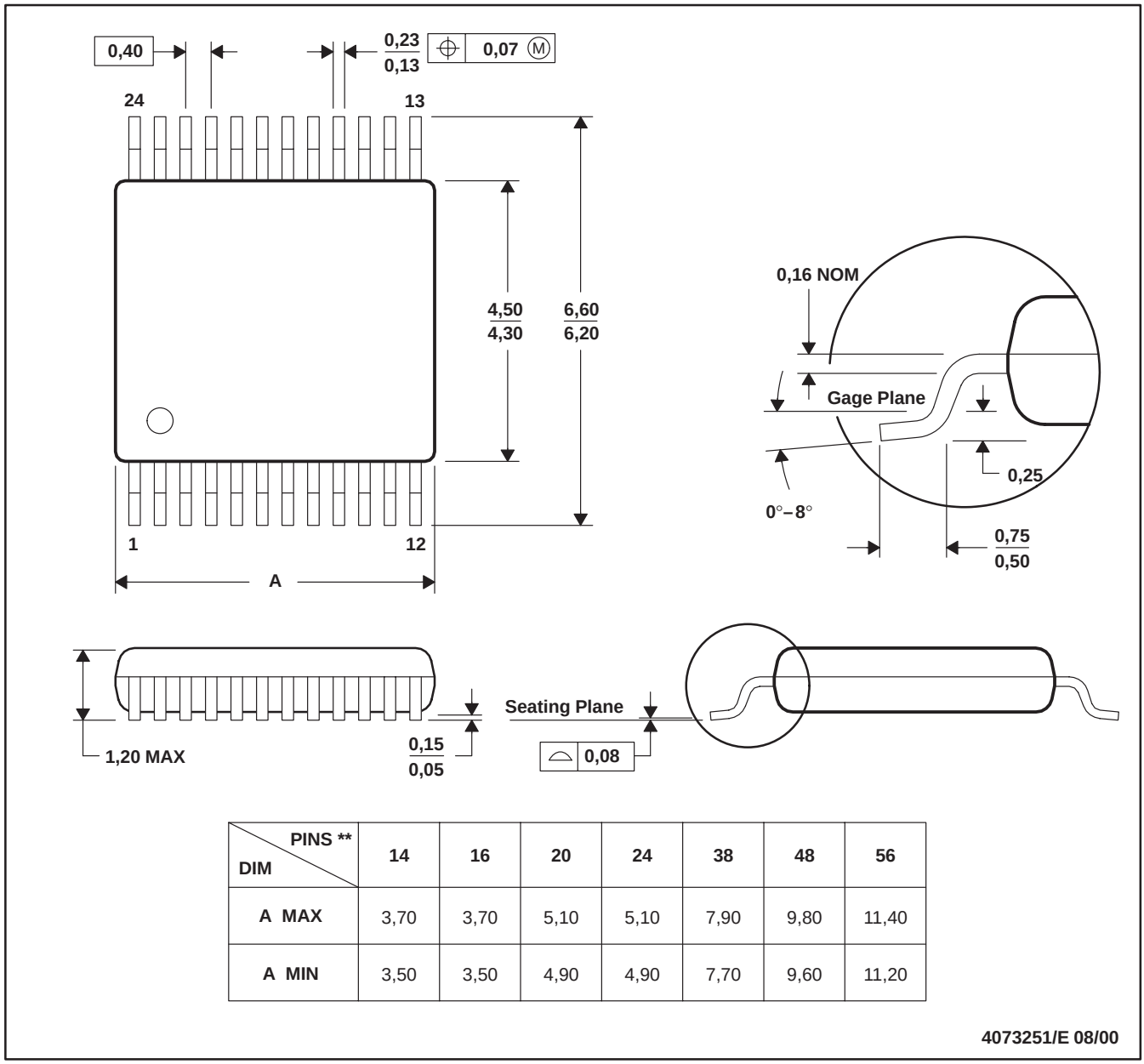
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

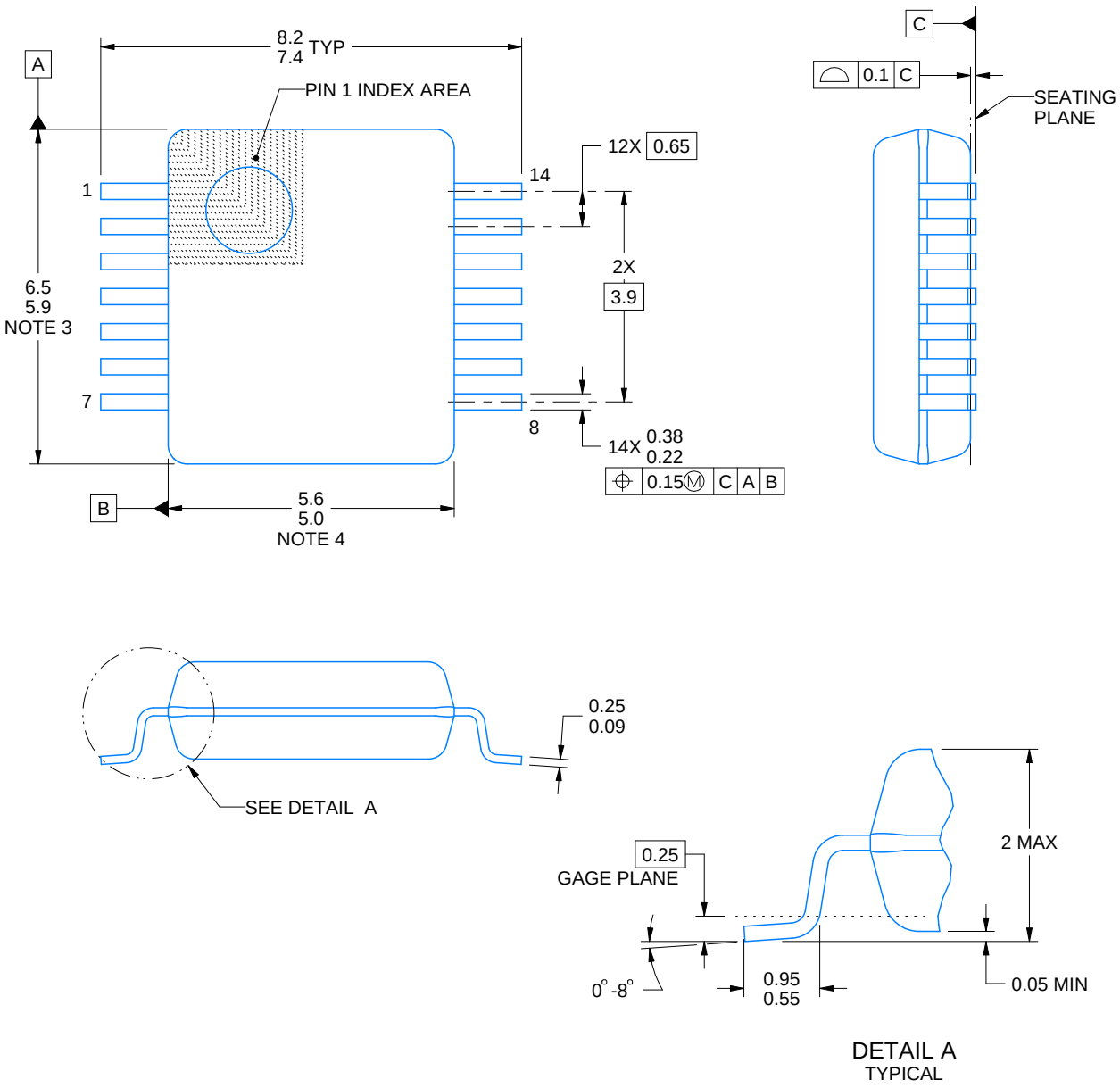
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

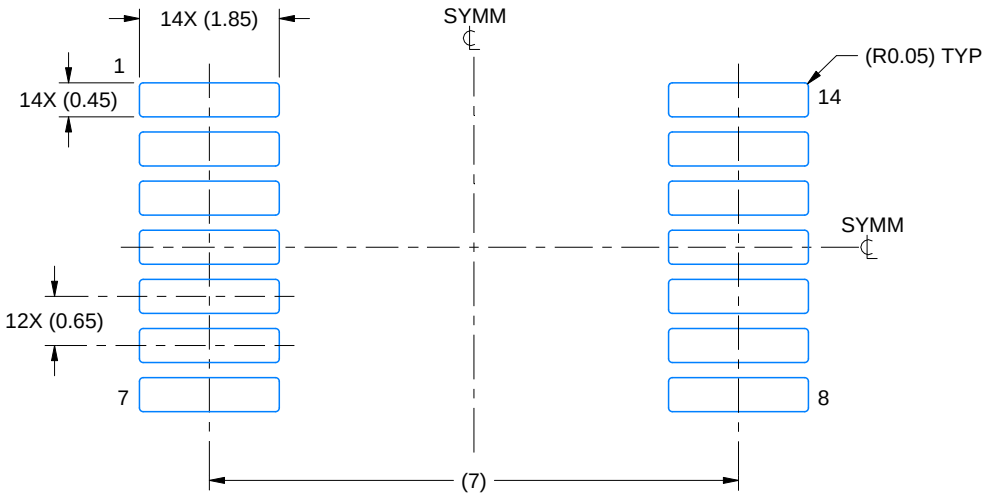
SMALL OUTLINE PACKAGE



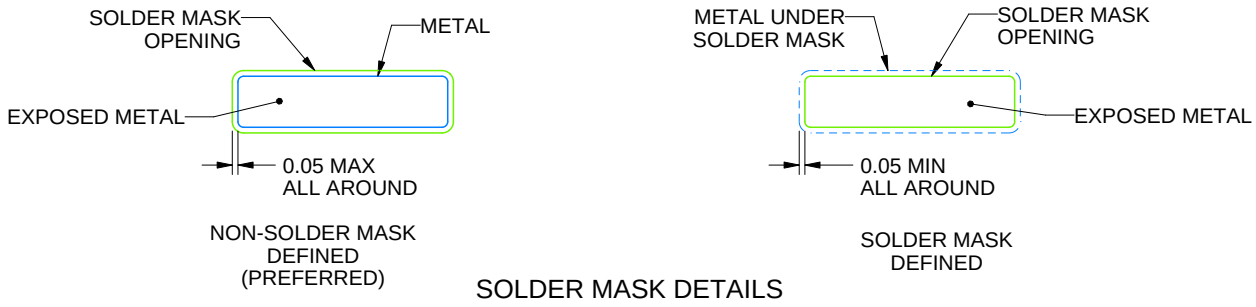
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

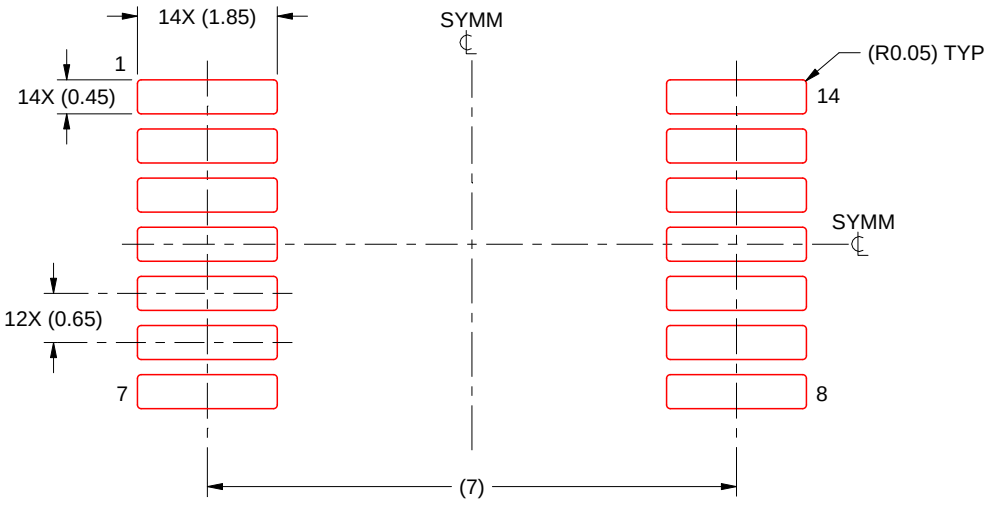


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

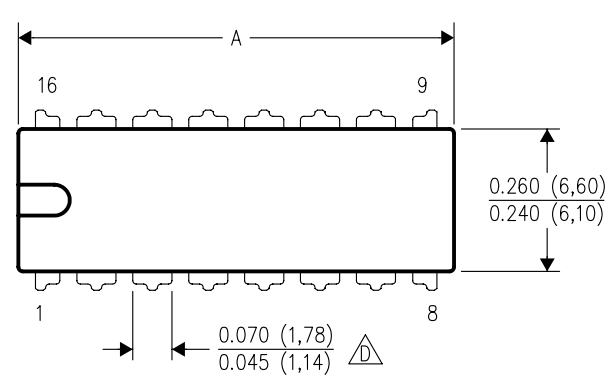
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

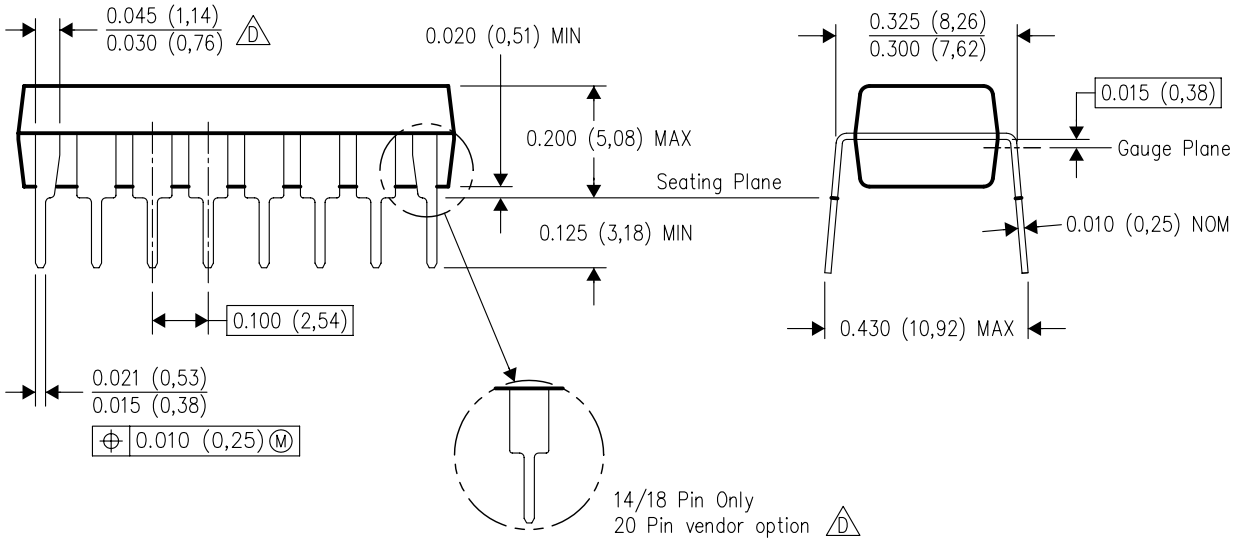
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

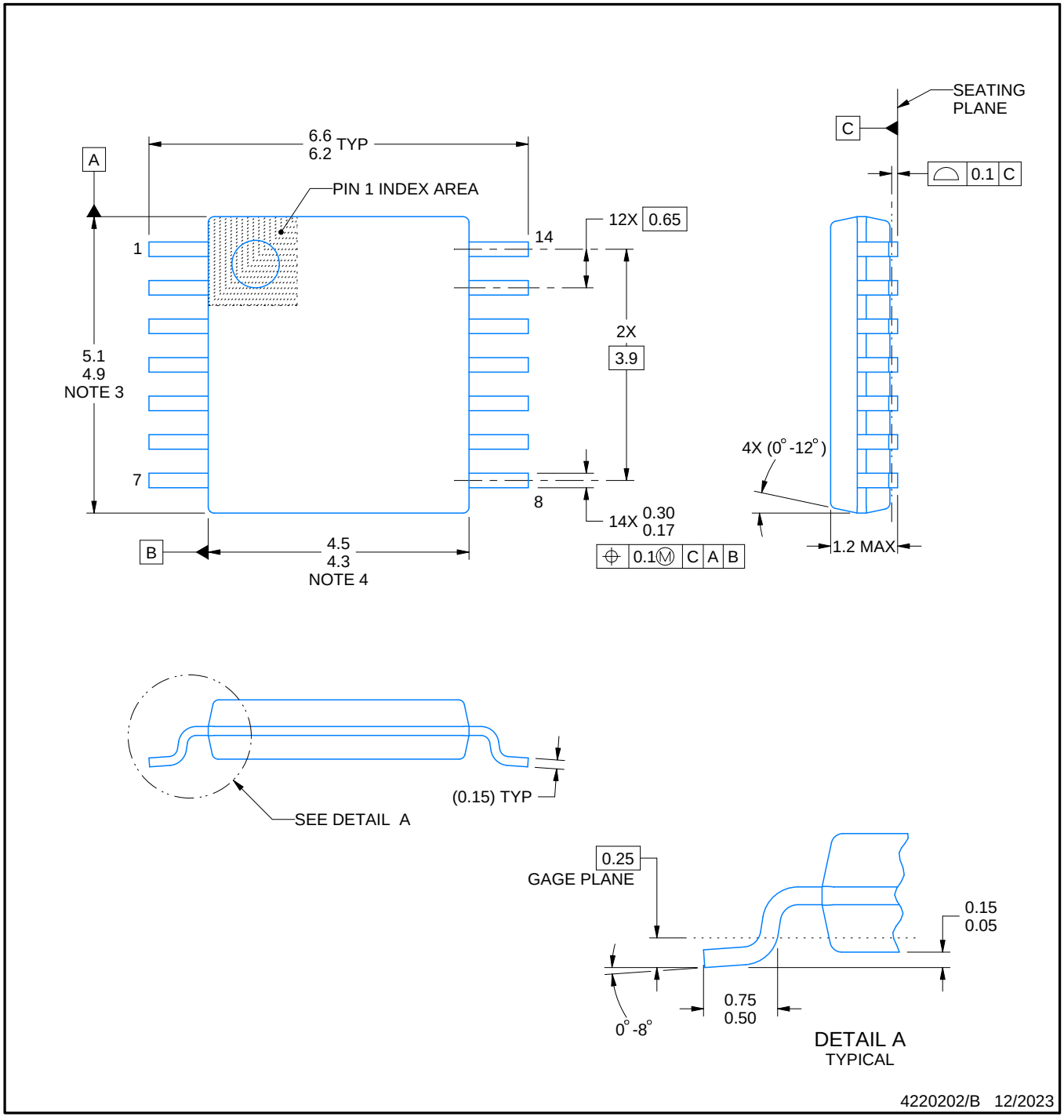
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

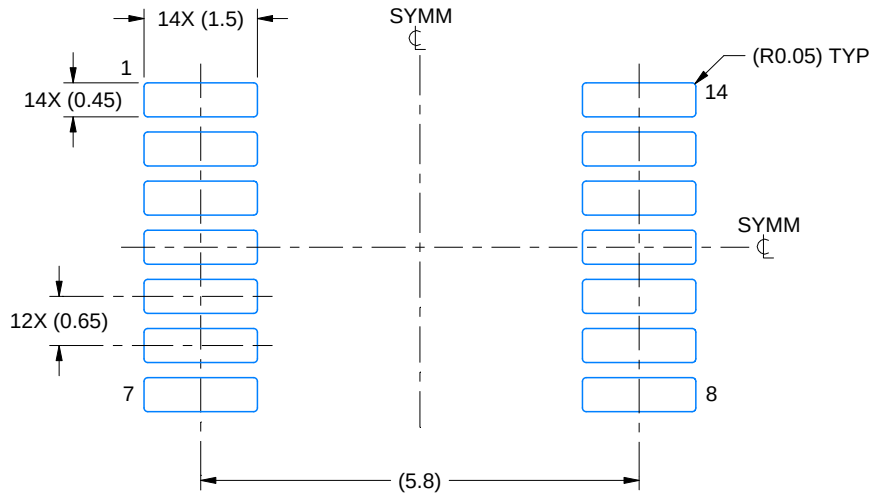
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

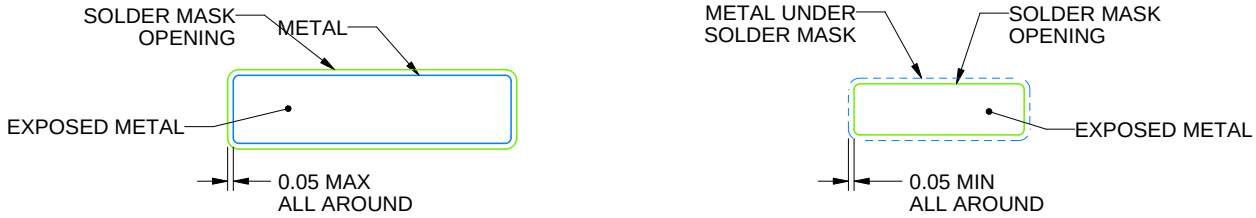


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

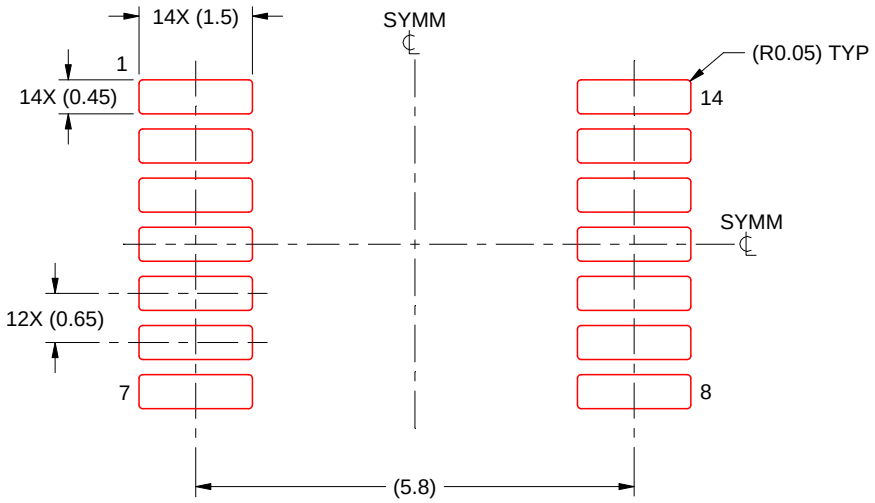


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

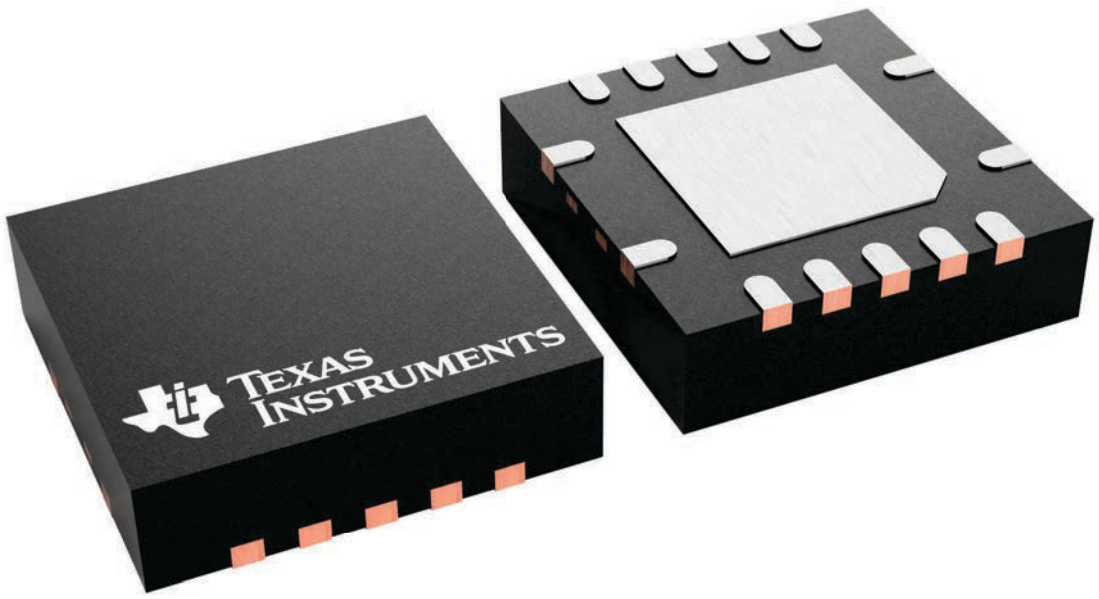
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



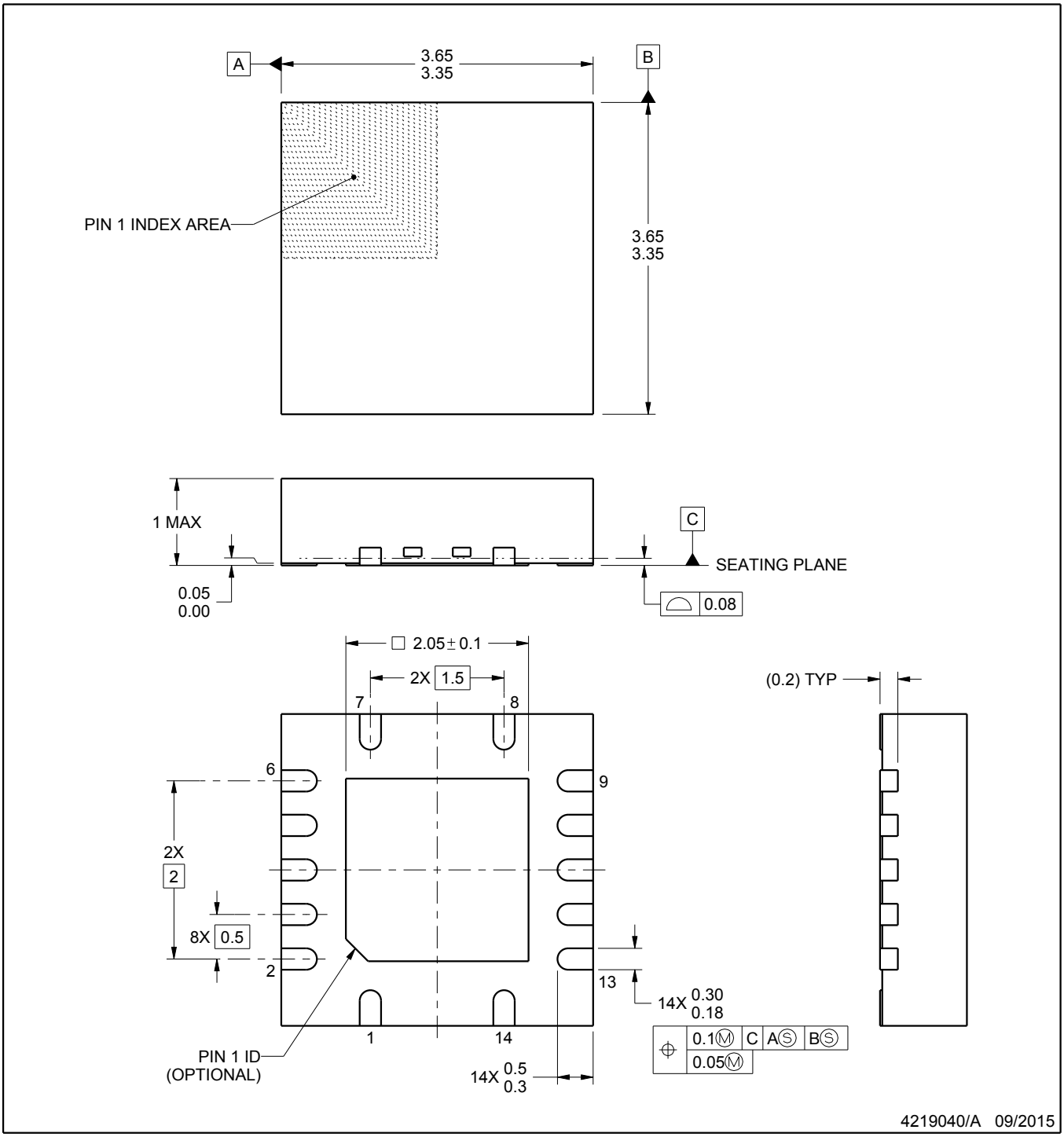
4231541/A

PACKAGE OUTLINE

RGY0014A

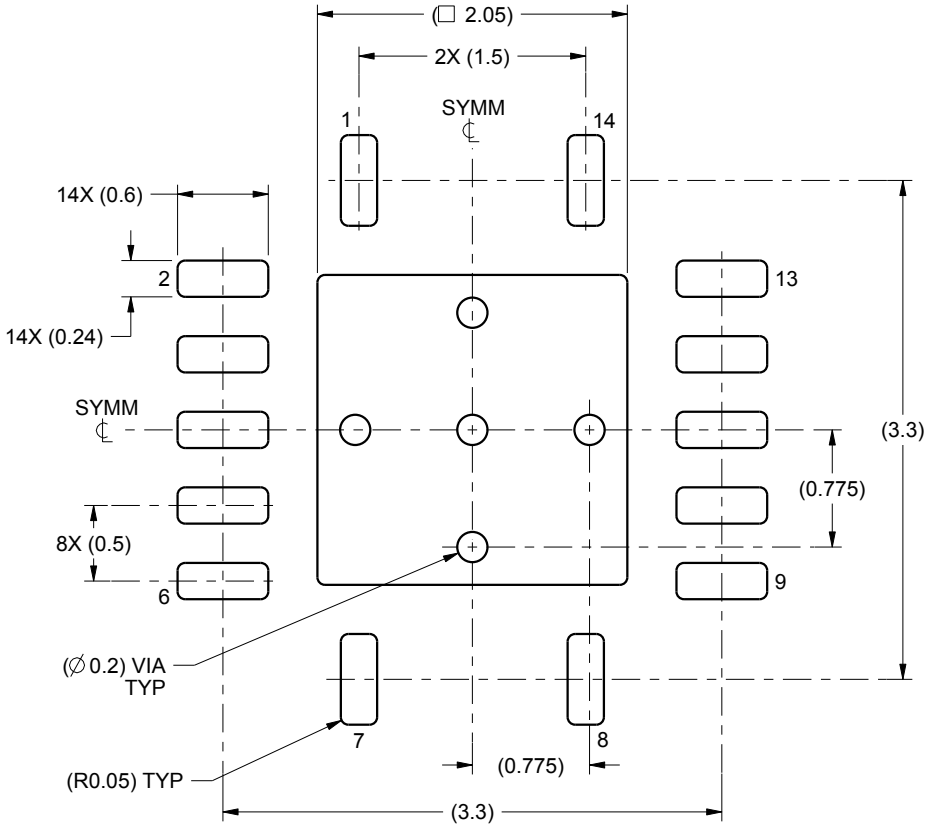
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

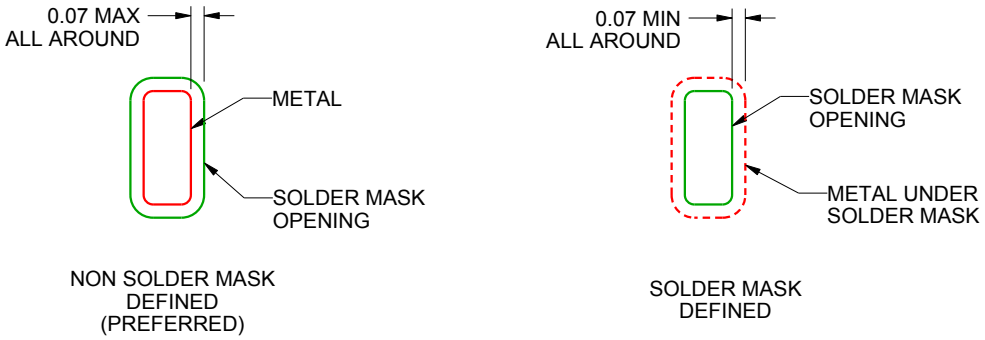


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

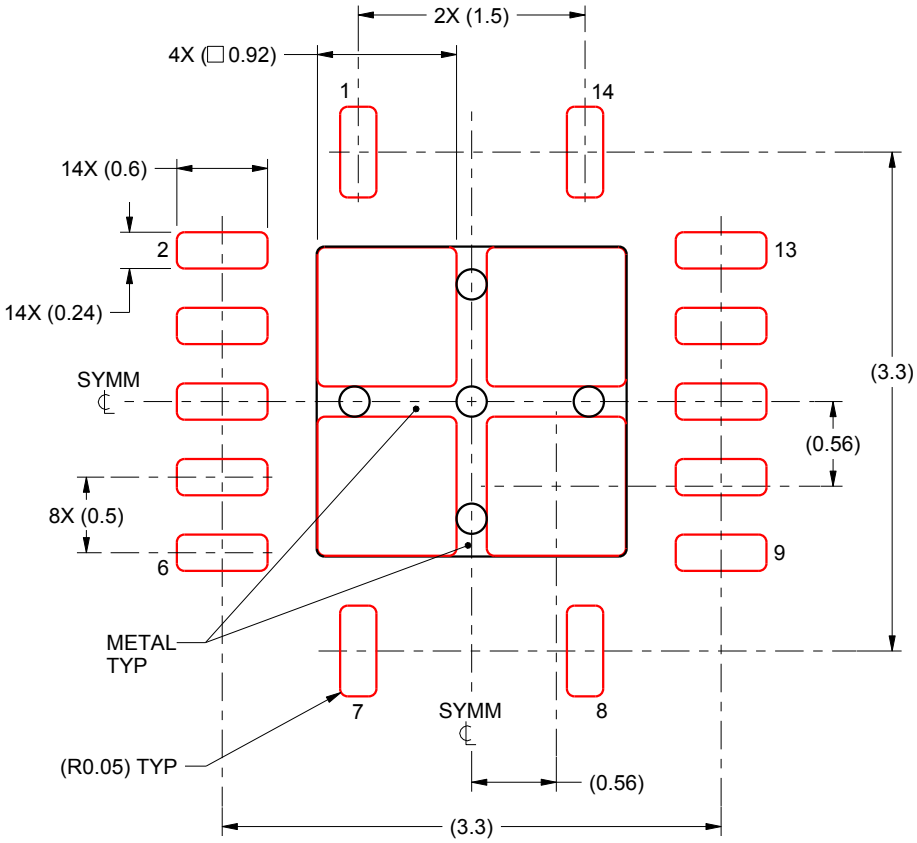


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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