

SN74LV4052A 双路 4 通道模拟多路复用器和多路解复用器

1 特性

- 1.65V 至 5.5V V_{CC} 运行
- 快速开关
- 高开关输出电压比
- 低开关串扰
- 极低输入电流
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求：
 - 2000V 人体放电模型 (A114-A)
 - 1000V 充电器件模型 (C101)

2 应用

- 电信
- 信息娱乐系统
- 信号选通和隔离
- 家用电器
- 可编程逻辑电路
- 调制和解调

3 说明

SNx4LV4052A 器件是可在 1.65V 至 5.5V V_{CC} 电压下运行的双路 4 通道 CMOS 模拟多路复用器和多路解复用器。

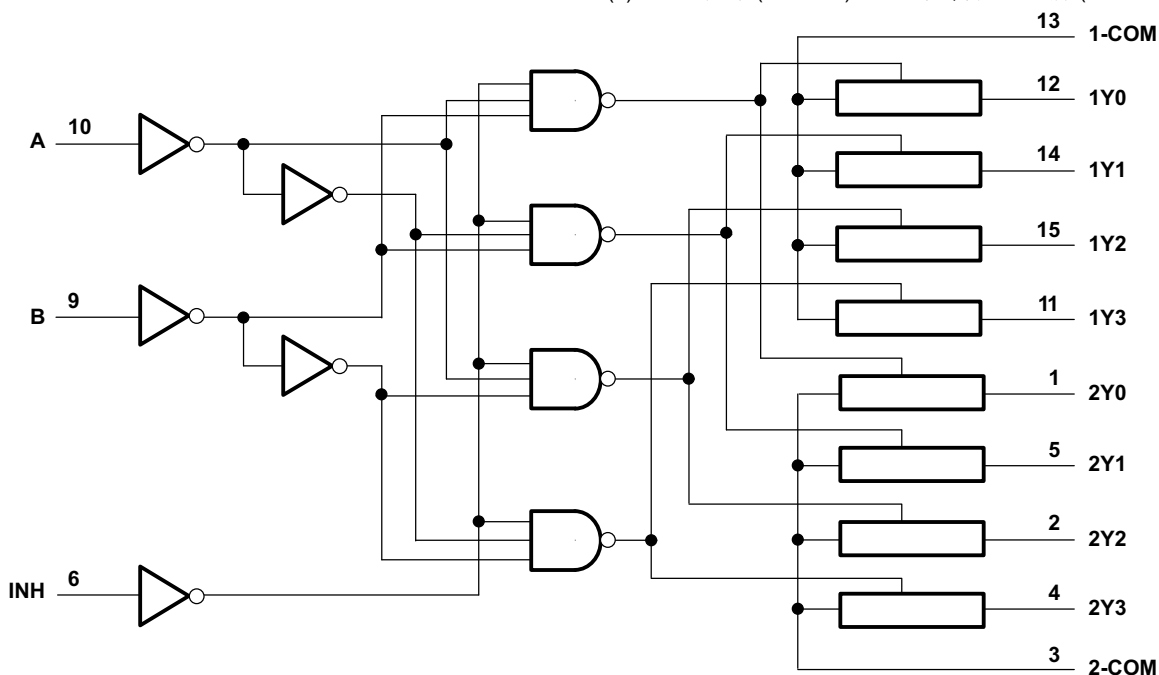
SNx4LV4052A 器件能够处理模拟和数字信号。每个通道允许在任意方向传输振幅高达 5.5V (峰值) 的信号。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SNx4LV4052A	D (SOIC, 16)	9.9mm × 6mm
	PW (TSSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4mm × 3.5mm
	DYY (SOT-23-THIN, 16)	4.2mm × 3.26mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



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逻辑图 (正逻辑)



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4 Pin Configuration and Functions

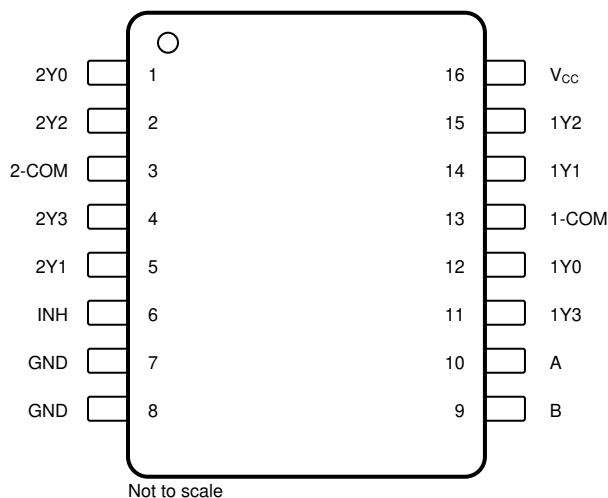


图 4-1. D, PW, or DYY Packages, 16-Pin SOIC, TSSOP, or SOT-23-THIN (Top View)

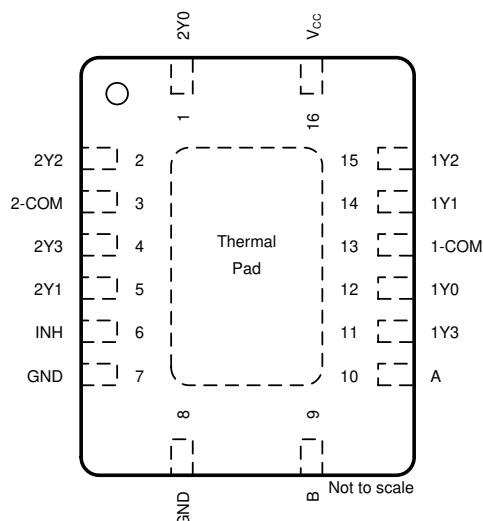


图 4-2. RGY Package, 16-Pin VQFN With Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
2Y0	1	I/O	Port 2 channel 0
2Y2	2	I/O	Port 2 channel 2
2-COM	3	I/O	Port 2 common channel
2Y3	4	I/O	Port 2 channel 3
2Y1	5	I/O	Port 2 channel 1
INH	6	I	Inhibit input
GND	7	—	Device ground
GND	8	—	Device ground
B	9	I	Logic input selector B
A	10	I	Logic input selector A
1Y3	11	I/O	Port 1 channel 3
1Y0	12	I/O	Port 1 channel 0
1-COM	13	I/O	Port 1 common channel
1Y1	14	I/O	Port 1 channel 1
1Y2	15	I/O	Port 1 channel 2
V _{CC}	16	—	Device power

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
V_{CC}	Supply voltage	- 0.5	7.0	V
V_I	Logic input voltage range	- 0.5	7.0	V
V_{IO}	Switch I/O voltage range ^{(2) (3)}	- 0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	- 20	mA
I_{IOK}	Switch IO diode clamp current	$V_{IO} < 0$ or $V_{IO} > V_{CC}$	50	mA
I_T	Switch continuous current	$V_{IO} = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5 V maximum

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000	V
		Charged device model (CDM), per AEC Q100-011	±2000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4052A

THERMAL METRIC ⁽¹⁾		SN74LV4052A	SN74LV4052A	SN74LV4052A	SN74LV4052A	UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	140.2	89.4	199.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.0	72.6	89.7	121.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.6	98.7	65.4	129.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	31.3	13.4	25.0	24.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.7	97.3	65.2	126.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	48.9	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		1 ⁽²⁾		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 1.65	1.2		5.5	V
		V _{CC} = 2 V	1.5		5.5	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		5.5	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		5.5	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 1.65	0		0.4	V
		V _{CC} = 2 V	0		0.5	
		V _{CC} = 2.3 V to 2.7 V	0	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	0	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	0	V _{CC} × 0.3		
V _I	Logic control input voltage		0		5.5	V
V _{IO}	Switch input or output voltage		0		V _{CC}	V
Δt / ΔV	Logic input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V			200	ns/V
		V _{CC} = 3 V to 3.6 V			100	
		V _{CC} = 4.5 V to 5.5 V			20	
T _A	Ambient temperature		- 40		125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V_{CC} of ≤ 1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	1.65 V	60	150	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	- 40°C to 85°C	1.65 V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	- 40°C to 125°C	1.65 V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	2.3 V	38	180	Ω
			- 40°C to 85°C			225	
			- 40°C to 125°C			225	
			25°C	3 V	30	150	Ω
			- 40°C to 85°C			190	
			- 40°C to 125°C			190	
			25°C	4.5 V	22	75	Ω
			- 40°C to 85°C			100	
			- 40°C to 125°C			100	
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V	220	600	Ω

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	– 40°C to 85°C	1.65 V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	– 40°C to 125°C	1.65 V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3 V		113	500	Ω
			– 40°C to 85°C				600	
			– 40°C to 125°C				600	
			25°C	3 V		54	180	Ω
			– 40°C to 85°C				225	
			– 40°C to 125°C				225	
			25°C	4.5 V		31	100	Ω
			– 40°C to 85°C				125	
			– 40°C to 125°C				125	
Δ r _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V		3	40	Ω
Δ r _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	– 40°C to 85°C	1.65 V			50	Ω
Δ r _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	– 40°C to 85°C	1.65 V			50	Ω
Δ r _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3 V		2.1	30	Ω
			– 40°C to 85°C				40	
			– 40°C to 125°C				40	
			25°C	3 V		1.4	20	Ω
			– 40°C to 85°C				30	
			– 40°C to 125°C				30	
			25°C	4.5 V		1.3	15	Ω
			– 40°C to 85°C				20	
			– 40°C to 125°C				20	
I _{IH} I _{IL}	Control input current	V _I = 5.5 V or GND	25°C	0 to 5.5 V			0.1	μA
			– 40°C to 85°C				1	
			– 40°C to 125°C				2	
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH}	25°C	5.5 V			0.1	μA
			– 40°C to 85°C				1	
			– 40°C to 125°C				2	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure4)	25°C	5.5 V			0.1	μA
			– 40°C to 85°C				1	
			– 40°C to 125°C				2	
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0 V	25°C	5.5 V		0.01		μA
			– 40°C to 85°C				20	
			– 40°C to 125°C				40	

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _{IC}	Control input capacitance	f = 10 MHz	25°C	3.3 V		2		pF
C _{OS}	Switch terminal capacitance	f = 10 MHz	25°C	3.3 V		5		pF
C _{IS}	Common terminal capacitance	f = 10 MHz	25°C	3.3 V		23		pF
C _{OS(on)}	Common terminal ON-capacitance	f = 10 MHz	25°C	3.3 V		23		pF
C _F	Feedthrough capacitance	f = 10 MHz	25°C	3.3 V		0.5		pF
C _{PD}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	25°C	3.3 V		6		pF

5.6 Timing Characteristics V_{CC} = 2.5 V ± 0.2 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15 pF	25°C		1.9	10	ns
					- 40°C to 85°C			16	
					- 40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15 pF	25°C		6.6	18	ns
					- 40°C to 85°C			23	
					- 40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15 pF	25°C		7.4	18	ns
					- 40°C to 85°C			23	
					- 40°C to 125°C			25	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50 pF	25°C		3.8	12	ns
					- 40°C to 85°C			18	
					- 40°C to 125°C			20	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50 pF	25°C		7.8	28	ns
					- 40°C to 85°C			35	
					- 40°C to 125°C			35	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50 pF	25°C		11.5	28	ns
					- 40°C to 85°C			35	
					- 40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15 pF	25°C		1.2	6	ns
					- 40°C to 85°C			10	
					- 40°C to 125°C			12	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15 pF	25°C		4.7	12	ns
					- 40°C to 85°C			15	
					- 40°C to 125°C			18	

5.7 Timing Characteristics $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (续)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15\text{ pF}$	25°C		5.7	12	ns
					– 40°C to 85°C			15	
					– 40°C to 125°C			18	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$	25°C		2.5	9	ns
					– 40°C to 85°C			12	
					– 40°C to 125°C			14	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C		5.5	20	ns
					– 40°C to 85°C			25	
					– 40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C		8.8	20	ns
					– 40°C to 85°C			25	
					– 40°C to 125°C			25	

5.8 Timing Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15\text{ pF}$	25°C		0.6	4	ns
					– 40°C to 85°C			7	
					– 40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15\text{ pF}$	25°C		3.5	8	ns
					– 40°C to 85°C			10	
					– 40°C to 125°C			12	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15\text{ pF}$	25°C		4.4	10	ns
					– 40°C to 85°C			11	
					– 40°C to 125°C			12	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$	25°C		1.5	6	ns
					– 40°C to 85°C			8	
					– 40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C		4	14	ns
					– 40°C to 85°C			18	
					– 40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C		6.2	14	ns
					– 40°C to 85°C			18	
					– 40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4052	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{ MHz}$ (sine wave) see Figure 7)(1)	$V_{CC} = 2.3\text{ V}$		30	MHz
					$V_{CC} = 3\text{ V}$		35	
					$V_{CC} = 4.5\text{ V}$		50	

5.9 AC Characteristics (续)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Charge Injection (control input to signal output)	INH	COM or Yn		$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $F_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 9)	$V_{CC} = 2.3 \text{ V}$	20		mV
					$V_{CC} = 3 \text{ V}$	35		
					$V_{CC} = 4.5 \text{ V}$	60		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM		$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $F_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 10) (2)	$V_{CC} = 2.3 \text{ V}$	-45		dB
					$V_{CC} = 3 \text{ V}$	-45		
					$V_{CC} = 4.5 \text{ V}$	-45		
Crosstalk (between any switches)	COM or Yn	Yn or COM		$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $F_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 8)(2)	$V_{CC} = 2.3 \text{ V}$	-45		dB
					$V_{CC} = 3 \text{ V}$	-45		
					$V_{CC} = 4.5 \text{ V}$	-45		
Sine-wave distortion	COM or Yn	Yn or COM		$C_L = 50 \text{ pF}$, $R_L = 10 \text{ k}\Omega$, $F_{in} = 1 \text{ kHz}$ (sine wave) (see Figure 11)	$V_I = 2 \text{ V}_{p-p}$ $V_{CC} = 2.3 \text{ V}$	0.1		%
					$V_I = 2.5 \text{ V}_{p-p}$ $V_{CC} = 3 \text{ V}$	0.1		
					$V_I = 4 \text{ V}_{p-p}$ $V_{CC} = 4.5 \text{ V}$	0.1		

5.10 Typical Characteristics

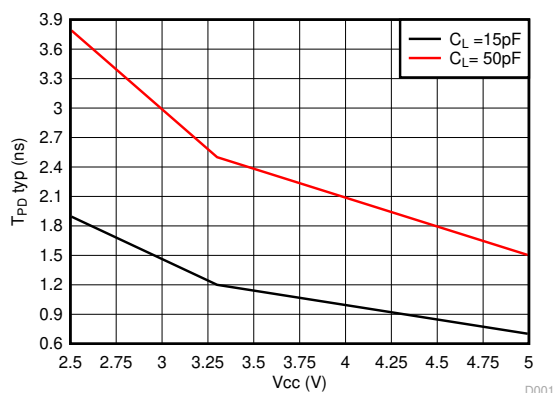


图 5-1. Typical Propagation Delay vs V_{CC}

6 Parameter Measurement Information

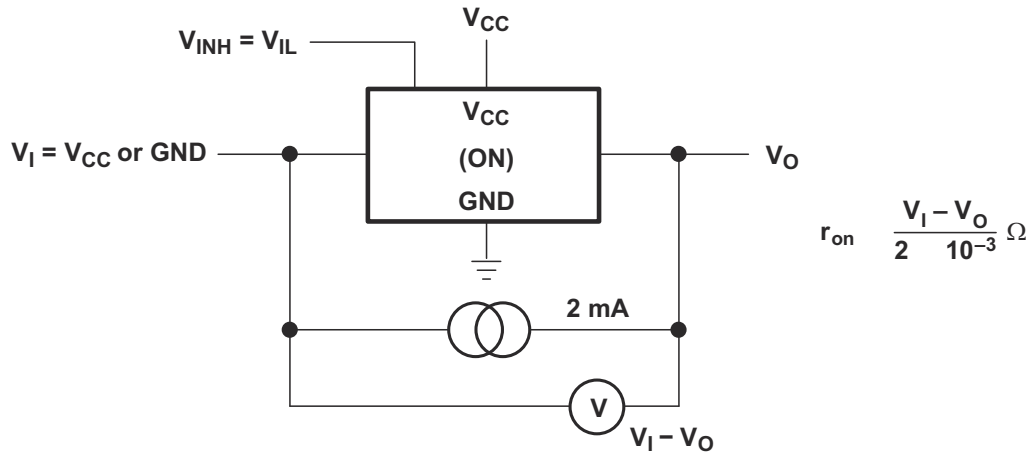


图 6-1. ON-State Resistance Test Circuit

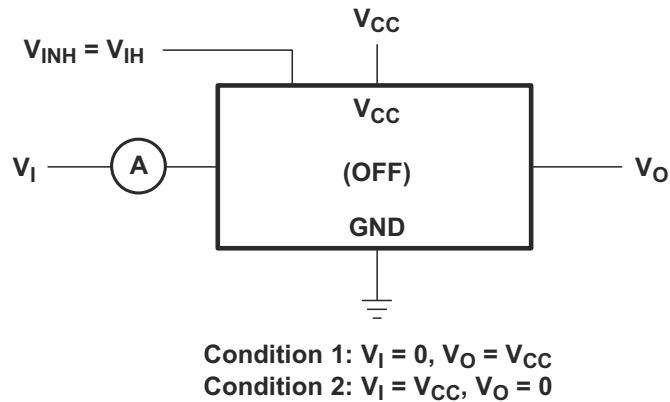


图 6-2. OFF-State Switch Leakage-Current Test Circuit

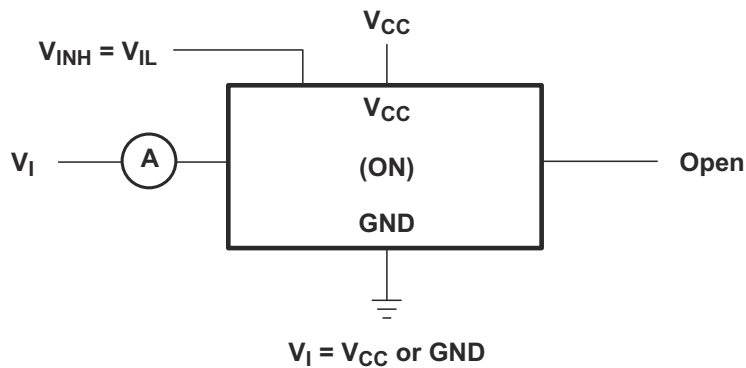


图 6-3. ON-State Switch Leakage-Current Test Circuit

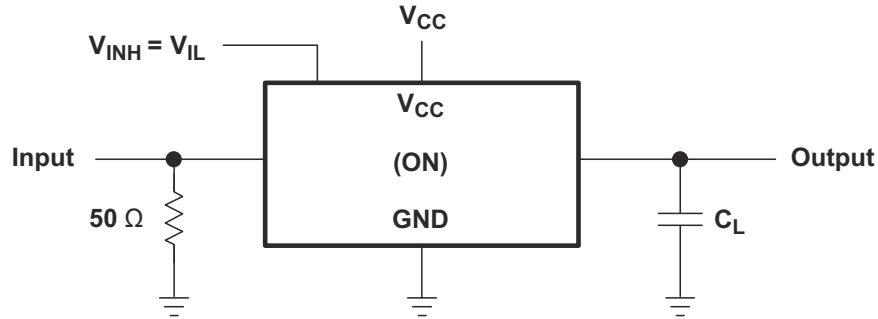


图 6-4. Propagation Delay Time, Signal Input to Signal Output

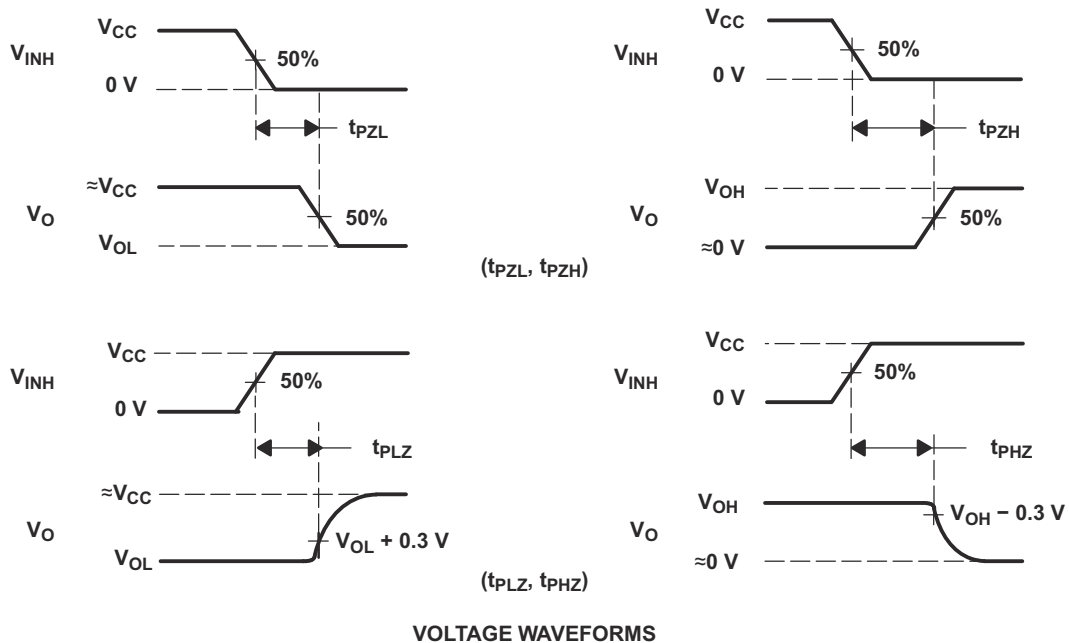
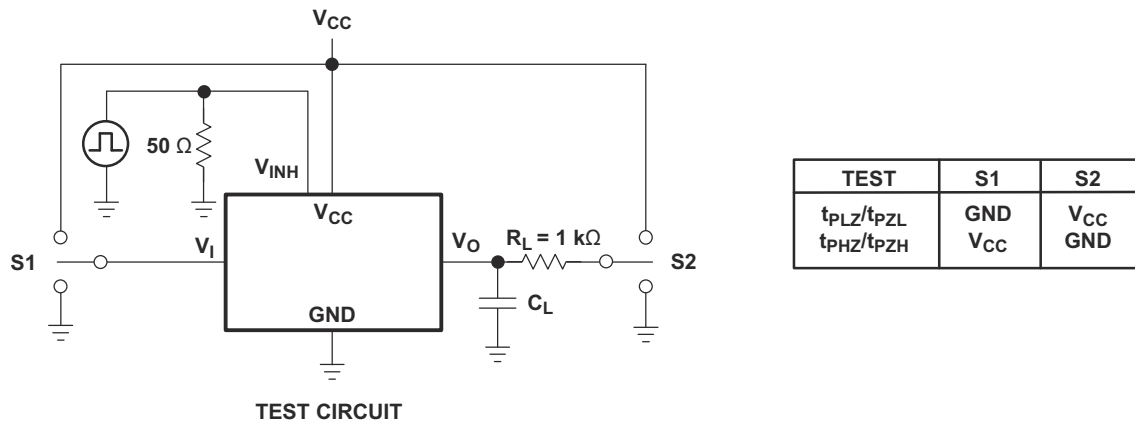
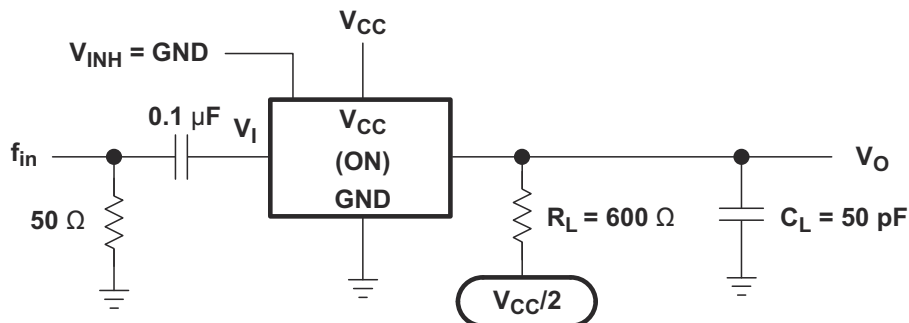


图 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

图 6-6. Frequency Response (Switch ON)

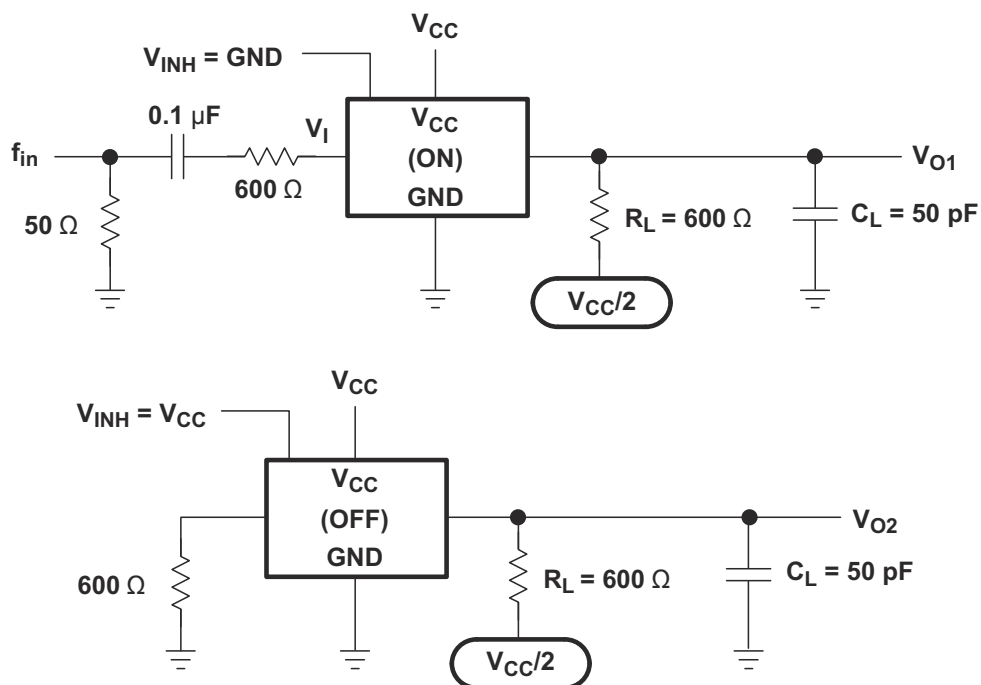


图 6-7. Crosstalk Between Any Two Switches

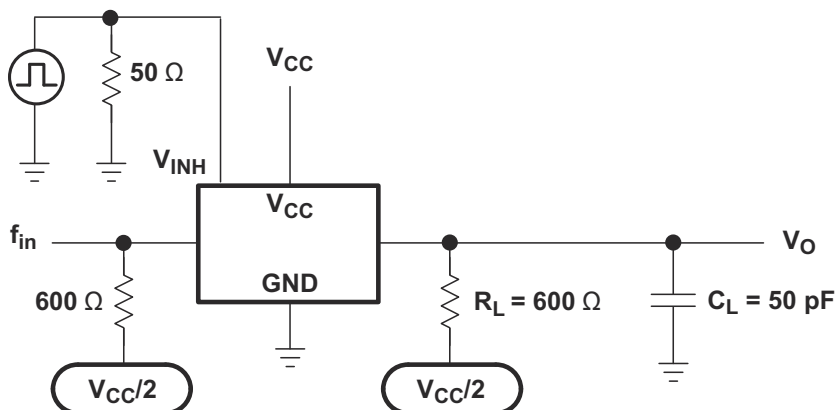


图 6-8. Crosstalk Between Control Input and Switch Output

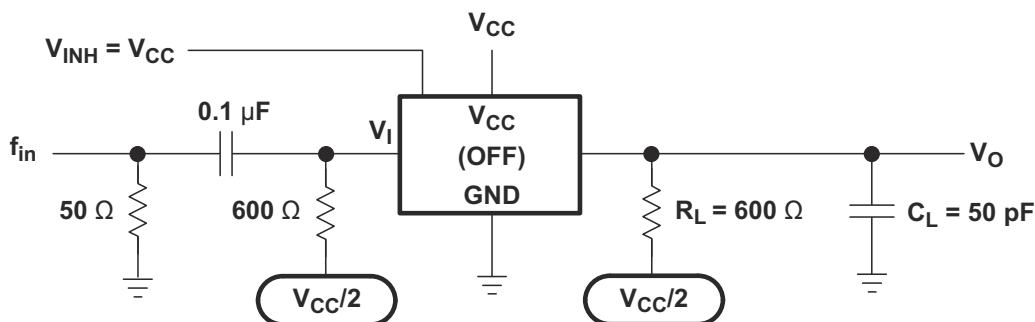


图 6-9. Feedthrough Attenuation (Switch OFF)

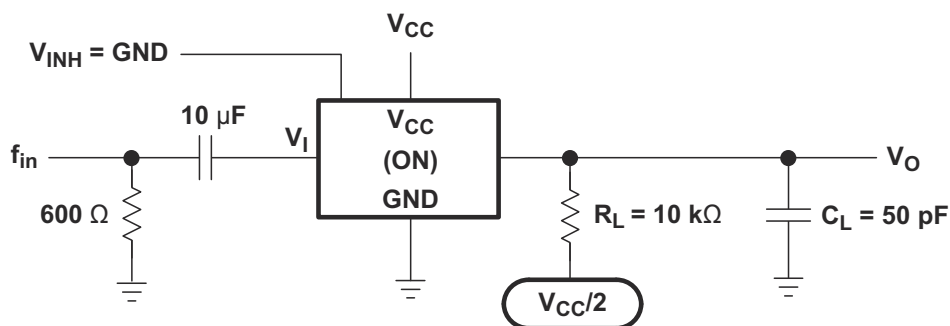


图 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SNx4LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2V to 5.5V V_{CC} operation. It has low input current consumption at the digital input pins and low crosstalk between switches. The active low Inhibit (INH) tri-state all the channels when high and when low, depending on the A and B inputs, one of the four independent input/outputs (nY0 - nY3) connects to the COM channel. The SNx4LV4052A is available in multiple package options including TSSOP (PW), SOIC (D), DYY (SOT-23-THIN) and QFN (RGY).

7.2 Functional Block Diagram

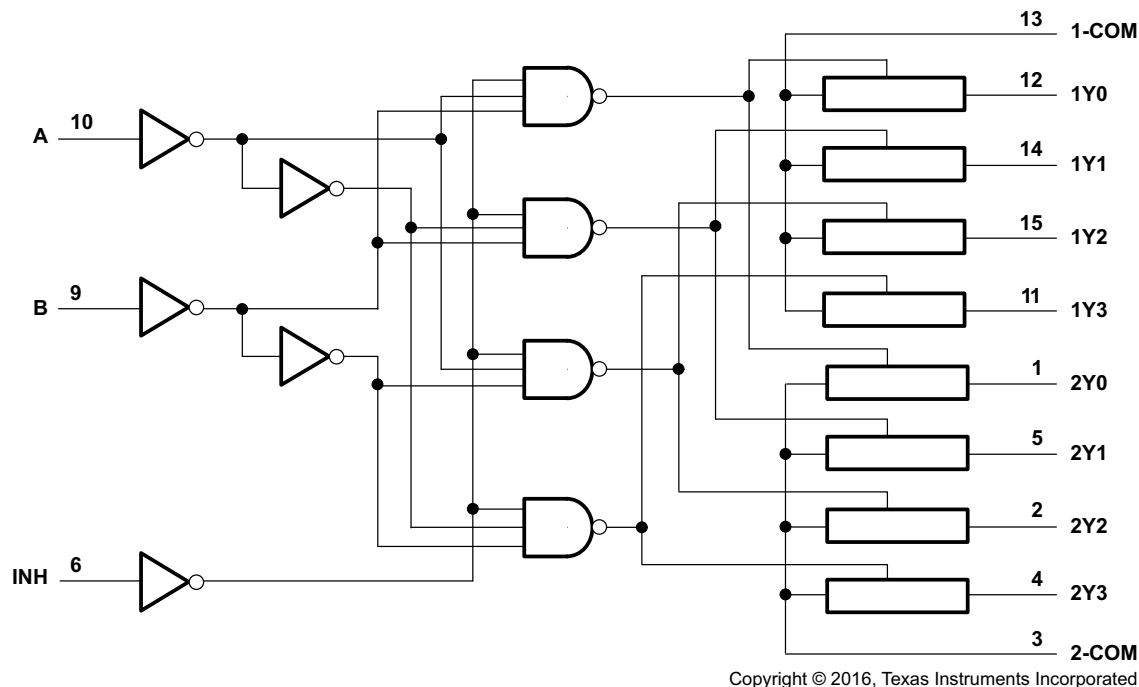


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- The SNx4LV4052A operates from 2V to 5.5V V_{CC} with extremely low input current consumption at the CMOS input pins of A, B and INH.
- The SNx4LV4052A enables fast switching with low crosstalk between the switches. 5.5V peak level bidirectional transmission allowed with the either analog or digital signals.

7.4 Device Functional Modes

表 7-1 lists the functional modes of SNx4LV4052A.

表 7-1. Function Table

INPUTS			ON CHANNELS
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

8 Application and Implementation

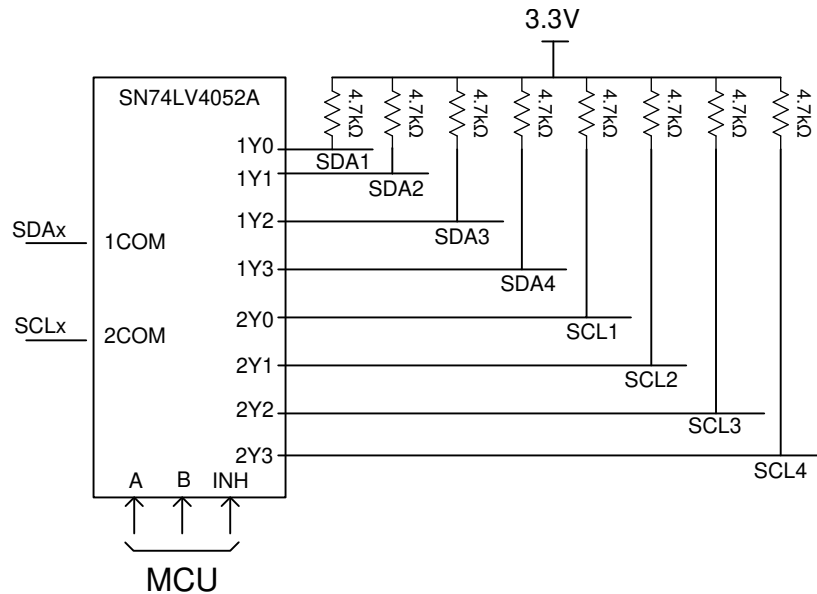
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

Typical applications for the SNx4LV4052A include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

8.2 Typical Application



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图 8-1. Typical I²C Multiplexing Application

8.2.1 Design Requirements

Designing with the SNx4LV4052A device requires a stable input voltage between 2V and 5.5V (see *Recommended Operating Conditions* for details). Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

The SNx4LV4052A dual 1- to 4-channel multiplexer is an excellent choice for I²C selection. The I²C data and clock lines are selected using A,B select lines from the MCU. The pullup resistors are selected based on the capability of the driver. Low pullup resistor results in faster rise time; however, it generates additional current during the low state into the driver. See the *Recommended Operating Conditions* for the input transition rates (V_{IH} and V_{IL}) of the CMOS inputs.

8.2.3 Application Curve

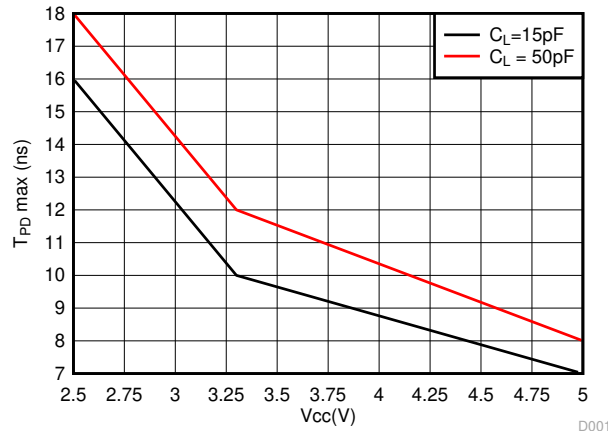


图 8-2. Maximum Propagation Delay vs V_{CC}

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

See the *Recommended Operating Conditions* for operating voltage range for this device. Having bypass capacitors of 0.1μF is highly recommended.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see 图 8-3). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1 in. long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω as required by the application.

Do not place this device too close to high-voltage switching components because they may cause interference. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

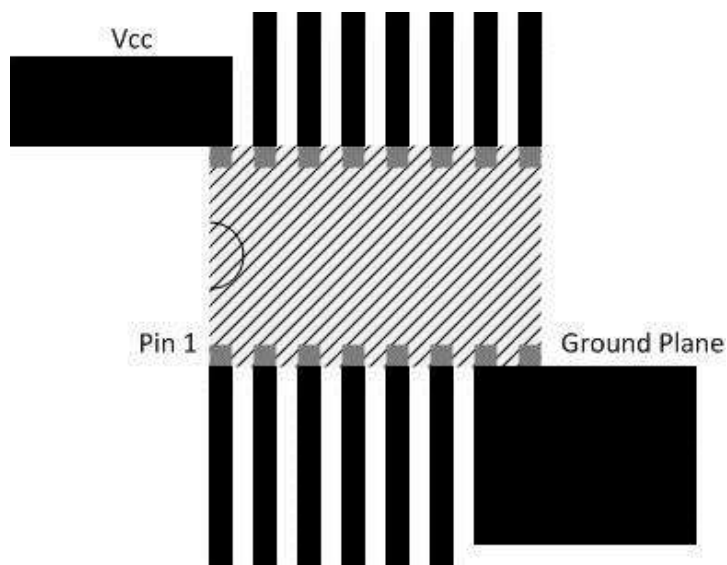


图 8-3. Layout Schematic

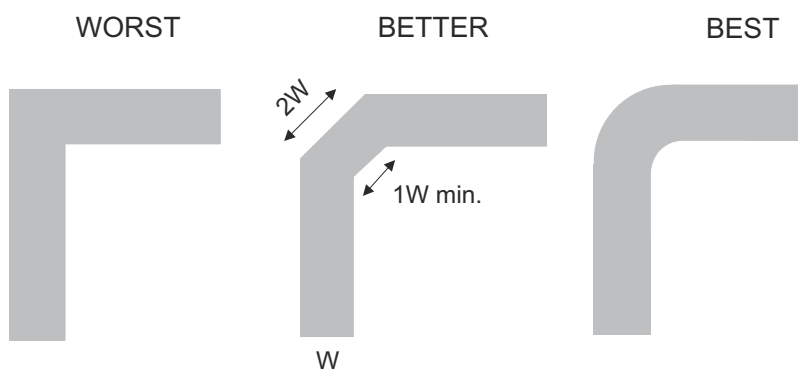


图 8-4. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (September 2024) to Revision N (September 2024)	Page
• 添加了 DYY 封装和尺寸.....	1
• Added DYY package.....	3
• Added DYY package.....	4
• Added DYY package.....	4

Changes from Revision L (June 2024) to Revision M (September 2024)	Page
• Updated ESD Ratings CDM from +/-1500V to +/-2000V.....	4

Changes from Revision K (November 2016) to Revision L (June 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added new VIH and VIL Specifications at 1.65V Vcc.....	5

• Increased max ambient temperature max to 125C.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 125C.....	5
• Added Timing Specifications at 125C.....	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4052AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	LV4052A
SN74LV4052ADBR	NRND	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADBR.A	NRND	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADBRE4	NRND	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A
SN74LV4052ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A
SN74LV4052ADYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052
SN74LV4052ADYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052
SN74LV4052AN	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4052AN
SN74LV4052AN.A	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4052AN
SN74LV4052ANSR	NRND	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A
SN74LV4052ANSR.A	NRND	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A
SN74LV4052APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052APWRG4	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW052A
SN74LV4052APWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW052A
SN74LV4052ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4052A :

- Automotive : [SN74LV4052A-Q1](#)
- Enhanced Product : [SN74LV4052A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

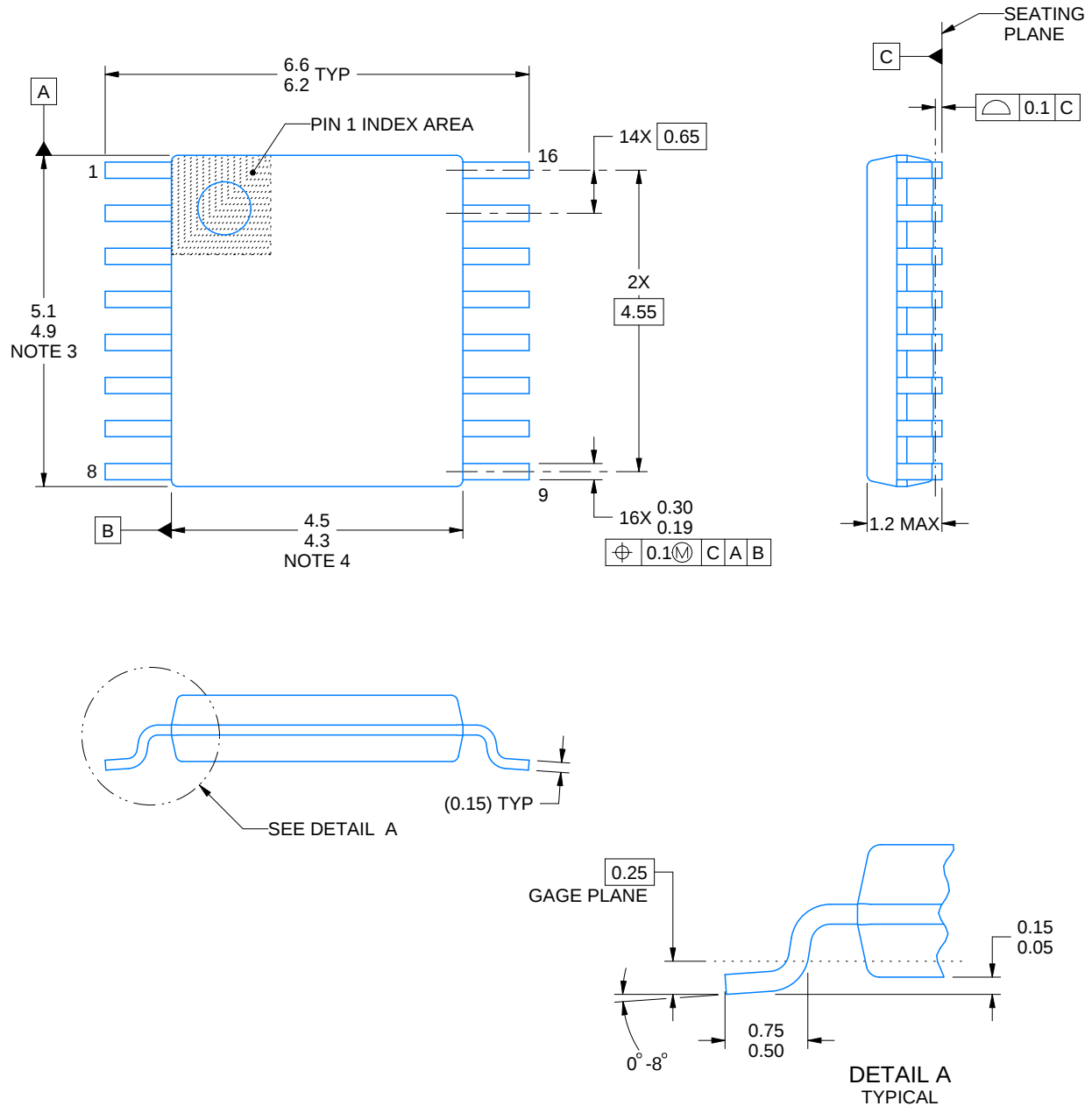
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

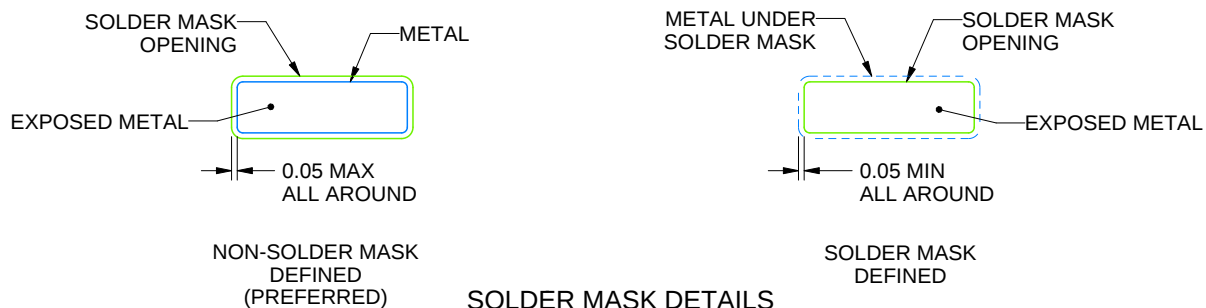
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

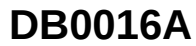


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SSOP - 2 mm max height

Technical drawing of a connector housing, showing three views: Top View, Side View, and Detail A (Typical).

Top View:

- Overall Width: 8.2 TYP (8.2 typical)
- Overall Height: 6.5 (5.9) (NOTE 3)
- Pin 1 Index Area: Circular feature for pin 1 identification.
- Pin 1: Located at the top left corner.
- Pin 16: Located at the top right corner.
- Pin 8: Located at the bottom left corner.
- Pin 9: Located at the bottom right corner.
- Pin Pitch: 5.6 (5.0) (NOTE 4)
- Pin 14: Located at the top right, 14X 0.65.
- Pin 2: Located at the bottom right, 2X 4.55.
- Pin 16: Located at the bottom right, 16X 0.38 0.22.
- Feature Control Frame: $\oplus 0.1 \text{ (M)} \text{ C A B}$

Side View:

- Seating Plane: Indicated by a dashed line.
- Feature Control Frame: $\text{C} \text{ 0.1 C}$

Detail A (Typical):

- Feature Control Frame: $\text{C} \text{ 0.1 C}$
- Dimensions: 0.25, 0.09, 0.25, 0.95, 0.55, 0.05 MIN, 2 MAX.
- Gage Plane: Indicated by a dashed line.
- Angle: $0^\circ - 8^\circ$

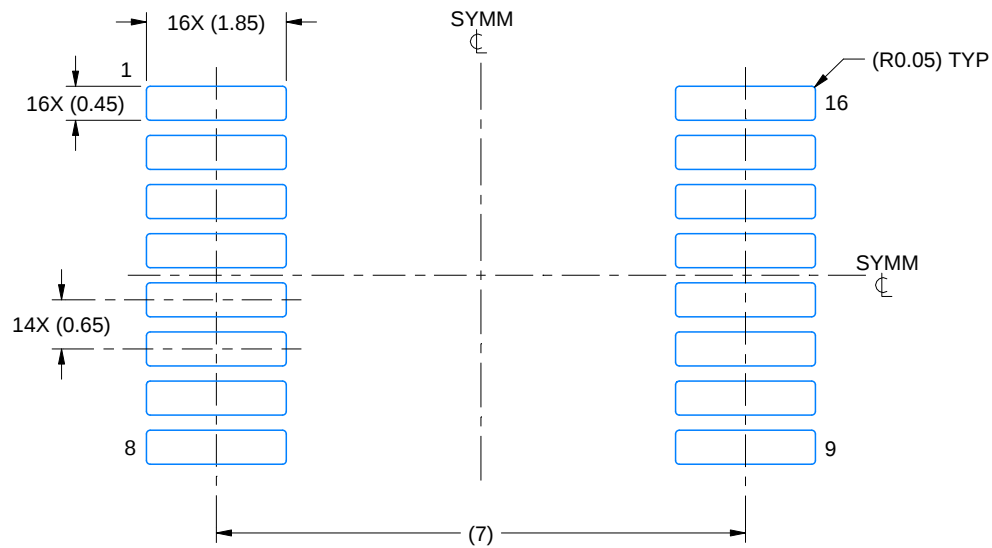
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

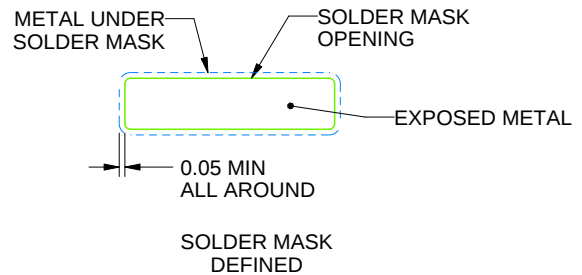
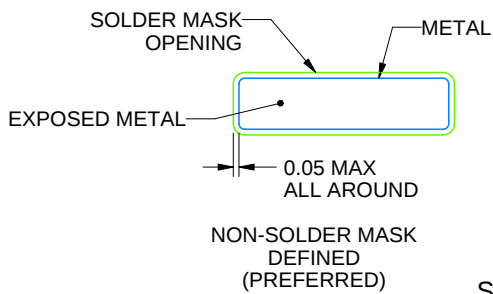
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

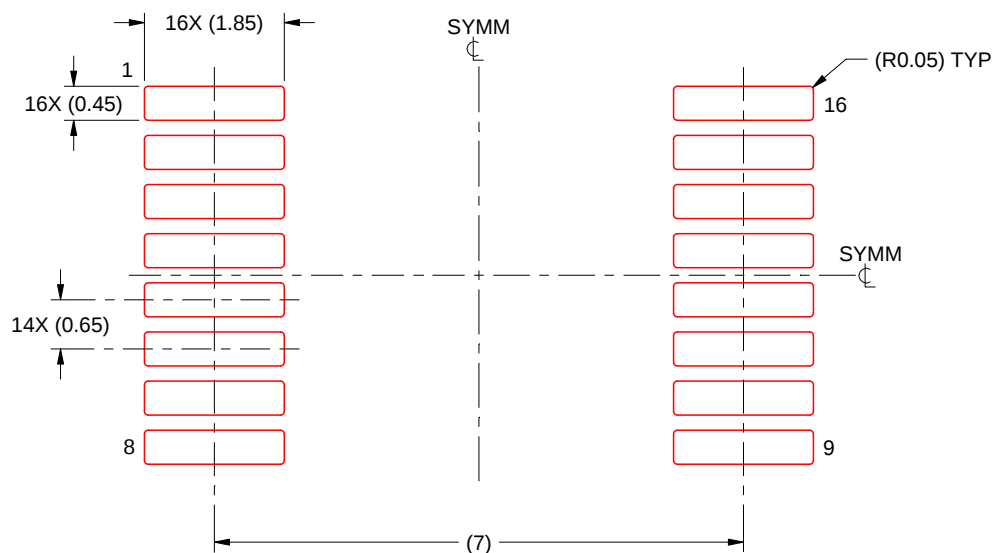
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

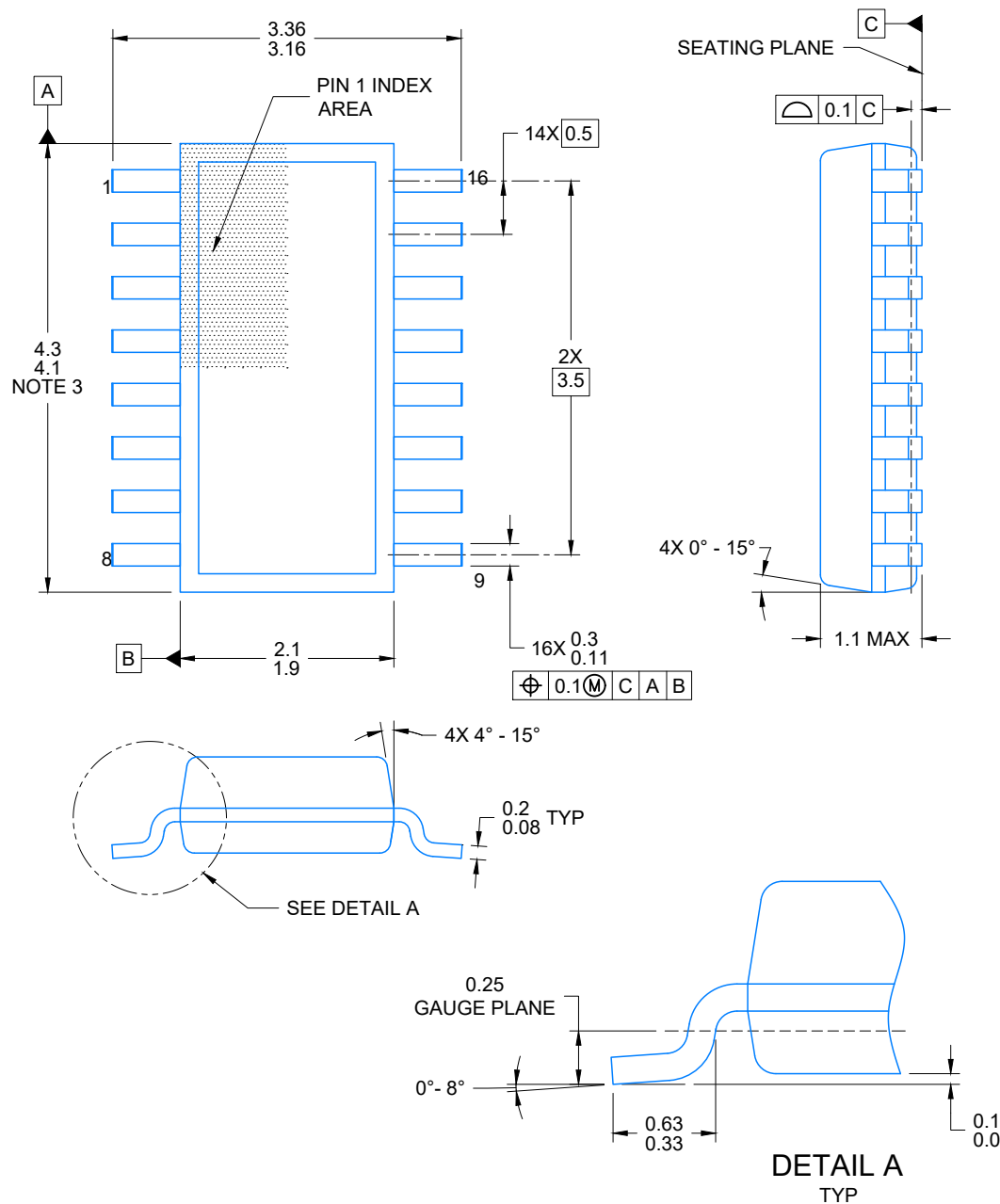
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



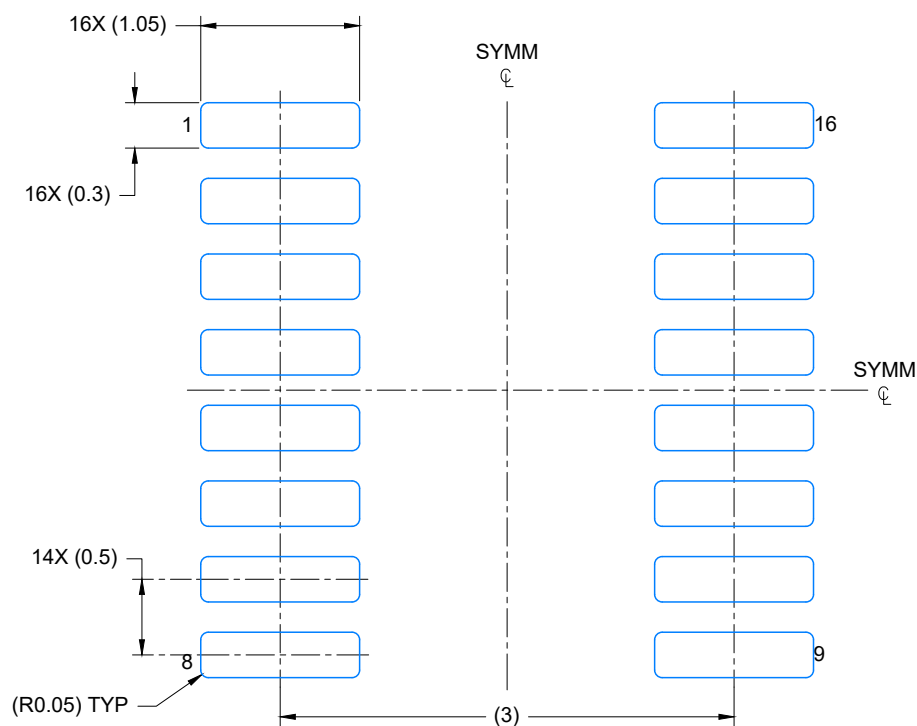
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



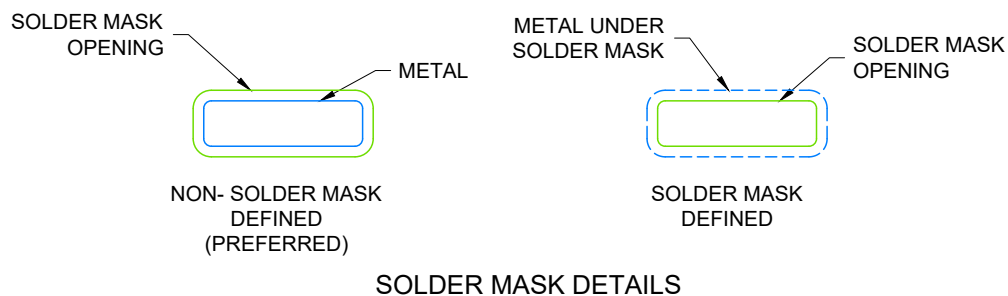
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



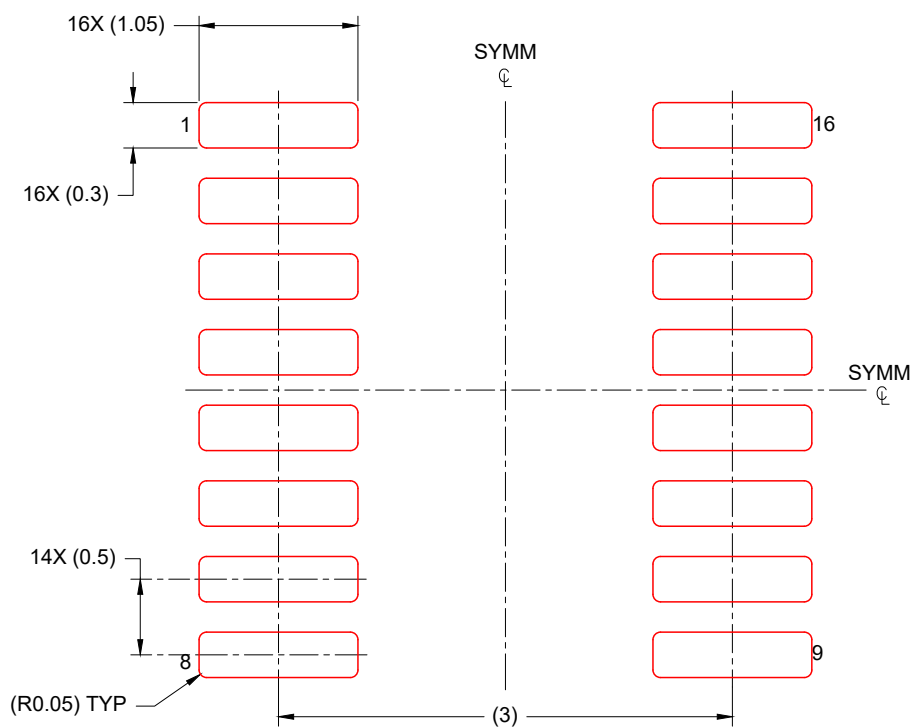
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



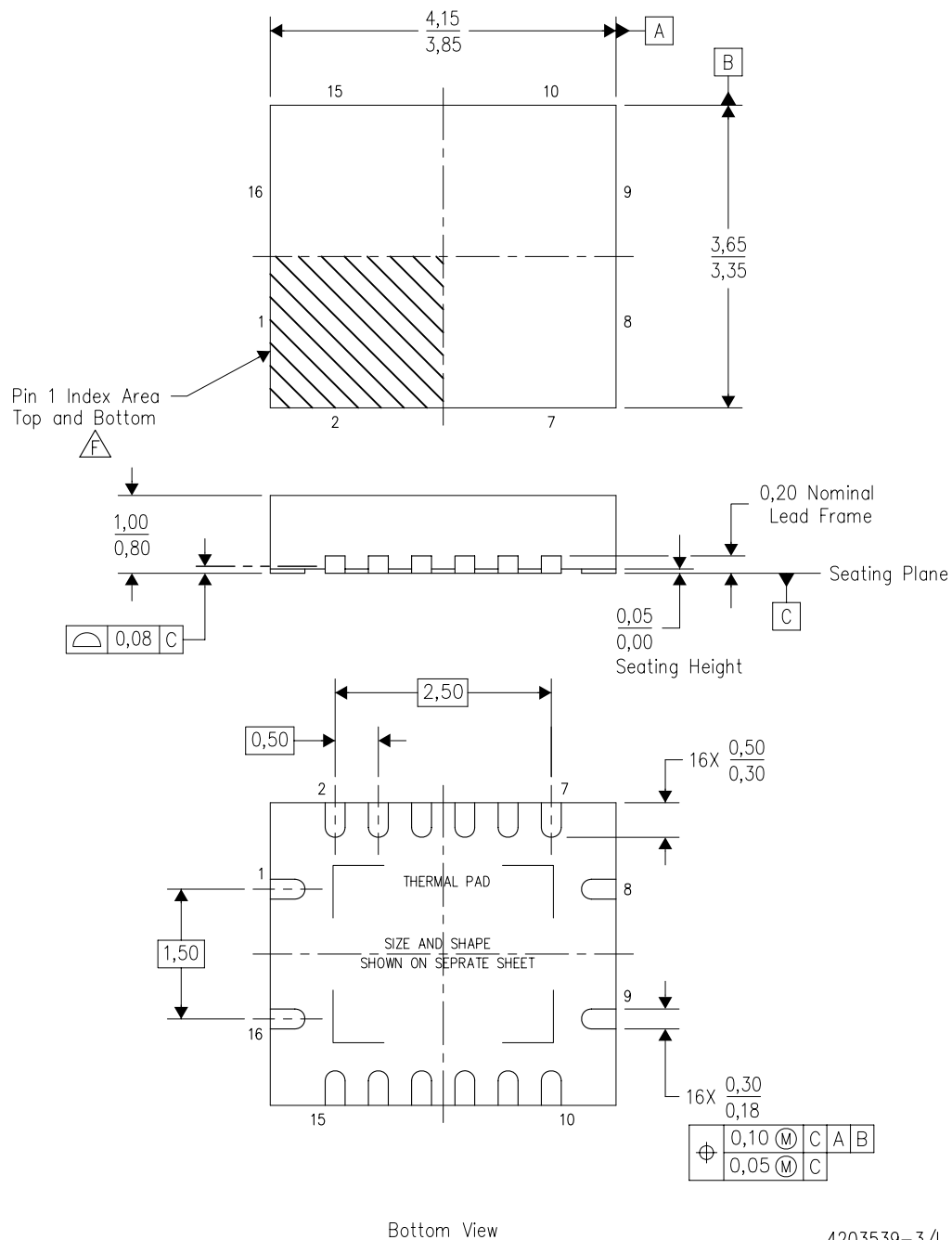
4040049/E 12/2002

NOTES:

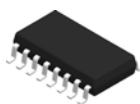
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

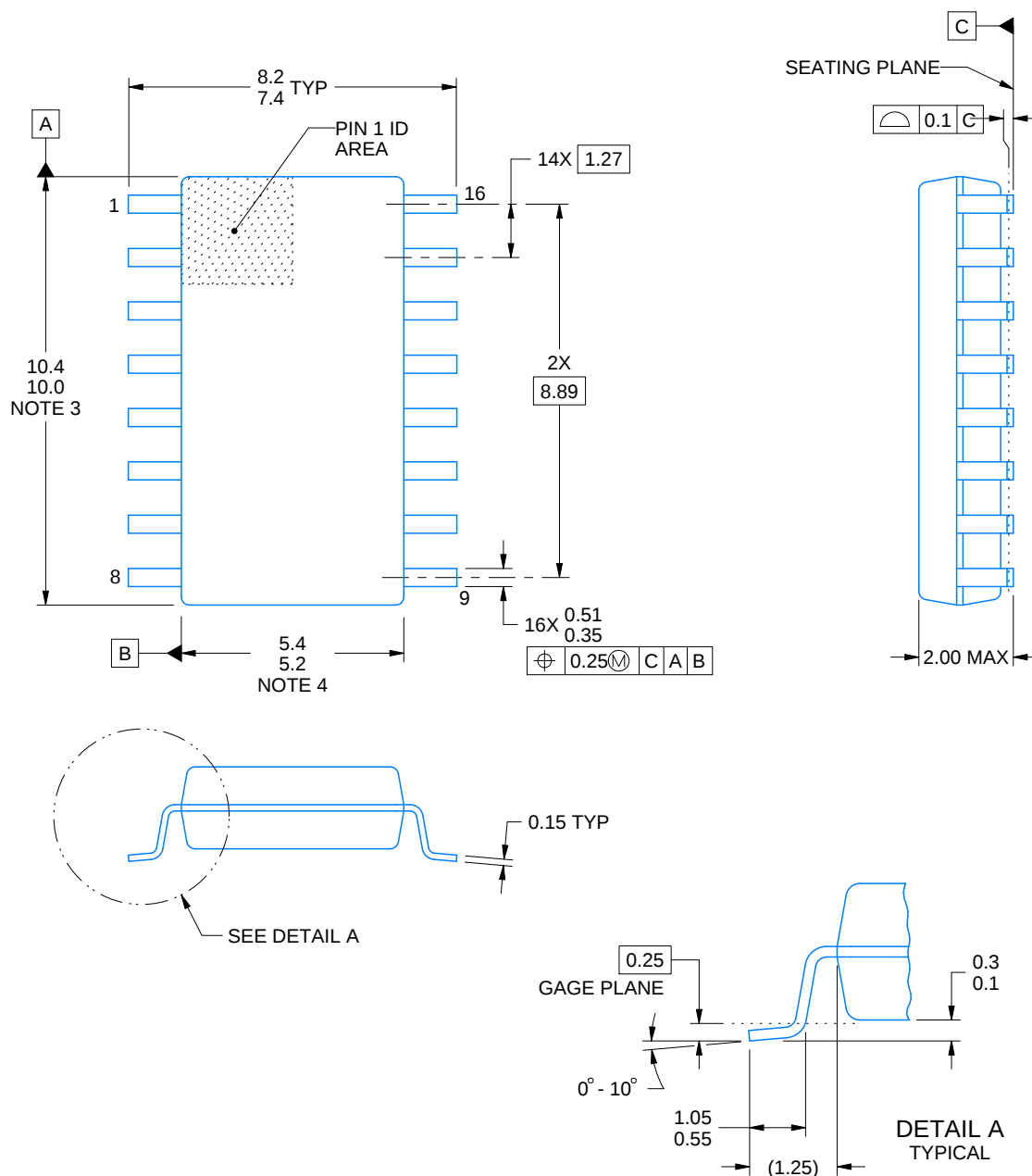


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

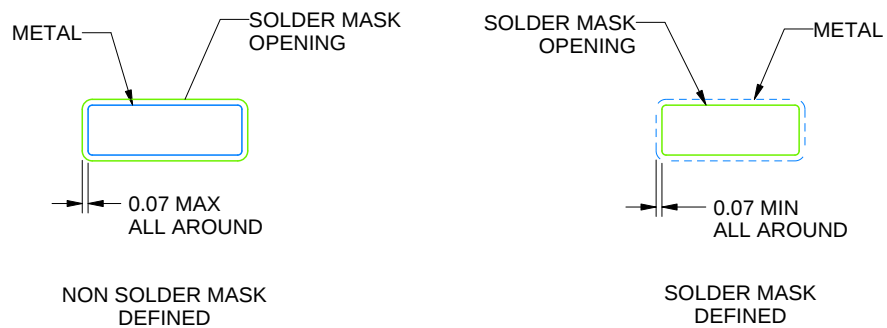
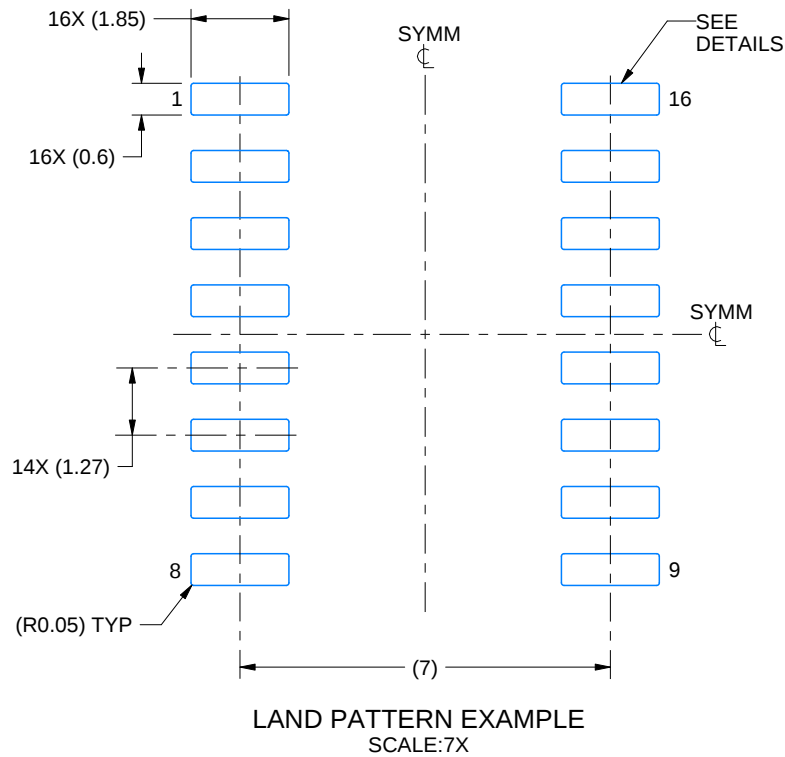
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



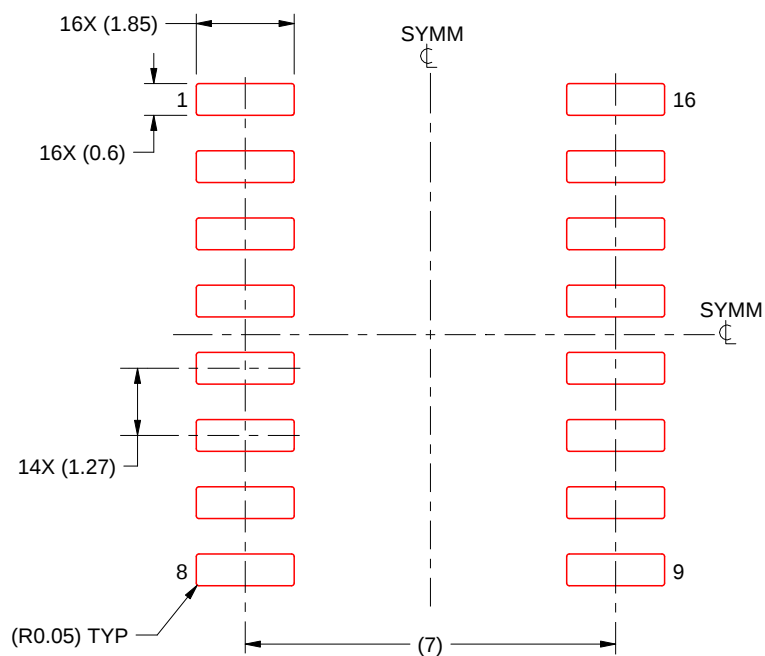
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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