

## SN74LV393B-EP 增强型产品 2V 至 5.5V 低噪声双路 4 位二进制计数器

### 1 特性

- 2V 至 5.5V  $V_{CC}$  运行
- 所有端口上均支持以混合模式电压运行
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- 工作环境温度：-55°C 至 +125°C
- 支持国防、航空航天和医疗应用：
  - 受控基线
  - 一个组装和测试基地
  - 一个制造基地
  - 延长了产品生命周期
  - 产品可追溯性

### 2 应用

- 增加微控制器上的输入数量
- 扩展系统时钟

### 3 说明

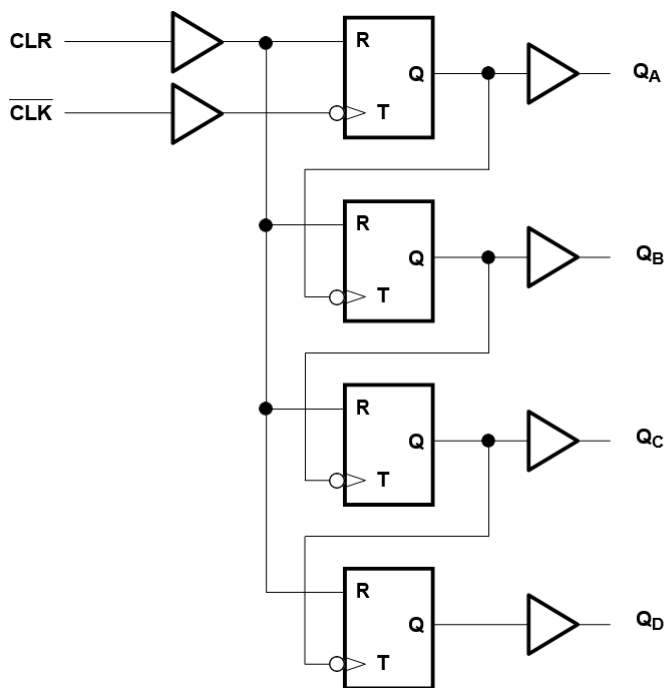
SN74LV393B-EP 包含八个触发器和额外的门控，可在单个封装中实现两个独立的 4 位计数器，而且旨在 2V 至 5.5V  $V_{CC}$  下运行。

该器件完全符合使用  $I_{off}$  的部分断电应用的规范要求。 $I_{off}$  电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
SN74LV393B-EP	PW ( TSSOP, 14 )	5mm × 6.4mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 )。



逻辑图 ( 正逻辑 )



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## 4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

## 5 Pin Configuration and Functions

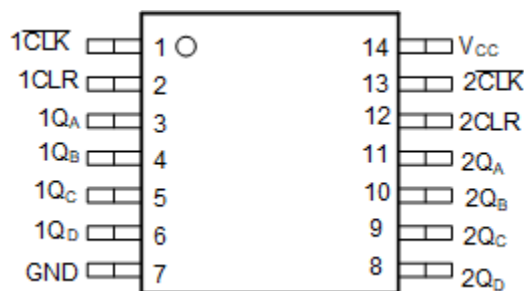


图 5-1. SN74LV393B-EP: PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1CLK	1	I	Counter 1 Clock Input
1CLR	2	I	Counter 1 Clear Input
1Q <sub>A</sub>	3	O	Counter 1 A Output
1Q <sub>B</sub>	4	O	Counter 1 B Output
1Q <sub>C</sub>	5	O	Counter 1 B Output
1Q <sub>D</sub>	6	O	Counter 1 B Output
GND	7	G	Ground
2Q <sub>D</sub>	8	O	Counter 2 D Output
2Q <sub>C</sub>	9	O	Counter 2 C Output
2Q <sub>B</sub>	10	O	Counter 2 B Output
2Q <sub>A</sub>	11	O	Counter 2 A Output
2CLR	12	I	Counter 2 Clear Input
2CLK	13	I	Counter 2 Clock Input
V <sub>CC</sub>	14	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		- 0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>		- 0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		- 0.5	7	V
V <sub>O</sub>	Output voltage <sup>(2)</sup> <sup>(3)</sup>		- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		- 20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		- 50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature		- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 2.3 V to 5.5 V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		– 50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		– 2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		– 6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		– 12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	
Δt / Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature		– 55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV393B-EP	UNIT
		PW (TSSOP)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	151	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	80	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	94.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	28	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	93.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = - 50 mA	2 V to 5.5 V	V <sub>CC</sub> - 0.1		V	
	I <sub>OH</sub> = - 2 mA	2.3 V	2			
	I <sub>OH</sub> = - 6 mA	3 V	2.48			
	I <sub>OH</sub> = - 12 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 mA	2 V to 5.5 V	0.1		V	
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20		μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.8		pF	

## 6.6 Timing Requirements, V<sub>CC</sub> = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK ↓	6		6		ns

## 6.7 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK ↓	5		5		ns

## 6.8 Timing Requirements, V<sub>CC</sub> = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK ↓	4		4		ns

## 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 50\text{ pF}$	30	70		25		MHz
$t_{pd}$	CLK	$Q_A$	$C_L = 50\text{ pF}$		9.3	21.3	1	24.5	ns
		$Q_B$			10.9	23.9	1	27.5	
		$Q_C$			12.3	26.1	1	30	
		$Q_D$			13.4	27.8	1	32	
$t_{PHL}$	CLR	$Q_n$			9.1	17.4	1	20	

## 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 50\text{ pF}$	45	105		35		MHz
$t_{pd}$	CLK	$Q_A$	$C_L = 50\text{ pF}$		6.7	16.7	1	19	ns
		$Q_B$			7.8	19.3	1	22	
		$Q_C$			8.7	21.5	1	24.5	
		$Q_D$			9.5	23.2	1	26.5	
$t_{PHL}$	CLR	$Q_n$			6.8	15.8	1	18	

## 6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 50\text{ pF}$	85	150		75		MHz
$t_{pd}$	CLK	$Q_A$	$C_L = 50\text{ pF}$		4.9	10.5	1	12	ns
		$Q_B$			5.6	11.8	1	13.5	
		$Q_C$			6.2	13.2	1	15	
		$Q_D$			6.6	14.5	1	16.5	
$t_{PHL}$	CLR	$Q_n$			5.2	10.1	1	11.5	

## 6.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>(1)</sup>		SN74LV393A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.2	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

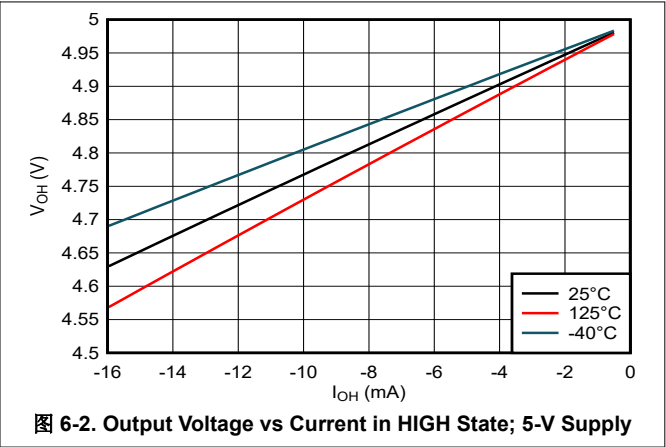
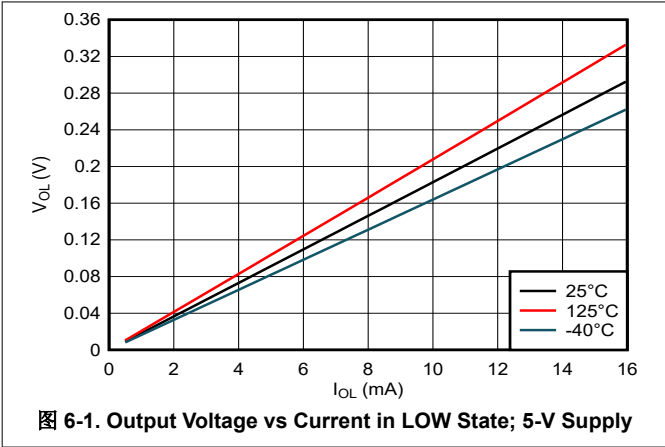
(1) Characteristics for surface-mount packages only.

6.13 Operating Characteristics

T<sub>A</sub> = 25°C

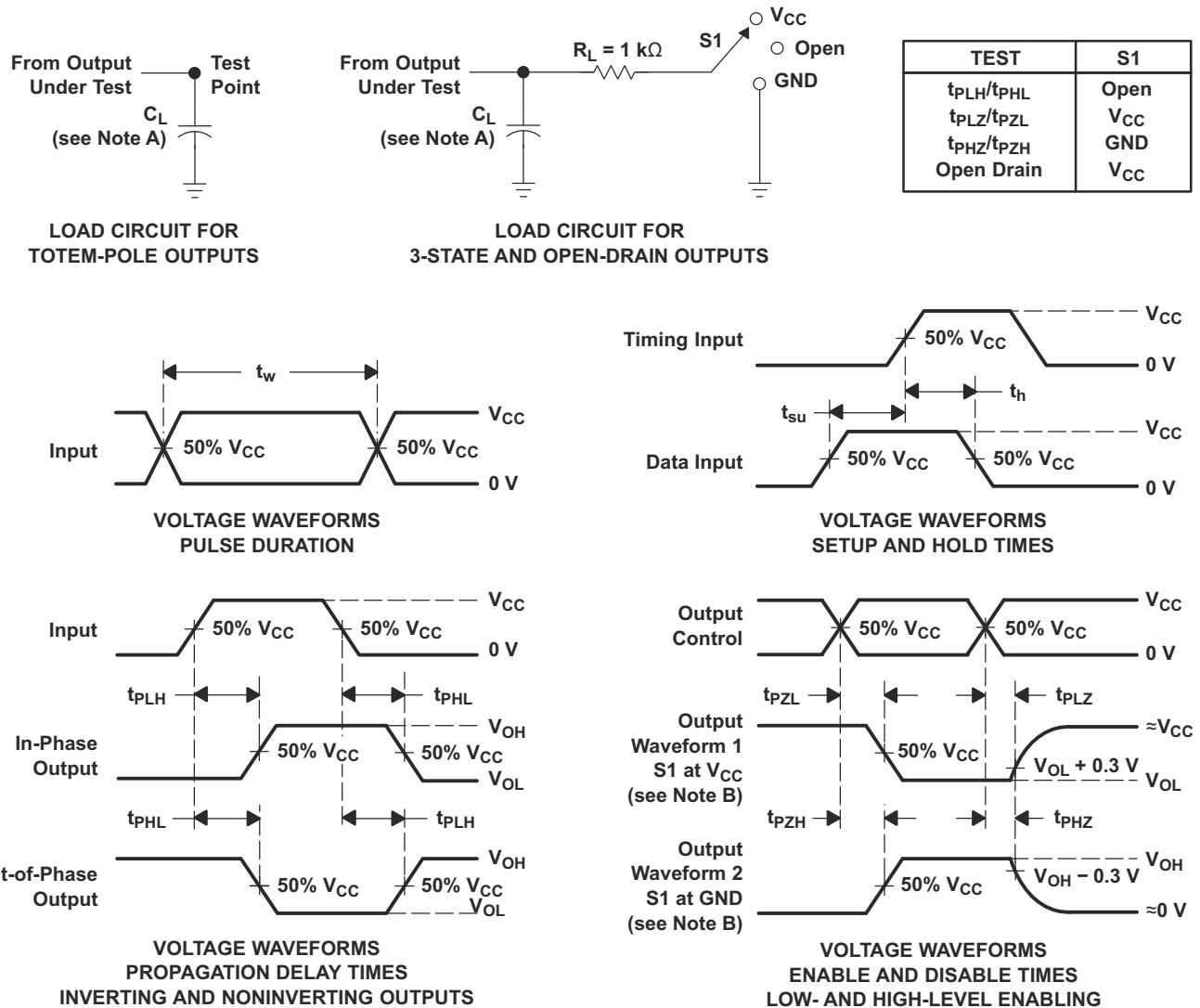
PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF    f = 10 MHz	3.3 V	36.1	pF
			5 V	37.5	

6.14 Typical Characteristics





## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ , and  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

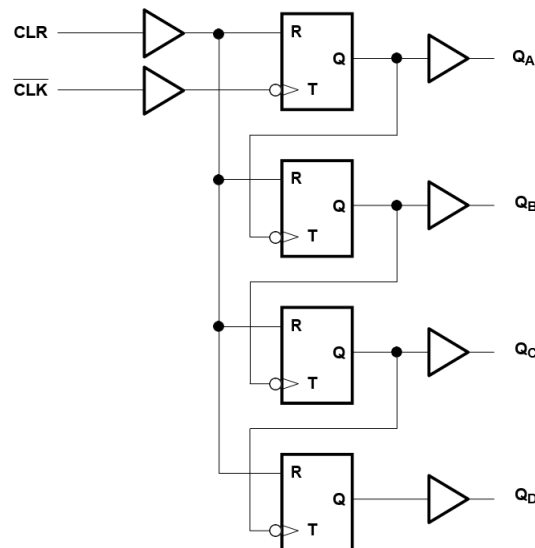
## 8 Detailed Description

### 8.1 Overview

The SN74LV393B-EP contains two independent 4-bit binary counters, each having a clear (CLR) and a clock ( $\overline{\text{CLK}}$ ) input. These devices change state on the negative-going transition of the  $\overline{\text{CLK}}$  pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The SN74LV393B-EP has parallel outputs from each counter stage so that any sub multiple of the input count frequency is available for system timing signals.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

### 8.3.3 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.4 Clamp Diode Structure

图 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

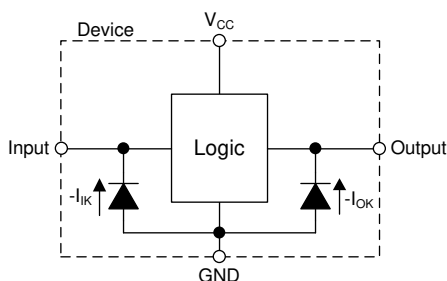


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV393B-EP.

表 8-1. Operating Mode Table

INPUTS		FUNCTION <sup>(1)</sup>
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, ↑ = Low to High transition

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV393B-EP is a dual 4-bit binary counter that can be used to create extended clock systems for controllers. Using a single CLK input and CLR signal, the device can output multiples of 2. Both counter banks can also be combined to divide the CLK signal by a factor of 256.

### 9.2 Typical Application

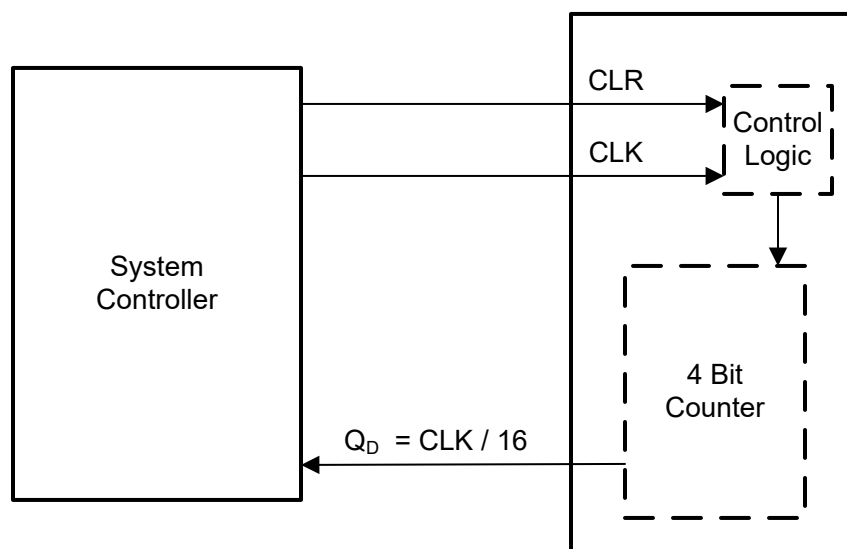


图 9-1. System Clock Divider

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV393B-EP plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV393B-EP plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV393B-EP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV393B-EP can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV393B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k  $\Omega$  resistor value is often used due to these factors.

The SN74LV393B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV393B-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , which will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.5 Application Curves

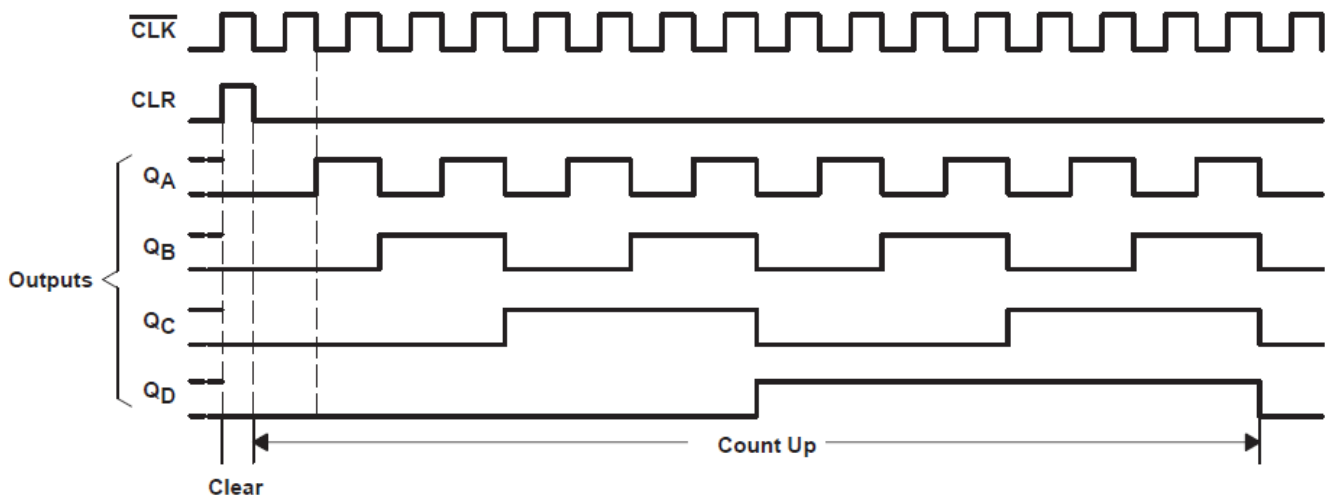


图 9-2. Application Timing Diagram

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a  $0.1\text{-}\mu\text{F}$  capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a  $0.01\text{-}\mu\text{F}$  or  $0.022\text{-}\mu\text{F}$  capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of  $0.1\text{ }\mu\text{F}$  and  $1\text{ }\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example

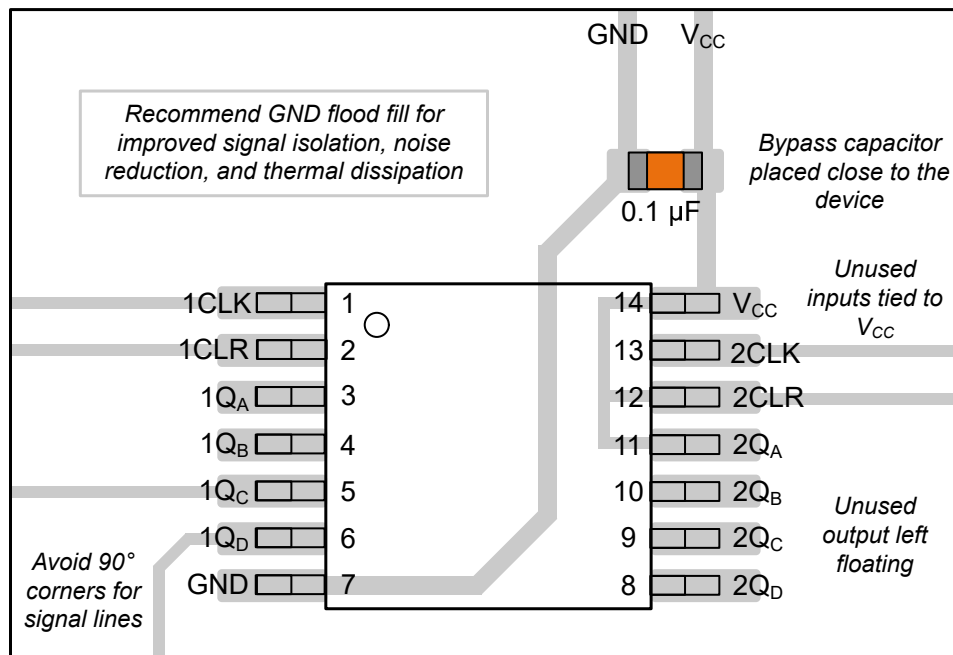


图 9-3. Layout Example for the SN74LV393B-EP in the PW Package

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Power-Up Behavior of Clocked Devices](#)
- Texas Instruments, [Introduction to Logic](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](https://www.ti.com). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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### 10.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LV393BMPWREP</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV393EP
SN74LV393BMPWREP.A	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV393EP
<a href="#">V62/23624-01XE</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN74LV393BMPWREP	LV393EP

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**PW0014A**

## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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