

## SN74LV138A-Q1 汽车类 3 线至 8 线解码器或多路解复用器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：-40°C 至 +125°C， $T_A$
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 在 2V 至 5.5V  $V_{CC}$  下运行
- 5V 时  $t_{pd}$  最大值为 9.5ns
- $V_{OLP}$  (输出接地反弹) 典型值  
小于 0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值  
大于 2.3V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- 支持所有端口上的混合模式电压运行
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

## 2 应用

- 输出扩展
- LED 矩阵控制
- 7 段显示控制
- 8 位数据存储

## 3 说明

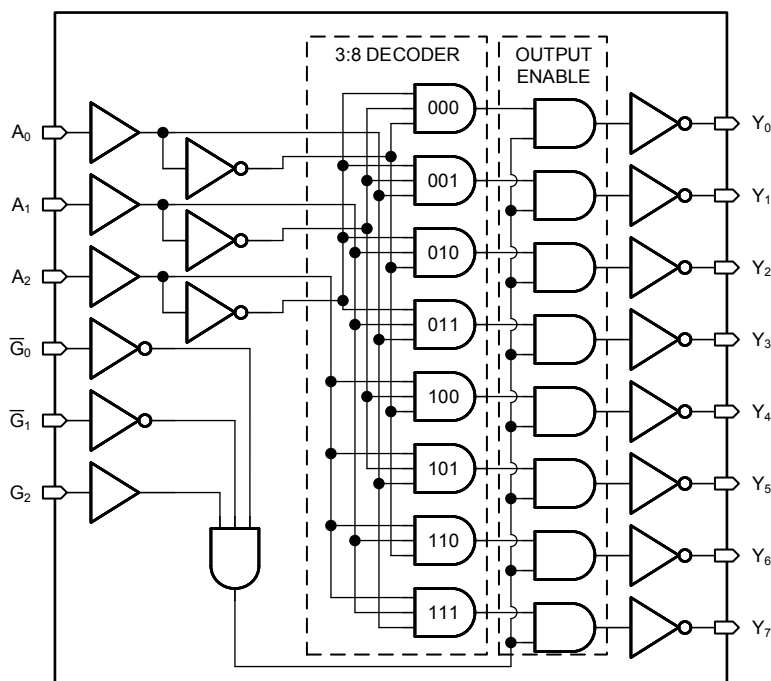
SN74LV138A-Q1 器件是旨在 2V 至 5.5V  $V_{CC}$  下运行的 3 线至 8 线解码器/多路解复用器。

二进制选择输入 ( $A_0$ 、 $A_1$ 、 $A_2$ ) 和三个使能输入 ( $G_2$ 、 $\overline{G_0}$ 、 $\overline{G_1}$ ) 条件可从八条输出线路中选择其中一条。两个低电平有效使能输入 ( $\overline{G_0}$ 、 $\overline{G_1}$ ) 和一个高电平有效使能输入 ( $G_2$ ) 可在扩展时减少对外部门电路或反相器的需求。

## 器件信息

| 器件型号          | 封装 <sup>(1)</sup> | 封装尺寸            |
|---------------|-------------------|-----------------|
| SN74LV138A-Q1 | BQB (WQFN, 16)    | 3.60mm × 2.60mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)



## Table of Contents

|                                                                                 |          |                                                                  |           |
|---------------------------------------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特性</b> .....                                                               | <b>1</b> | <b>8.2 Functional Block Diagram</b> .....                        | <b>9</b>  |
| <b>2 应用</b> .....                                                               | <b>1</b> | <b>8.3 Feature Description</b> .....                             | <b>9</b>  |
| <b>3 说明</b> .....                                                               | <b>1</b> | <b>8.4 Device Functional Modes</b> .....                         | <b>11</b> |
| <b>4 Revision History</b> .....                                                 | <b>2</b> | <b>9 Application and Implementation</b> .....                    | <b>12</b> |
| <b>5 Pin Configuration and Functions</b> .....                                  | <b>3</b> | 9.1 Application Information.....                                 | 12        |
| <b>6 Specifications</b> .....                                                   | <b>4</b> | 9.2 Typical Application.....                                     | 12        |
| 6.1 Absolute Maximum Ratings.....                                               | 4        | <b>10 Power Supply Recommendations</b> .....                     | <b>15</b> |
| 6.2 ESD Ratings.....                                                            | 4        | <b>11 Layout</b> .....                                           | <b>16</b> |
| 6.3 Recommended Operating Conditions <sup>(1)</sup> .....                       | 5        | 11.1 Layout Guidelines.....                                      | 16        |
| 6.4 Thermal Information.....                                                    | 5        | 11.2 Layout Example.....                                         | 16        |
| 6.5 Electrical Characteristics.....                                             | 6        | <b>12 Device and Documentation Support</b> .....                 | <b>17</b> |
| 6.6 Switching Characteristics - $V_{CC} = 2.5\text{ V} \pm 0.25\text{ V}$ ..... | 6        | 12.1 接收文档更新通知.....                                               | 17        |
| 6.7 Switching Characteristics - $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....  | 6        | 12.2 支持资源.....                                                   | 17        |
| 6.8 Switching Characteristics - $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....    | 7        | 12.3 Trademarks.....                                             | 17        |
| 6.9 Operating Characteristics.....                                              | 7        | 12.4 Electrostatic Discharge Caution.....                        | 17        |
| 6.10 Typical Characteristics.....                                               | 7        | 12.5 术语表.....                                                    | 17        |
| <b>7 Parameter Measurement Information</b> .....                                | <b>8</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>18</b> |
| <b>8 Detailed Description</b> .....                                             | <b>9</b> |                                                                  |           |
| 8.1 Overview.....                                                               | 9        |                                                                  |           |

## 4 Revision History

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| December 2022 | *        | Initial Release |

## 5 Pin Configuration and Functions

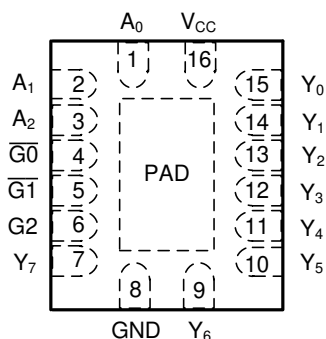


图 5-1. BQB Package 16-Pin (Top View)

表 5-1. Pin Functions

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                |
|-----------------|-----|---------------------|----------------------------|
| NAME            | NO. |                     |                            |
| A <sub>0</sub>  | 1   | I                   | Address select 0           |
| A <sub>1</sub>  | 2   | I                   | Address select 1           |
| A <sub>2</sub>  | 3   | I                   | Address select 2           |
| G2              | 6   | I                   | Strobe input               |
| $\overline{G0}$ | 4   | I                   | Strobe input, active low   |
| $\overline{G1}$ | 5   | I                   | Strobe input, active low   |
| GND             | 8   | G                   | Ground                     |
| V <sub>CC</sub> | 16  | P                   | Positive supply            |
| Y <sub>0</sub>  | 15  | O                   | Output 0                   |
| Y <sub>1</sub>  | 14  | O                   | Output 1                   |
| Y <sub>2</sub>  | 13  | O                   | Output 2                   |
| Y <sub>3</sub>  | 12  | O                   | Output 3                   |
| Y <sub>4</sub>  | 11  | O                   | Output 4                   |
| Y <sub>5</sub>  | 10  | O                   | Output 5                   |
| Y <sub>6</sub>  | 9   | O                   | Output 6                   |
| Y <sub>7</sub>  | 7   | O                   | Output 7                   |
| Thermal Pad     |     | -                   | Thermal Pad <sup>(2)</sup> |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

(2) BQB package only

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                                                                             | MIN                                   | MAX                   | UNIT    |
|------------------|---------------------------------------------------------------------------------------------|---------------------------------------|-----------------------|---------|
| V <sub>CC</sub>  | Supply voltage range                                                                        | - 0.5                                 | 7                     | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                          | - 0.5                                 | 7                     | V       |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | - 0.5                                 | 7                     | V       |
| V <sub>O</sub>   | Output voltage range <sup>(2) (3)</sup>                                                     | - 0.5                                 | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0                    |                       | - 20 mA |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0                    |                       | - 50 mA |
| I <sub>O</sub>   | Continuous output current                                                                   | V <sub>O</sub> = 0 to V <sub>CC</sub> |                       | ±25 mA  |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                                       |                       | ±50 mA  |
| T <sub>stg</sub> | Storage temperature range                                                                   | - 65                                  | 150                   | °C      |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                                  | UNIT  |
|--------------------|-------------------------|----------------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup> | ±2000 |
|                    |                         | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B          | ±1000 |

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions<sup>(1)</sup>

|                 |                                    | SN74LV138A-Q1                    |                       | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|------|
|                 |                                    | MIN                              | MAX                   |      |
| V <sub>CC</sub> | Supply voltage                     | 2                                | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            | 0.5                   | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 |      |
| V <sub>I</sub>  | Input voltage                      | 0                                | 5.5                   | V    |
| V <sub>O</sub>  | Output voltage                     | 0                                | V <sub>CC</sub>       | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            | – 50                  | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | – 2                   | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | – 6                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | – 12                  |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            | 50                    | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | 2                     | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 6                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 12                    |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V | 200                   | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 100                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 20                    |      |
| T <sub>A</sub>  | Operating free-air temperature     | – 40                             | 125                   | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LV138A-Q1 | UNIT |
|-------------------------------|----------------------------------------------|---------------|------|
|                               |                                              | WBQB (WQFN)   |      |
|                               |                                              | 16 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 86            | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 82.6          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 54.9          | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 9.5           | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 54.9          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 32.5          | °C/W |

(1) For more information about traditional and new thermal metrics, see [IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                               |                                                             | TEST CONDITIONS | V <sub>CC</sub>       | SN74LV138A-Q1 |     |     | UNIT |
|---------------------------------------------------------|-------------------------------------------------------------|-----------------|-----------------------|---------------|-----|-----|------|
|                                                         |                                                             |                 |                       | MIN           | TYP | MAX |      |
| V <sub>OH</sub> High-Level Output Voltage               | I <sub>OH</sub> = - 50   μ A                                | 2 V to 5.5 V    | V <sub>CC</sub> - 0.1 |               |     | V   |      |
|                                                         | I <sub>OH</sub> = - 2 mA                                    | 2.3 V           | 2                     |               |     |     |      |
|                                                         | I <sub>OH</sub> = - 6 mA                                    | 3 V             | 2.48                  |               |     |     |      |
|                                                         | I <sub>OH</sub> = - 12 mA                                   | 4.5 V           | 3.8                   |               |     |     |      |
| V <sub>OL</sub> Low-Level Output Voltage                | I <sub>OL</sub> = 50   μ A                                  | 2 V to 5.5 V    | 0.1                   |               |     | V   |      |
|                                                         | I <sub>OL</sub> = 2 mA                                      | 2.3 V           | 0.4                   |               |     |     |      |
|                                                         | I <sub>OL</sub> = 6 mA                                      | 3 V             | 0.44                  |               |     |     |      |
|                                                         | I <sub>OL</sub> = 12 mA                                     | 4.5 V           | 0.55                  |               |     |     |      |
| I <sub>I</sub> Input Current                            | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      | ±1                    |               |     | μ A |      |
| I <sub>CC</sub> Supply Current                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 20                    |               |     | μ A |      |
| I <sub>off</sub> Input/Output Power-Off Leakage Current | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               | 5                     |               |     | μ A |      |
| C <sub>i</sub> Input Capacitance                        | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V           | 2.1                   |               |     | pF  |      |

## 6.6 Switching Characteristics - V<sub>CC</sub> = 2.5 V $\pm$ 0.25 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER       | FROM<br>(INPUT)                                  | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |      |     | SN74LV138A-Q1 |     | UNIT |
|-----------------|--------------------------------------------------|----------------|------------------------|-----------------------|------|-----|---------------|-----|------|
|                 |                                                  |                |                        | MIN                   | TYP  | MAX | MIN           | MAX |      |
| t <sub>pd</sub> | A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Y              | C <sub>L</sub> = 15 pF | 11.7                  | 17.6 | 1   | 21            | ns  |      |
|                 | G2                                               |                |                        | 12.3                  | 19.2 | 1   | 22            |     |      |
|                 | $\overline{G0}$ or $\overline{G1}$               |                |                        | 11.4                  | 18.2 | 1   | 21            |     |      |
| t <sub>pd</sub> | A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Y              | C <sub>L</sub> = 50 pF | 14.9                  | 21.4 | 1   | 25            | ns  |      |
|                 | G2                                               |                |                        | 15.7                  | 22.6 | 1   | 26            |     |      |
|                 | $\overline{G0}$ or $\overline{G1}$               |                |                        | 14.8                  | 22   | 1   | 25            |     |      |

## 6.7 Switching Characteristics - V<sub>CC</sub> = 3.3 V $\pm$ 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER       | FROM<br>(INPUT)                                  | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |      |     | SN74LV138A-Q1 | UNIT |
|-----------------|--------------------------------------------------|----------------|------------------------|-----------------------|------|-----|---------------|------|
|                 |                                                  |                |                        | MIN                   | TYP  | MAX | MIN           |      |
| t <sub>pd</sub> | A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Y              | C <sub>L</sub> = 15 pF | 8.1                   | 11.4 | 1   | 13.5          | ns   |
|                 | G2                                               |                |                        | 8.4                   | 12.8 | 1   | 15            |      |
|                 | $\overline{G0}$ or $\overline{G1}$               |                |                        | 7.8                   | 11.4 | 1   | 13.5          |      |
| t <sub>pd</sub> | A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Y              | C <sub>L</sub> = 50 pF | 10.3                  | 15.8 | 1   | 18            | ns   |
|                 | G2                                               |                |                        | 10.6                  | 16.3 | 1   | 18.5          |      |
|                 | $\overline{G0}$ or $\overline{G1}$               |                |                        | 10                    | 14.9 | 1   | 17            |      |

## 6.8 Switching Characteristics - $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM<br>(INPUT)                    | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |      | SN74LV138A-Q1 |      | UNIT |
|-----------|------------------------------------|----------------|----------------------|--------------------------|-----|------|---------------|------|------|
|           |                                    |                |                      | MIN                      | TYP | MAX  | MIN           | MAX  |      |
| $t_{pd}$  | $A_0, A_1, A_2$                    | Y              | $C_L = 15\text{ pF}$ |                          | 5.6 | 8.1  | 1             | 9.5  | ns   |
|           | G2                                 |                |                      |                          | 5.7 | 8.1  | 1             | 9.5  |      |
|           | $\overline{G0}$ or $\overline{G1}$ |                |                      |                          | 5.4 | 8.1  | 1             | 9.5  |      |
| $t_{pd}$  | $A_0, A_1, A_2$                    | Y              | $C_L = 50\text{ pF}$ |                          | 7   | 10.1 | 1             | 11.5 | ns   |
|           | G2                                 |                |                      |                          | 7.1 | 10.1 | 1             | 11.5 |      |
|           | $\overline{G0}$ or $\overline{G1}$ |                |                      |                          | 6.8 | 10.1 | 1             | 11.5 |      |

## 6.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS                         | $V_{CC}$ | TYP  | UNIT |
|-----------|-------------------------------|-----------------------------------------|----------|------|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}, f = 10\text{ MHz}$ | 3.3 V    | 16.8 | pF   |
|           |                               |                                         | 5 V      | 19.1 |      |

## 6.10 Typical Characteristics

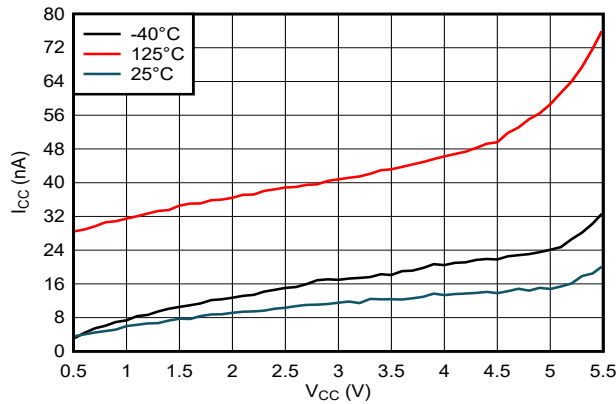


图 6-1. Supply Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ )

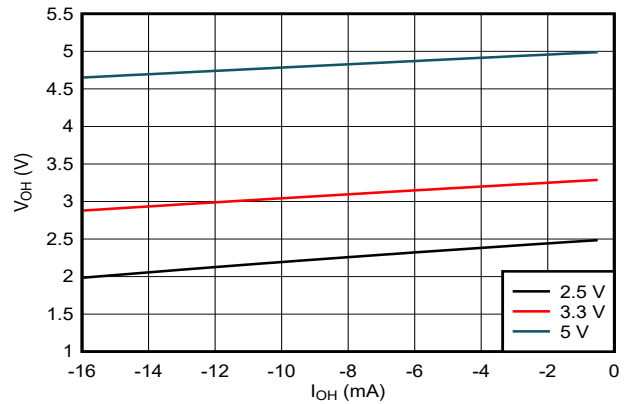


图 6-2. Output Voltage vs Current in HIGH State

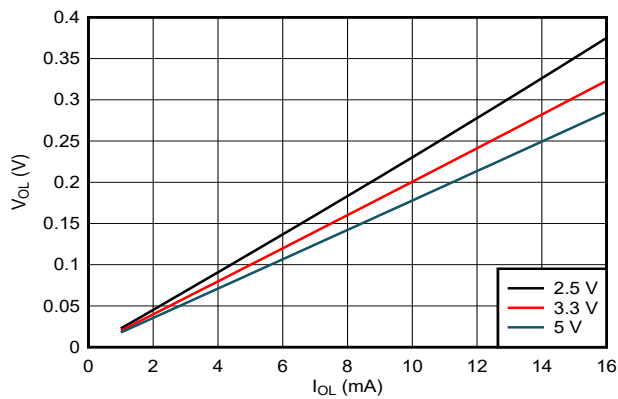
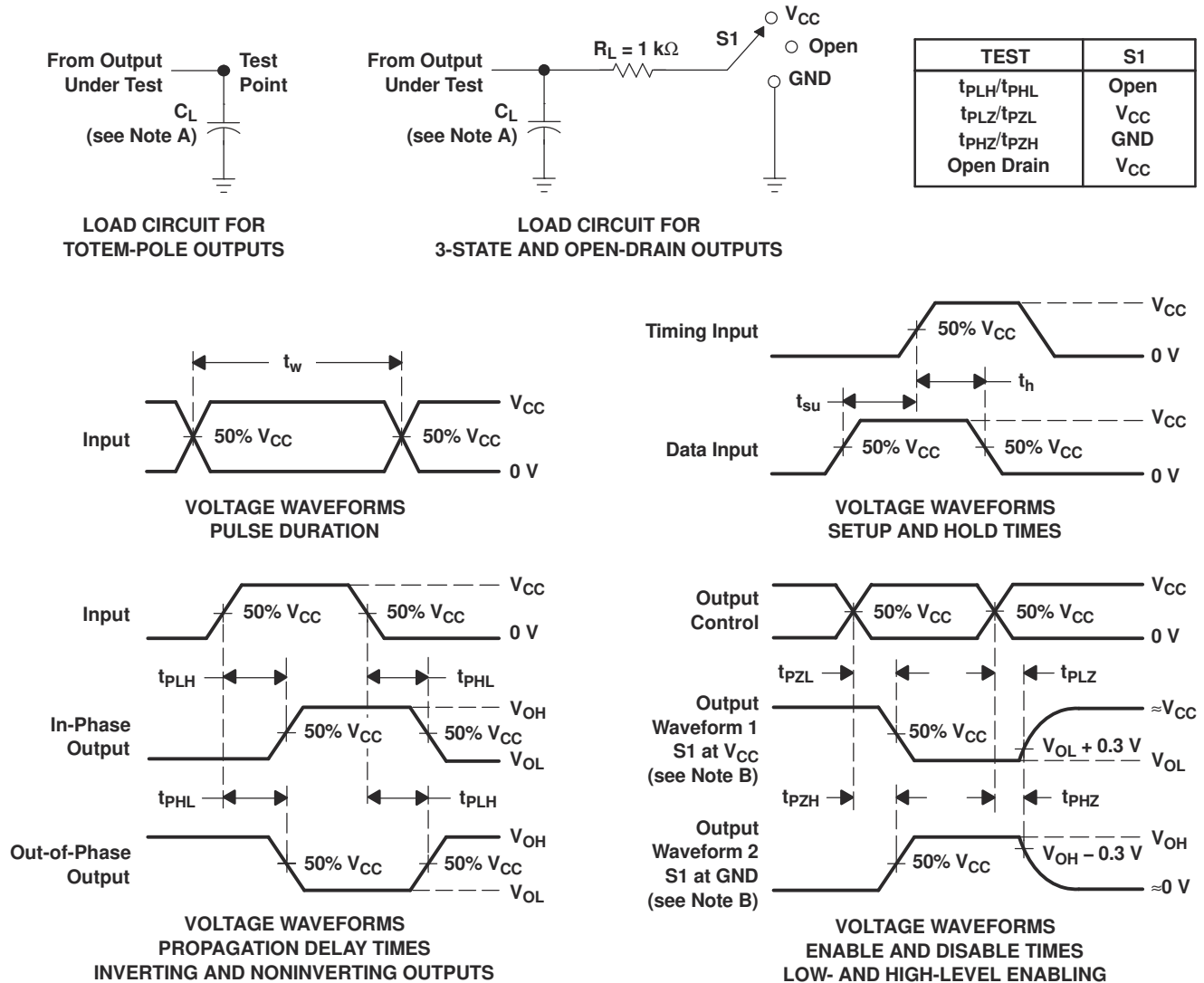


图 6-3. Output Voltage vs Current in LOW State

## 7 Parameter Measurement Information



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**图 7-1. Load Circuits and Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

The SN74LV138A-Q1 devices are 3-line to 8-line decoders/demultiplexers designed for 2 V to 5.5 V  $V_{CC}$  operation.

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and the three enable inputs ( $G_2$ ,  $\overline{G_0}$ ,  $\overline{G_1}$ ) select one of eight output lines. The two active-low ( $\overline{G_0}$ ,  $\overline{G_1}$ ) and one active-high ( $G_2$ ) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

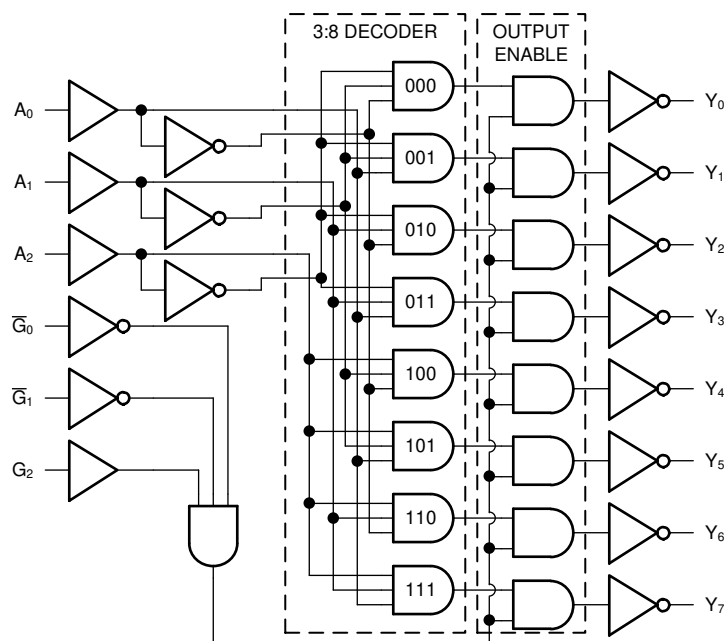


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

#### 8.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

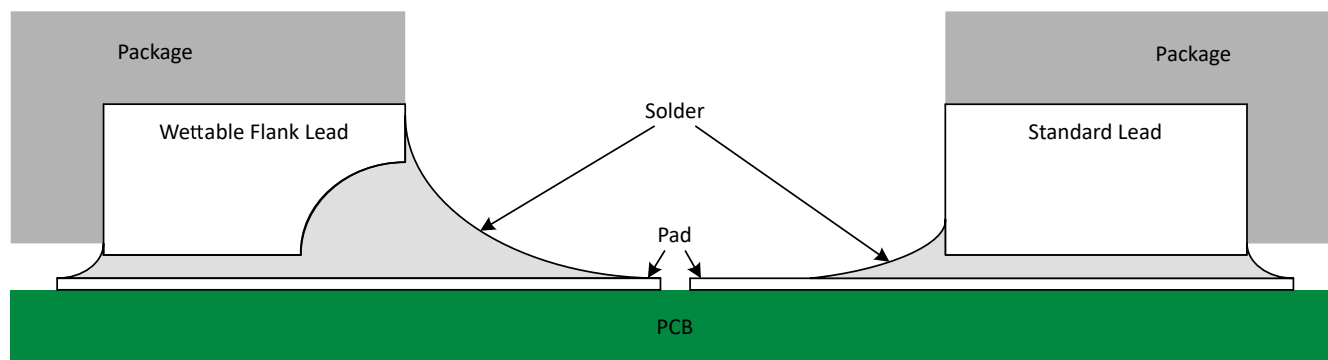
Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.



**图 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 8-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### 8.3.5 Clamp Diode Structure

图 8-3 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

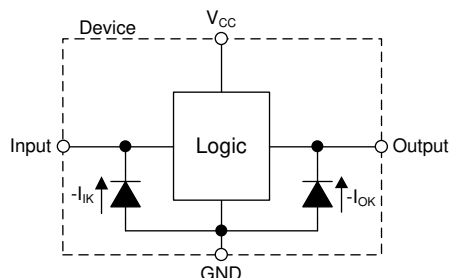


图 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

Function Table

| ENABLE INPUTS <sup>(1)</sup> |    |    | SELECT INPUTS  |                |                | OUTPUTS <sup>(2)</sup> |    |     |    |    |    |    |    |
|------------------------------|----|----|----------------|----------------|----------------|------------------------|----|-----|----|----|----|----|----|
| G2                           | G0 | G1 | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | Y0                     | Y1 | Y20 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X                            | H  | X  | X              | X              | X              | H                      | H  | H   | H  | H  | H  | H  | H  |
| X                            | X  | H  | X              | X              | X              | H                      | H  | H   | H  | H  | H  | H  | H  |
| L                            | X  | X  | X              | X              | X              | H                      | H  | H   | H  | H  | H  | H  | H  |
| H                            | L  | L  | L              | L              | L              | L                      | H  | H   | H  | H  | H  | H  | H  |
| H                            | L  | L  | L              | L              | H              | H                      | L  | H   | H  | H  | H  | H  | H  |
| H                            | L  | L  | L              | H              | L              | H                      | H  | L   | H  | H  | H  | H  | H  |
| H                            | L  | L  | L              | H              | H              | H                      | H  | H   | L  | H  | H  | H  | H  |
| H                            | L  | L  | H              | L              | L              | H                      | H  | H   | H  | L  | H  | H  | H  |
| H                            | L  | L  | H              | L              | H              | H                      | H  | H   | H  | H  | L  | H  | H  |
| H                            | L  | L  | H              | H              | L              | H                      | H  | H   | H  | H  | H  | L  | H  |
| H                            | L  | L  | H              | H              | H              | H                      | H  | H   | H  | H  | H  | H  | L  |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The SN74LV138A-Q1 is a low drive CMOS device that can be used for a multitude of output expansion applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

### 9.2 Typical Application

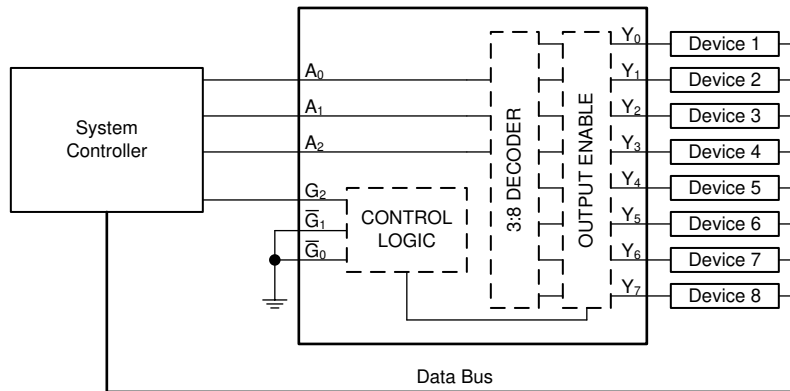


图 9-1. Output Exapnsion with Multiplexer

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV138A-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV138A-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV138A-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV138A-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV138A-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k  $\Omega$  resistor value is often used due to these factors.

The SN74LV138A-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV138A-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.5 Application Curves

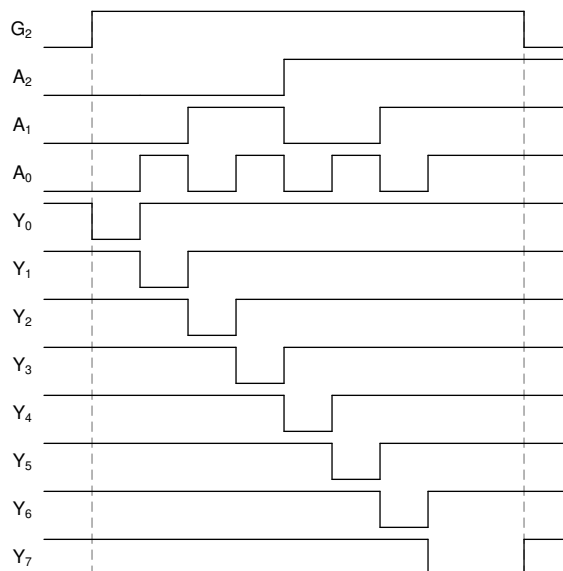


图 9-2. Application Timing Diagram

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

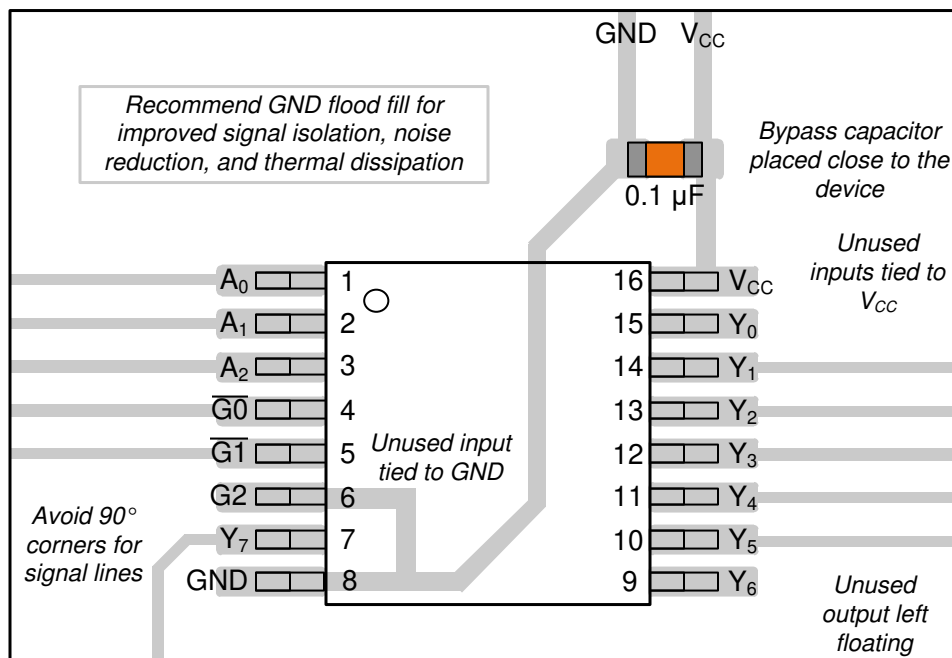


图 11-1. Layout Example for the SN74LV138A-Q1



## 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LV138AQWBQBRQ1</a> | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LV138Q              |
| SN74LV138AQWBQBRQ1.A               | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LV138Q              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF SN74LV138A-Q1 :

- Catalog : [SN74LV138A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## GENERIC PACKAGE VIEW

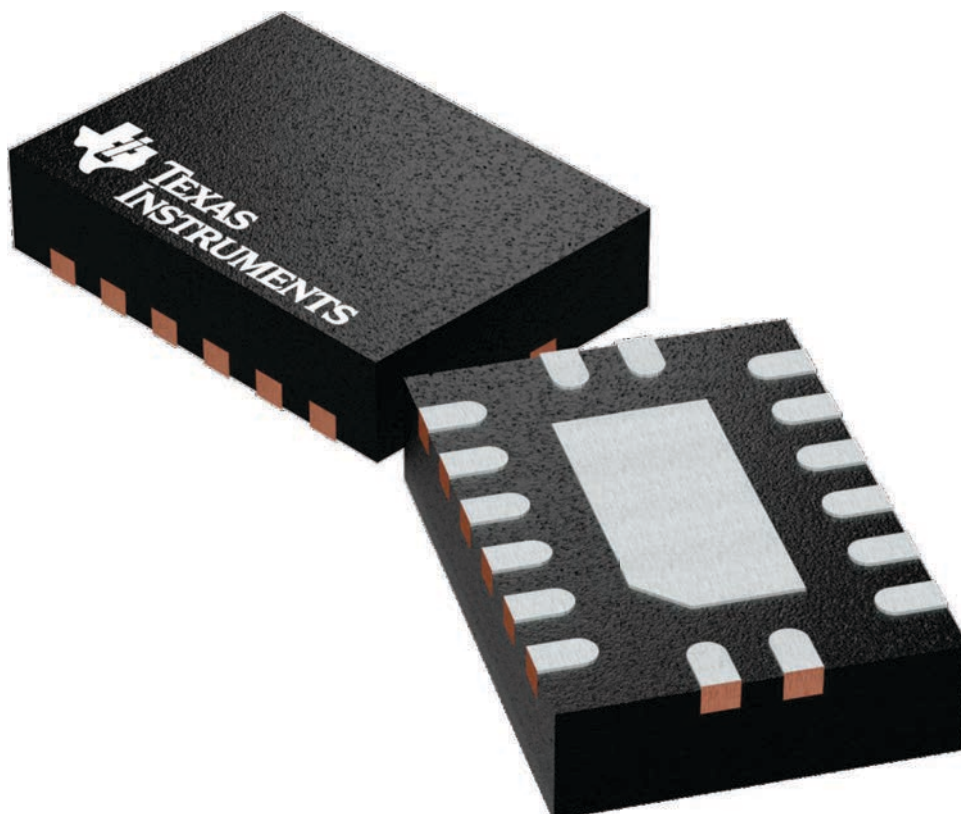
**BQB 16**

**WQFN - 0.8 mm max height**

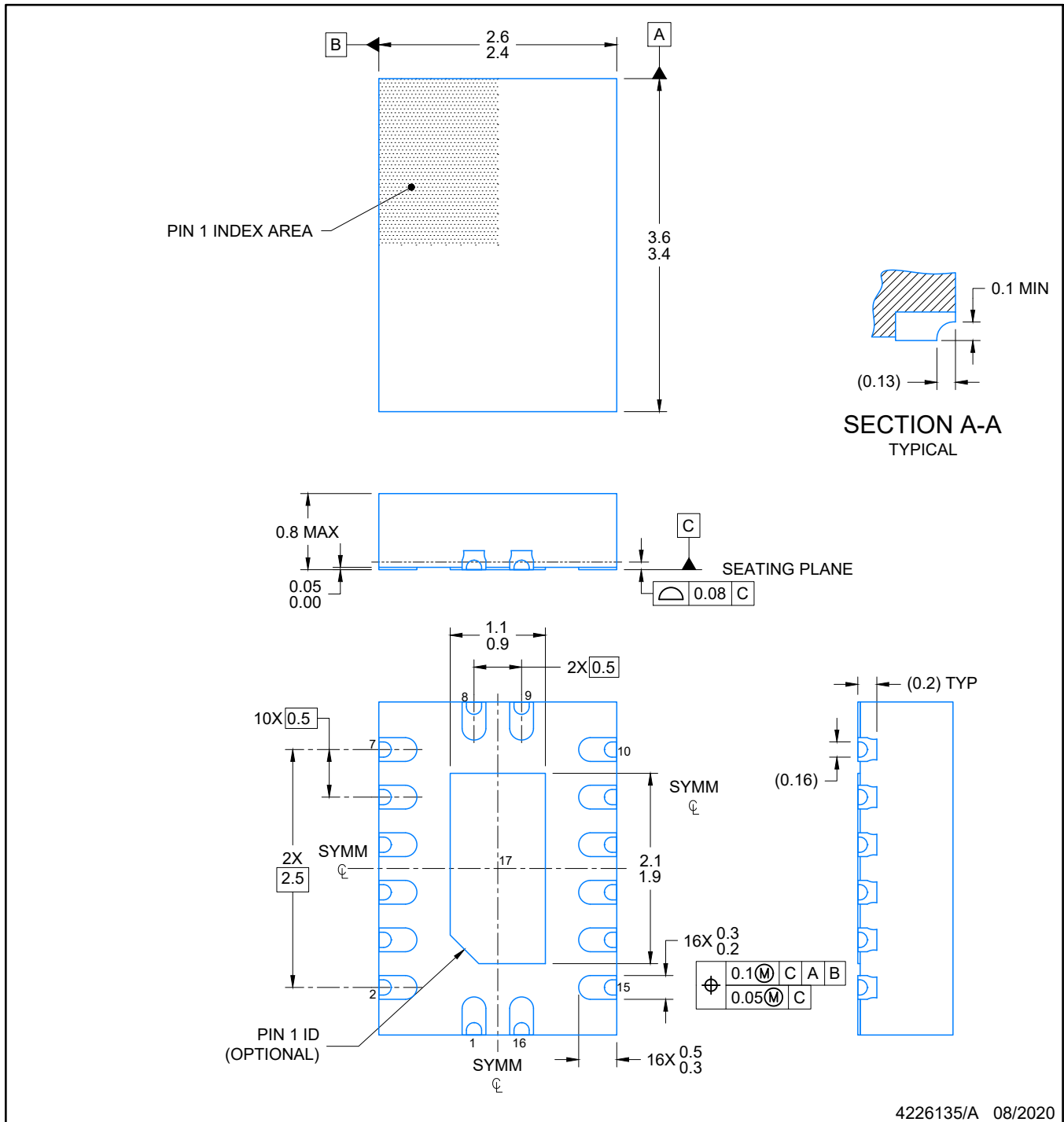
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

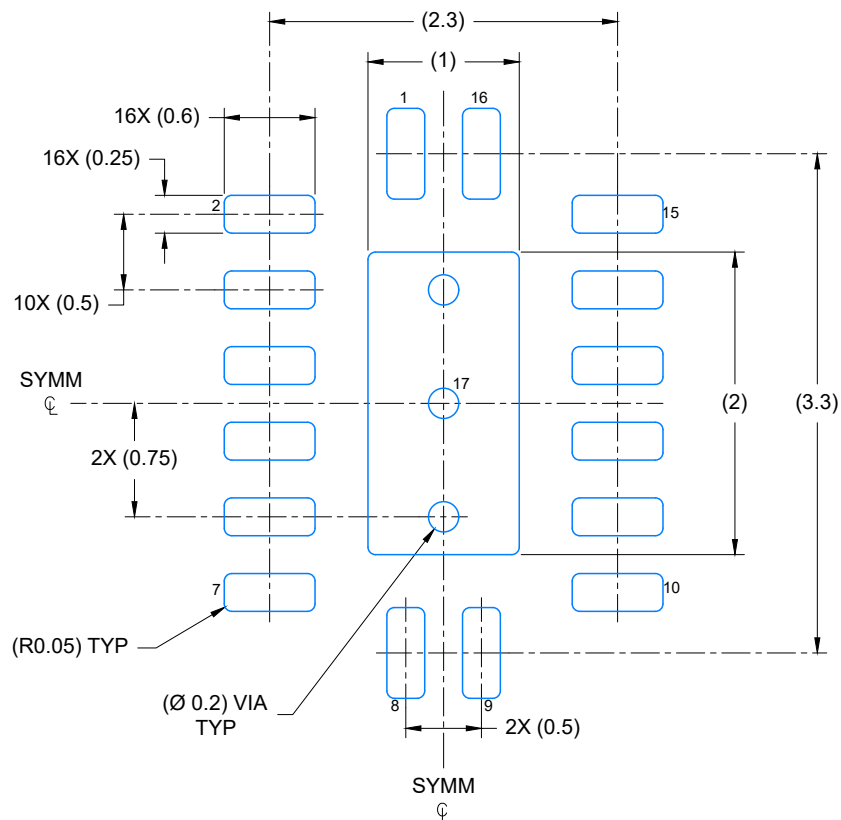


4226161/A



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

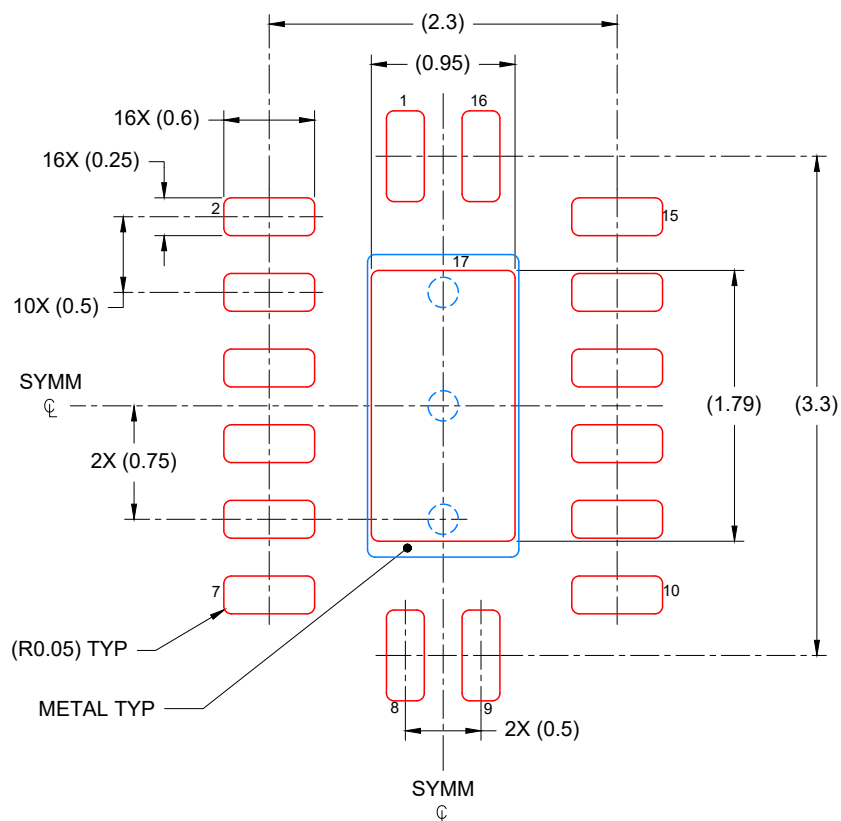


LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

4226135/A 08/2020

## NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
85% PRINTED COVERAGE BY AREA  
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司