SN74LV123A-Q1 Dual Retriggerable Monostable Multivibrator With Schmitt-Trigger Inputs

1 Features

- Qualified for Automotive Applications
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Automotive
- Infotainment Systems
- DVD and Blu-ray Players
- GPS Navigation Devices
- Advanced Driver Assistance Systems
- Automotive Body and Lighting

3 Description

The SN74LV123A-Q1 device is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V V_{CC} operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV123A-Q1	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram, Each Multivibrator (Positive Logic)

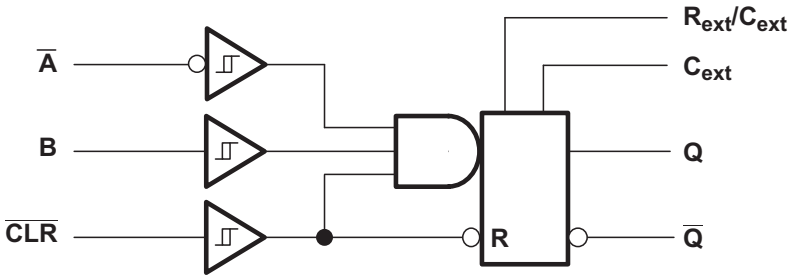


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2012) to Revision F — **Page**

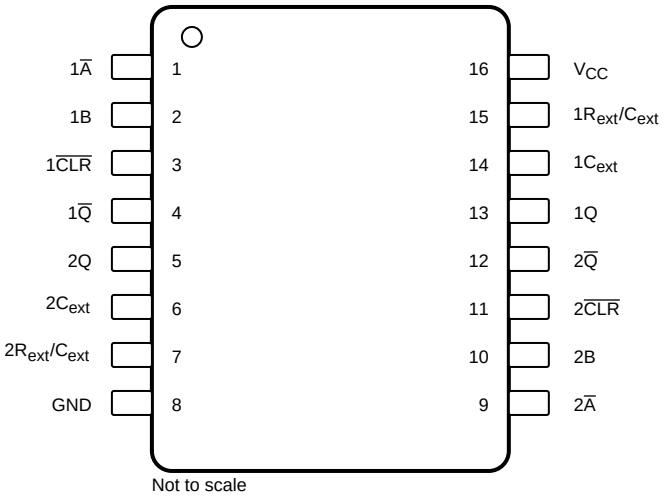
- Deleted 200-V Machine Model (A115-A) from *Features* ... 1
- Added 'Infotainment Systems' application. ... 1
- Added 'DVD and Blu-ray Players' application. ... 1
- Added 'GPS Navigation Devices' application. ... 1
- Added 'Advanced Driver Assistance Systems' application. ... 1
- Added 'Automotive Body and Lighting' application. ... 1
- Updated the data sheet to meet the new TI data sheet standard ... 1
- Deleted *Ordering Information* table from the data sheet ... 1
- Moved extraneous description details to *Overview* section ... 1
- Added *Device Information* table, *ESD Ratings* table, *Pin Configuration and Functions* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, *Receiving Notification of Documentation Updates* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added logic diagram for front page image ... 1
- Added Operating virtual junction temperature, T_J to *Absolute Maximum Ratings* table ... 4
- Changed Maximum Operating free-air temperature from 105 to 125 ... 5

Changes from Revision D (April 2008) to Revision E — **Page**

- Added *Thermal Information* table ... 5
- Added *Caution* section describing power-down timing ... 11

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1$\overline{A}$	I	Channel 1 falling edge trigger input when 1B = L; Hold low for other input methods
2	1B	I	Channel 1 rising edge trigger input when 1$\overline{A}$ = H; Hold high for other input methods
3	1$\overline{CLR}$	I	Channel 1 rising edge trigger when 1$\overline{A}$ = H and 1B = L; Hold high for other input methods; Can cut pulse length short by driving low during output
4	1$\overline{Q}$	O	Channel 1 inverted output
5	2Q	O	Channel 2 output
6	2C_{ext}	—	Channel 2 external capacitor negative connection
7	2R_{ext}/C_{ext}	—	Channel 2 external capacitor and resistor junction connection
8	GND	—	Ground
9	2$\overline{A}$	I	Channel 2 falling edge trigger input when 2B = L; Hold low for other input methods
10	2B	I	Channel 2 rising edge trigger input when 2$\overline{A}$ = H; Hold high for other input methods
11	2$\overline{CLR}$	I	Channel 2 rising edge trigger when 2$\overline{A}$ = H and 2B = L; Hold high for other input methods; Can cut pulse length short by driving low during output
12	2$\overline{Q}$	O	Channel 2 inverted output
13	1Q	O	Channel 1 output
14	1C_{ext}	—	Channel 1 external capacitor negative connection
15	1R_{ext}/C_{ext}	—	Channel 1 external capacitor and resistor junction connection
16	V_{CC}	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	7	V
Input voltage, V_I(2)		–0.5	7	V
Voltage range applied to any output in the high-impedance or power-off state, V_O(2)		–0.5	7	V
Output voltage, V_O V_O	In the high or low state(3)(2)	–0.5	V_{CC} + 0.5	V
	In the power-off state, V_O(2)	–0.5	7	V
Input clamp current, I_{IK}	V_I < 0		–20	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O	V_O = 0 to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Recommended Operating Conditions (continued)

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
R_{ext}	External timing resistance	V_{CC} = 2 V	5		kΩ
		V_{CC} ≥ 3 V	1		
C_{ext}	External timing capacitance		No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		ms/V
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV123A-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –50 μA	2 V to 5.5 V	0.1			V
			I_{OH} = –2 mA	2.3 V	2			
			I_{OH} = –6 mA	3 V	2.48			
			I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	Low-level output voltage		I_{OL} = 50 μA	2 V to 5.5 V			0.1	V
			I_{OL} = 2 mA	2.3 V			0.4	
			I_{OL} = 6 mA	3 V			0.44	
			I_{OL} = 12 mA	4.5 V			0.55	
I_I	Input current	R_{ext}/C_{ext}(1)	V_I = 5.5 V or GND	5.5 V			±2.5	μA
		$\overline{A}$, B, and $\overline{CLR}$	V_I = 5.5 V or GND	0 V			±1	
				0 to 5.5 V			±1	
I_{CC}	Quiescent current		V_I = V_{CC} or GND, I_O = 0	5.5 V			20	μA
I_{CC}	Supply current, Active state (per circuit)		V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V			280	μA
				4.5 V			650	
				5.5 V			975	
I_{off}	Off-state current		V_I or V_O = 0 to 5.5 V	0 V			5	μA
C_i	Input capacitance		V_I = V_{CC} or GND	3.3 V		1.9		pF
				5 V		1.9		

(1) This test is performed with the terminal in the off-state condition.

6.6 Timing Requirements — V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted). See Figure 1 and the circuits in the *Parameter Measurement Information* section.

			MIN	NOM(1)	MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$	5			ns
		$\overline{A}$ or B trigger	5			
t_{rr}	Pulse retrigger time, R_{ext} = 1 kΩ	C_{ext} = 100 pF	See(2)	76		ns
		C_{ext} = 0.01 µF	See(2)	1.8		µs

(1) T_A = 25°C
(2) See retriggering data in the *Application and Implementation* section.

6.7 Timing Requirements — V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted). See Figure 1 and the circuits in the *Parameter Measurement Information* section.

			MIN	NOM(1)	MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$	5			ns
		$\overline{A}$ or B trigger	5			
t_{rr}	Pulse retrigger time, R_{ext} = 1 kΩ	C_{ext} = 100 pF	See(2)	59		ns
		C_{ext} = 0.01 µF	See(2)	1.5		µs

(1) T_A = 25°C
(2) See retriggering data in the *Application and Implementation* section

6.8 Switching Characteristics — V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted). See the circuits in the *Parameter Measurement Information* section.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			T_A = –40 to +125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	Propagation delay	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		11.8	24.1	1	27.5	ns
		$\overline{CLR}$	Q or $\overline{Q}$			10.5	19.3	1	22	
		$\overline{CLR}$ trigger	Q or $\overline{Q}$			12.3	25.9	1	29.5	
t_w	Duration of pulse at Q and $\overline{Q}$ outputs		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		182	240		300	ns
				C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	µs
				C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	ms
Δt_w	Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package			C_L = 50 pF		±1%				

6.9 Switching Characteristics — V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted). See the circuits in the *Parameter Measurement Information* section.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			T_A = –40 to +125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	Propagation delay	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		8.3	14	1	16	ns
		$\overline{CLR}$	Q or $\overline{Q}$			7.4	11.4	1	13	
		$\overline{CLR}$ trigger	Q or $\overline{Q}$			8.7	14.9	1	17	
t_w	Duration of pulse at Q and $\overline{Q}$ outputs		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		167	200		240	ns
				C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	µs
				C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	ms
Δt_w	Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package			C_L = 50 pF		±1%				

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	44	pF
				5 V	49	

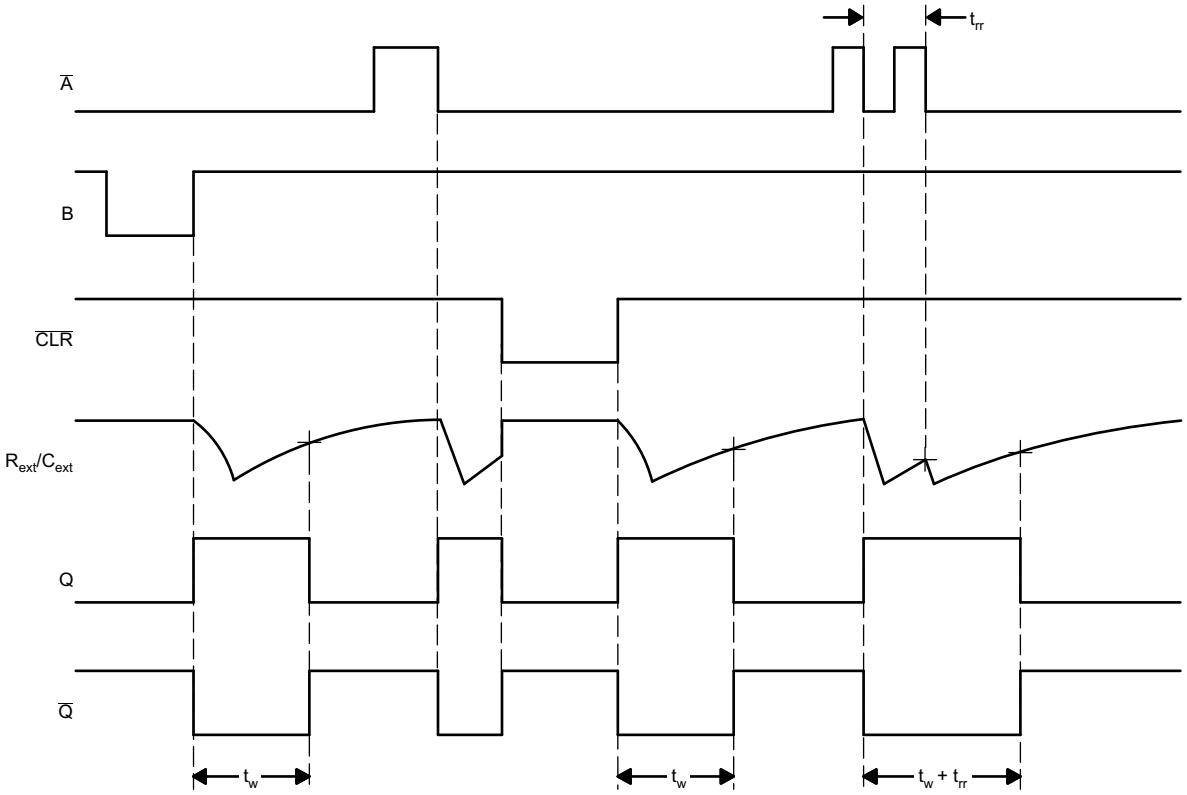


Figure 1. Input and Output (I/O) Timing Diagram

6.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.

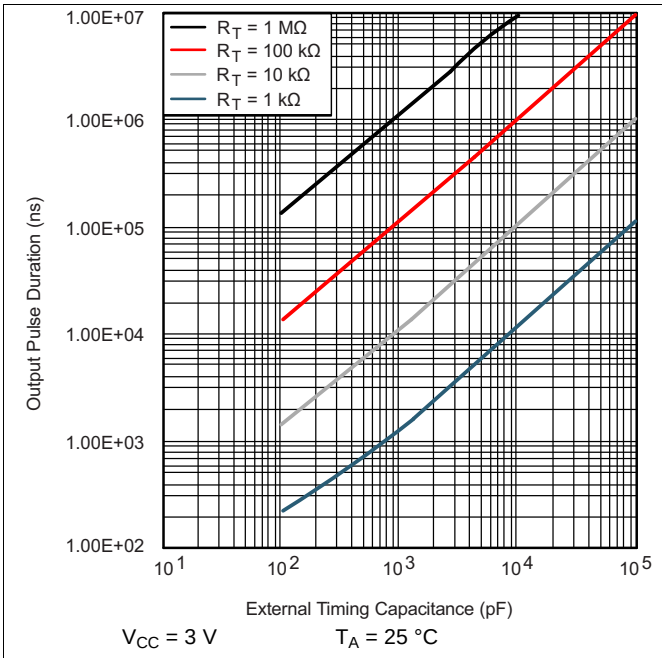


Figure 2. Output Pulse Duration (t_w) vs External Timing Capacitance (C_T)

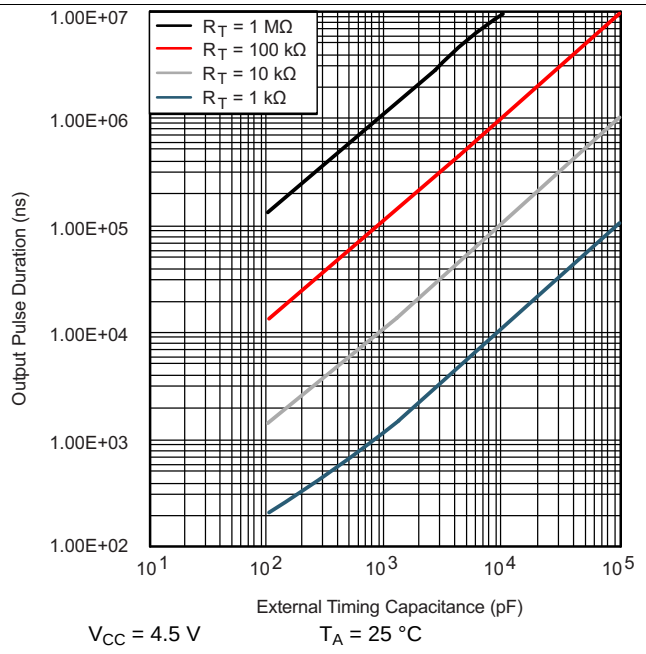


Figure 3. Output Pulse Duration vs External Timing Capacitance

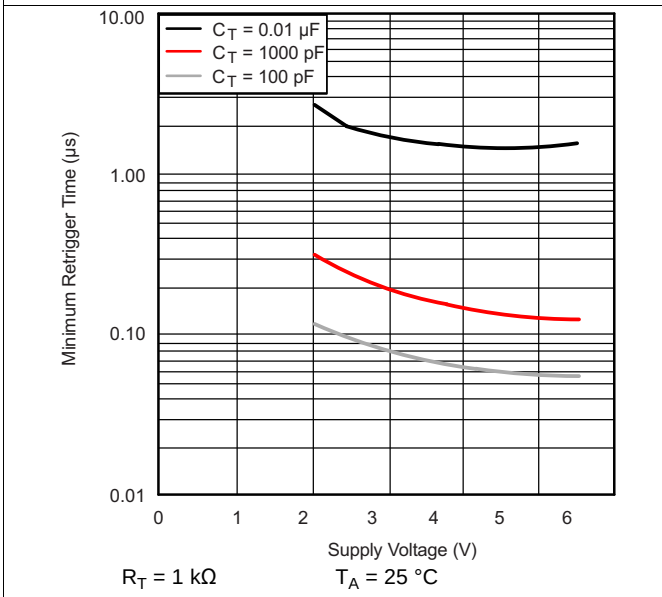


Figure 4. Minimum Trigger Time (t_{rr}) vs V_{CC} Characteristics

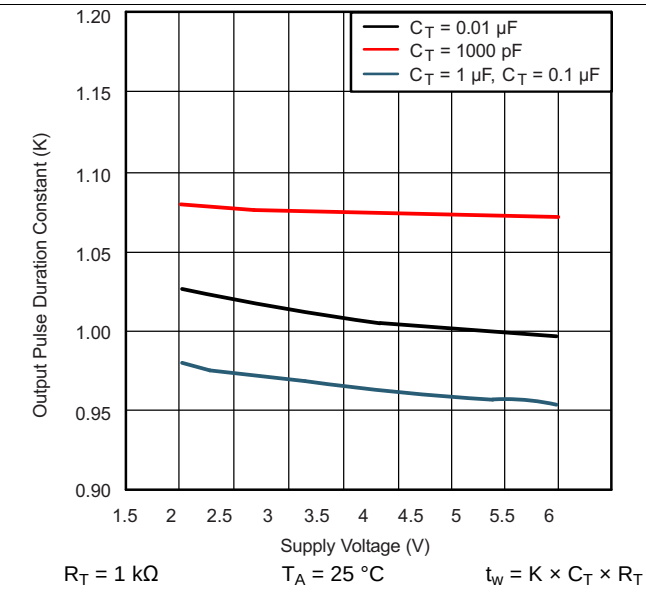


Figure 5. Output Pulse-Duration Constant vs Supply Voltage

7 Parameter Measurement Information

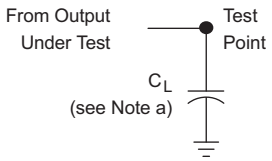


Figure 6. Load Circuit

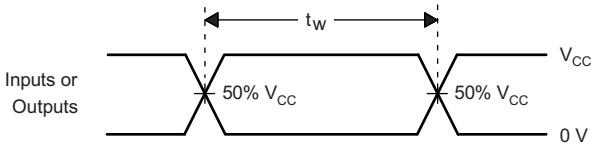


Figure 7. Voltage Waveforms Pulse Duration

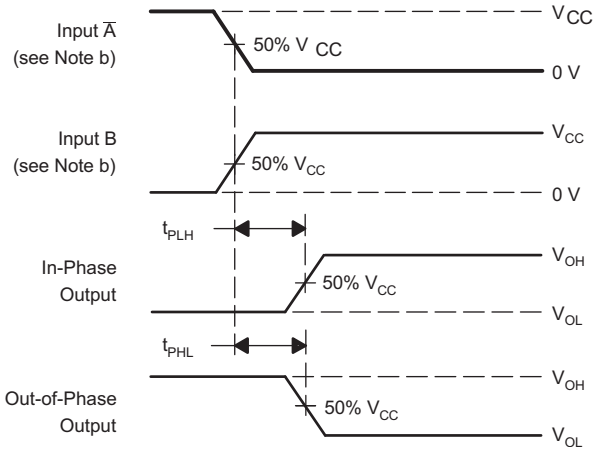


Figure 8. Voltage Waveforms Delay Times

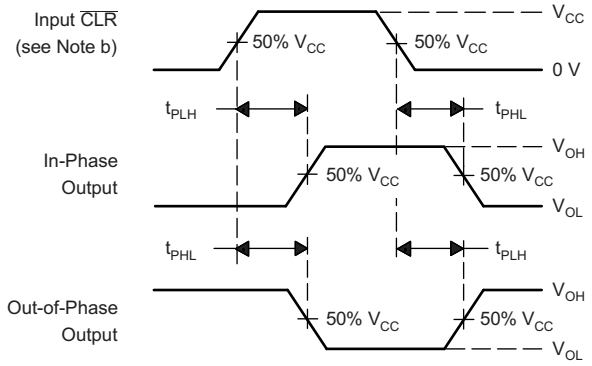


Figure 9. Voltage Waveforms Delay Times

a. C_L includes probe and jig capacitance.

b. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.

c. The outputs are measured one at a time, with one input transition per measurement.

8 Detailed Description

8.1 Overview

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. Connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} to obtain variable pulse durations. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

When triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration may be reduced by taking $\overline{CLR}$ low. The input-output timing diagram (Figure 1) shows pulse control by retriggering the inputs and early clearing.

The Q outputs are in the low state, and the $\overline{Q}$ outputs are in the high state during power up. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, which prevents damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

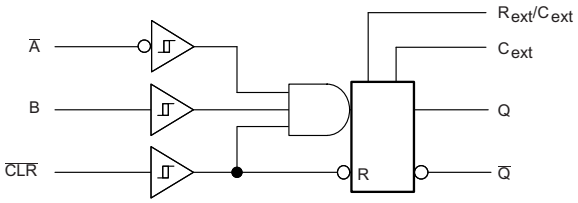


Figure 10. Logic Diagram, Each Multivibrator (Positive Logic)

8.3 Feature Description

The SN74LV123A operates over a wide supply range from 2 V to 5.5 V. The propagation delay has a maximum of 11 ns at 5-V supply. The typical output ground bounce is less than 0.8 V at 3.3-V supply and 25°C. The typical output V_{OH} undershoot is greater than 2.3 V at 3.3-V supply and 25°C.

These parts support mixed-mode voltage operation on all ports.

Schmitt-trigger circuitry on the $\overline{A}$, B, and $\overline{CLR}$ inputs allow for slow input transition rates and noisy input signals.

This device can be configured for rising or falling edge triggering.

This device supports partial-power-down mode operation.

This device is retriggerable for very long output pulses up to 100% duty cycle.

The clear signal overrides an output pulse and terminates it early.

Glitch-free power-up reset on outputs.

Feature Description (continued)

8.3.1 Power-Down Considerations

Large values of C_{ext} can cause problems when powering down the SN74LV123A-Q1 devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than t = V_{CC} × C_{ext} / 30 mA. For example, if V_{CC} = 5 V and Cext = 15 pF, the V_{CC} supply must turn off no faster than t = (5 V) × (15 pF) / 30 mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. The SN74LV123A-Q1 devices can sustain damage when a more rapid decrease of V_{CC} to zero occurs. Use external clamping diodes to avoid this possibility.

8.4 Device Functional Modes

Table 1 shows the functional modes for each monostable multivibrator in the SN74LV123A-Q1.

Table 1. Function Table (Each Multivibrator)

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L(1)	H(1)
X	X	L	L(1)	H(1)
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4LV123A device is a dual monostable multivibrator. It can be configured for many pulse width outputs and rising or falling-edge triggering. The application shown here could be used to signal separate interruptable inputs on a microcontroller when an input had a rising or falling edge.

9.2 Typical Application

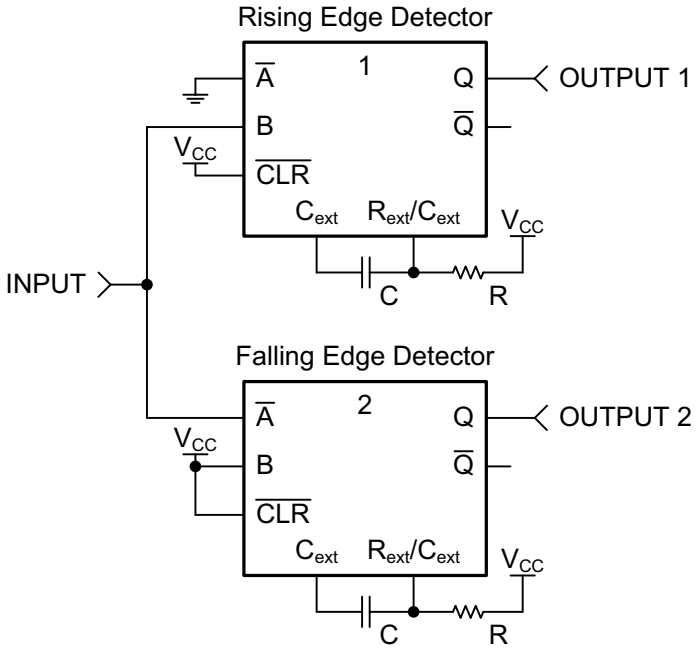


Figure 11. Simplified Application Schematic

9.2.1 Design Requirements

NOTE

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

9.2.1.1 Output Pulse Duration

The output pulse duration, t_w, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 12.

Typical Application (continued)

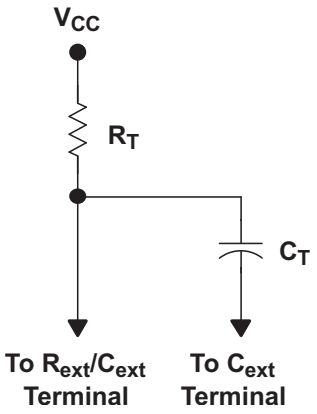


Figure 12. Timing-Component Connections

If C_T is ≥1000 pF and K = 1.0, the pulse duration is given by Equation 1:

$$t_w = K \times R_T \times C_T \quad (1)$$

where

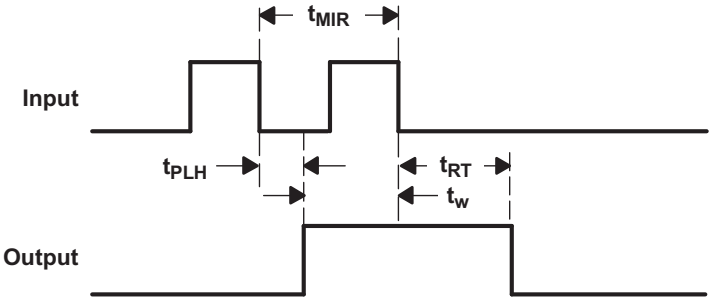
- t_w = pulse duration in ns
- R_T = external timing resistance in kΩ
- C_T = external capacitance in pF
- K = multiplier factor

if C_T is <1000 pF, K can be determined from Figure 5

Equation 1 and Figure 16 can be used to determine values for pulse duration, external resistance, and external capacitance.

9.2.1.2 Retriggering Data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR}, the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals must be t_{MIR} apart, where t_{MIR} = 0.30 × t_w. The retrigger pulse duration is calculated as shown in Figure 13.



$$t_{RT} = t_w + t_{PLH} = (K \times R_T \times C_T) + t_{PLH}$$

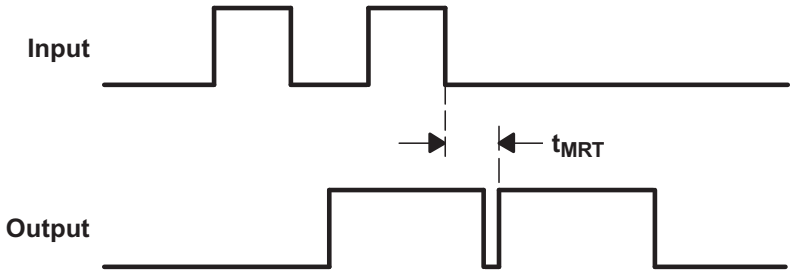
Where:

t_{MIR} = Minimum Input Retriggering Time
t_{PLH} = Propagation Delay
t_{RT} = Retrigger Time
t_w = Output Pulse Duration Before Retriggering

Figure 13. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output must be approximately 15 ns to ensure a retriggered output (see Figure 14).

Typical Application (continued)



t_{MRT} = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output
t_{MRT} = 15 ns

Figure 14. Input and Output Requirements

9.2.2 Detailed Design Procedure

- Timing requirements:
  - The pulse width must be long enough to be read by the desired output system, but short enough so that the output pulse completes prior to the next trigger event. It is recommended to make the output pulse just 10% longer than the minimum required for the output system.
- Recommended input conditions:
  - Slow or noisy inputs are allowed on $\overline{A}$, B, and $\overline{CLR}$ due to Schmitt-trigger input circuitry.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* .
- Recommended output conditions:
  - Load currents must not exceed the values listed in *Absolute Maximum Ratings*.

Typical Application (continued)

9.2.3 Application Curves

Operation of the devices at these or any other conditions beyond those indicated under (1) is not implied.

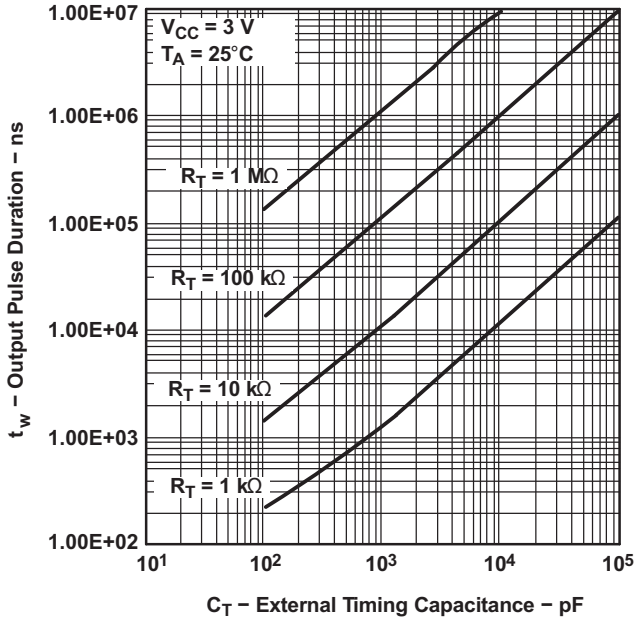


Figure 15. Output Pulse Duration vs. External Timing Capacitance

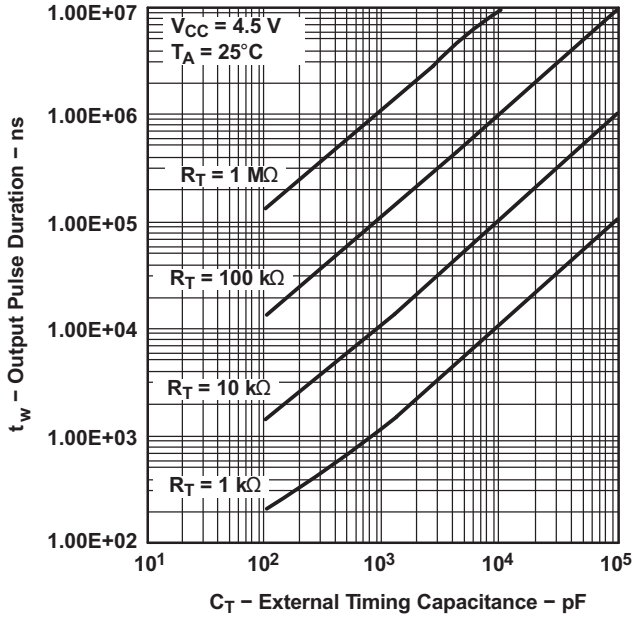


Figure 16. Output Pulse Duration vs. External Timing Capacitance

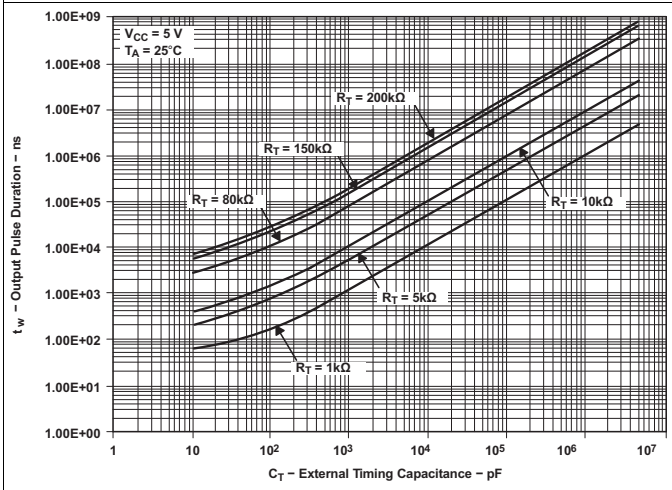


Figure 17. Output Pulse Duration vs External Timing Capacitance

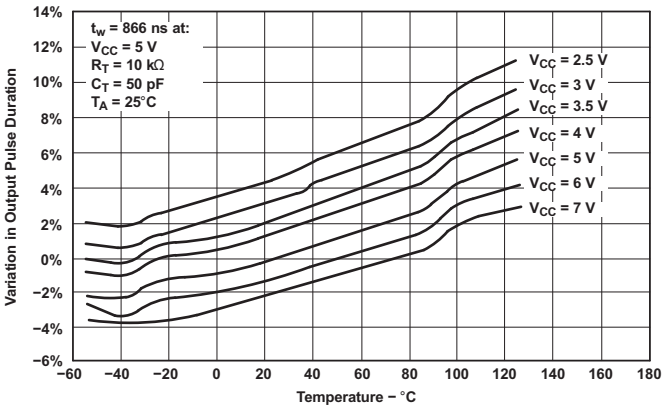


Figure 18. Variations in Output Pulse Duration vs Temperature

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* . Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends a 0.1-µF capacitor for devices with a single supply. If there are multiple VCC terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

Inputs must never float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

11.2 Layout Example

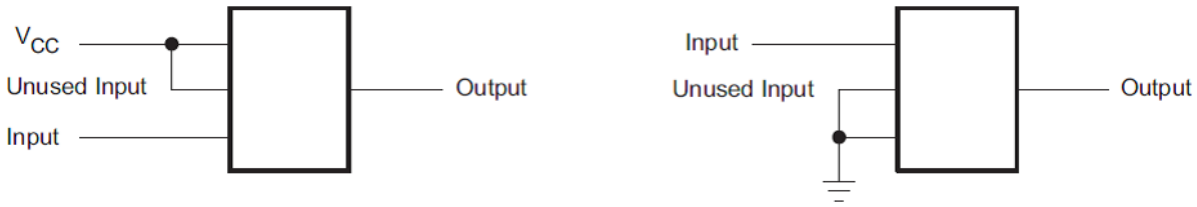


Figure 19. Layout Recommendation

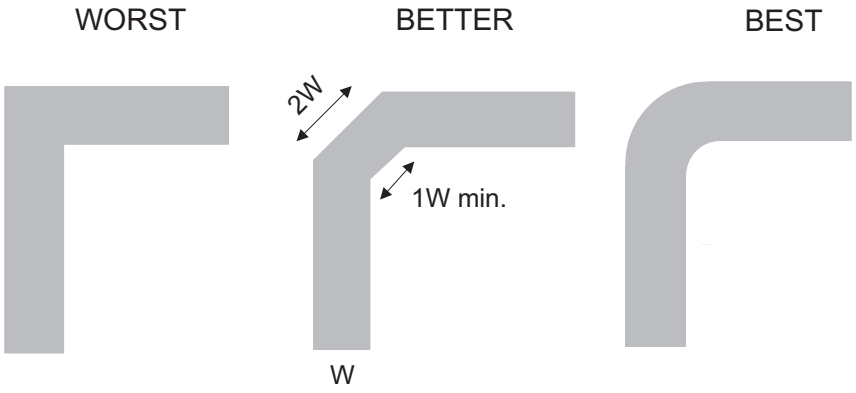


Figure 20. Trace Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV123ATPWRG4Q1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ
SN74LV123ATPWRG4Q1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ
SN74LV123ATPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ
SN74LV123ATPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ
SN74LV123ATPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV123A-Q1 :

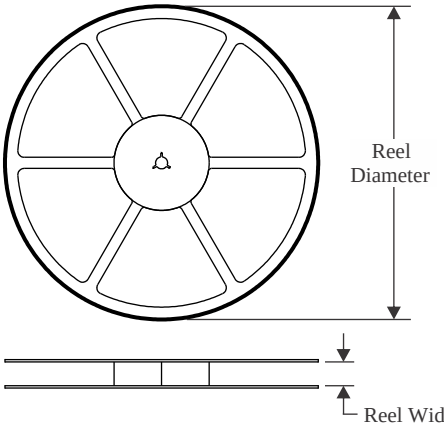
- Catalog : SN74LV123A
- Enhanced Product : SN74LV123A-EP

NOTE: Qualified Version Definitions:

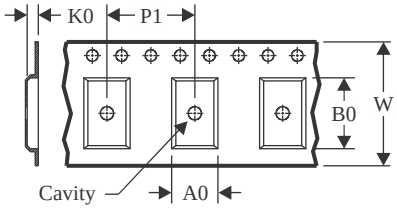
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

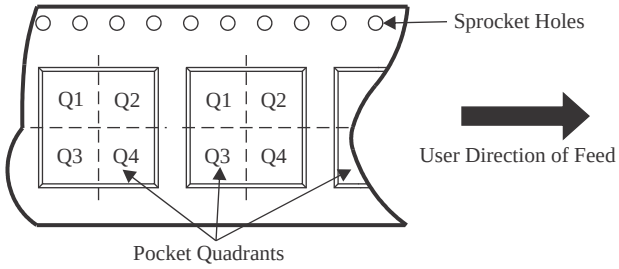


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

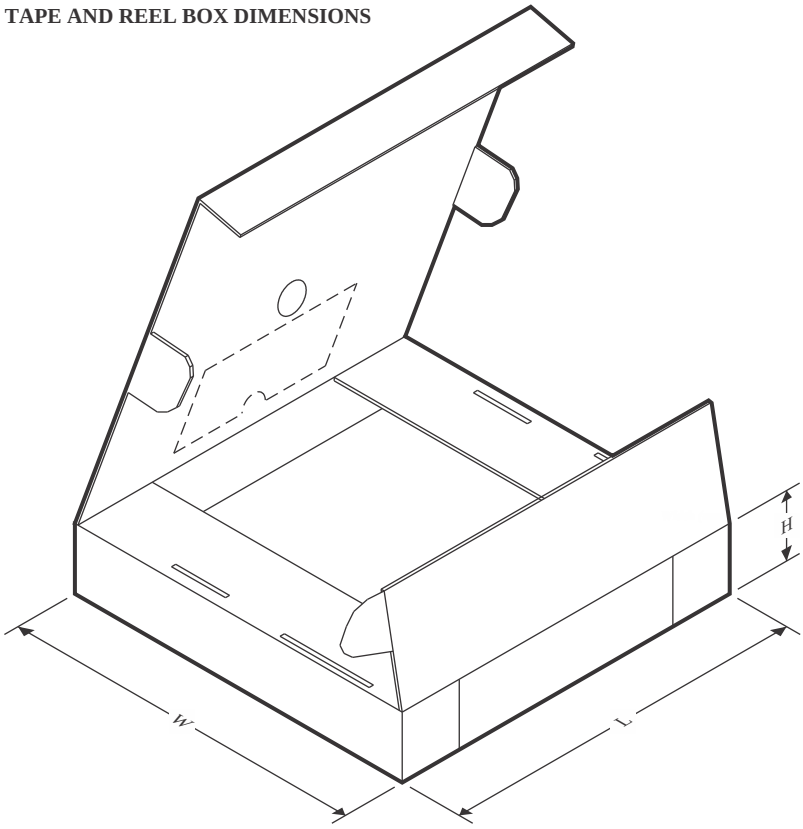
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV123ATPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

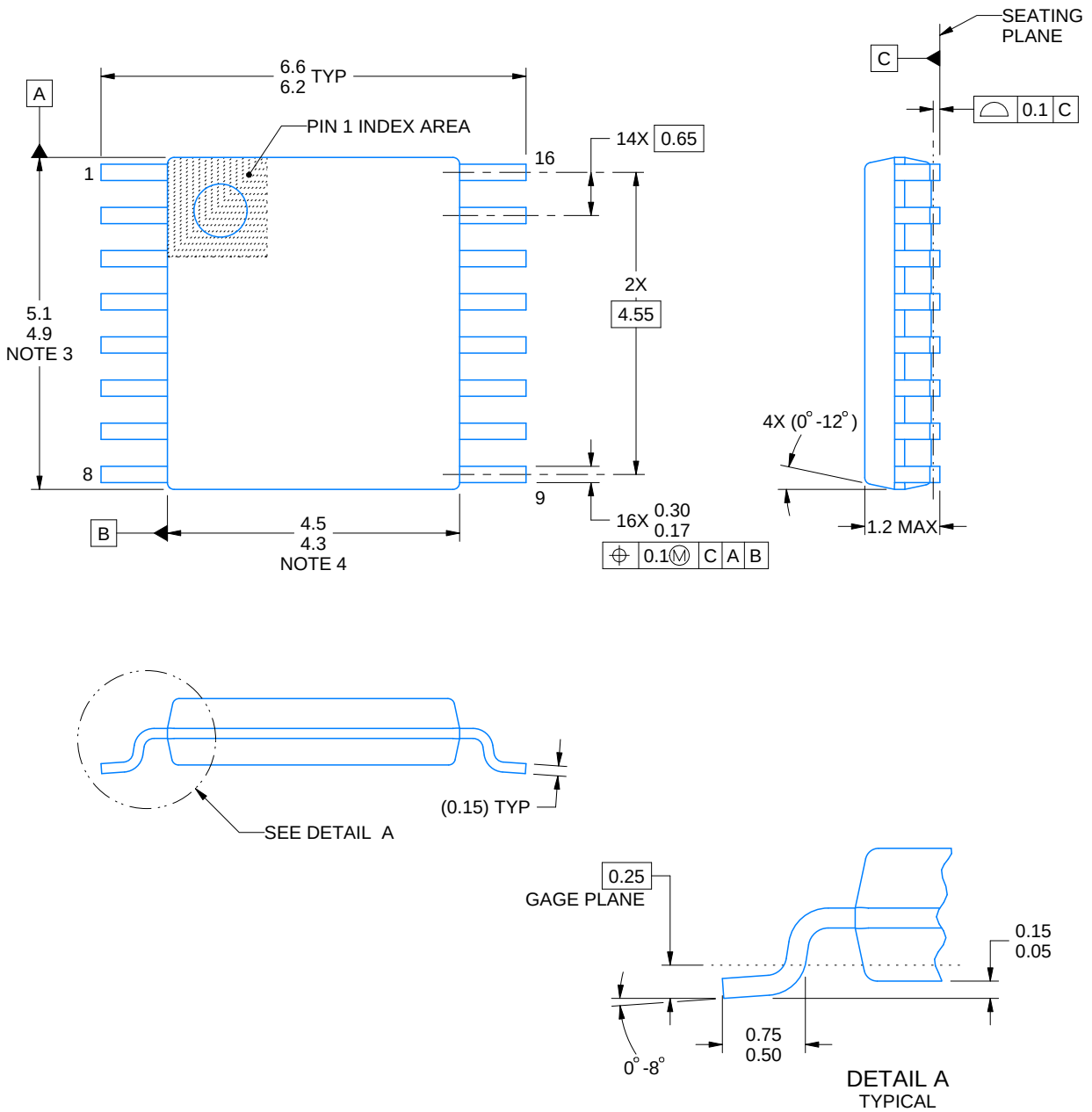
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV123ATPWRG4Q1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV123ATPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

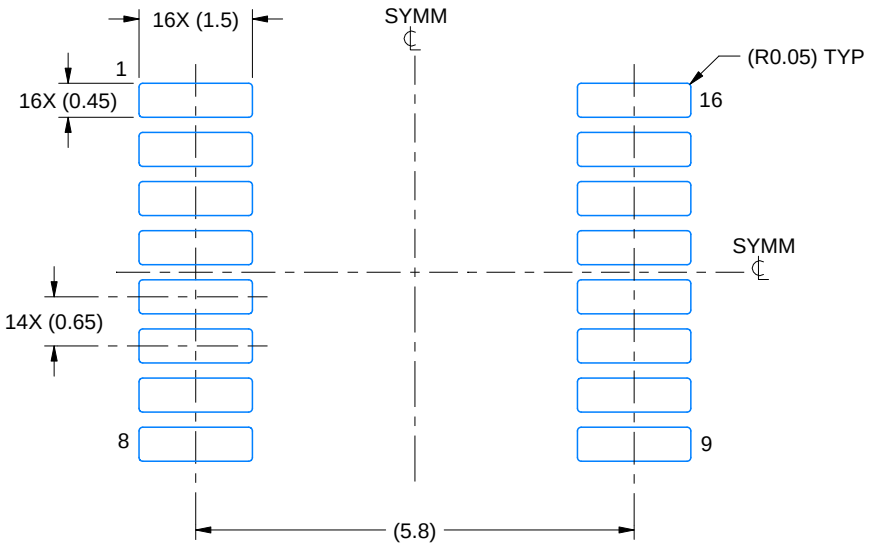
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



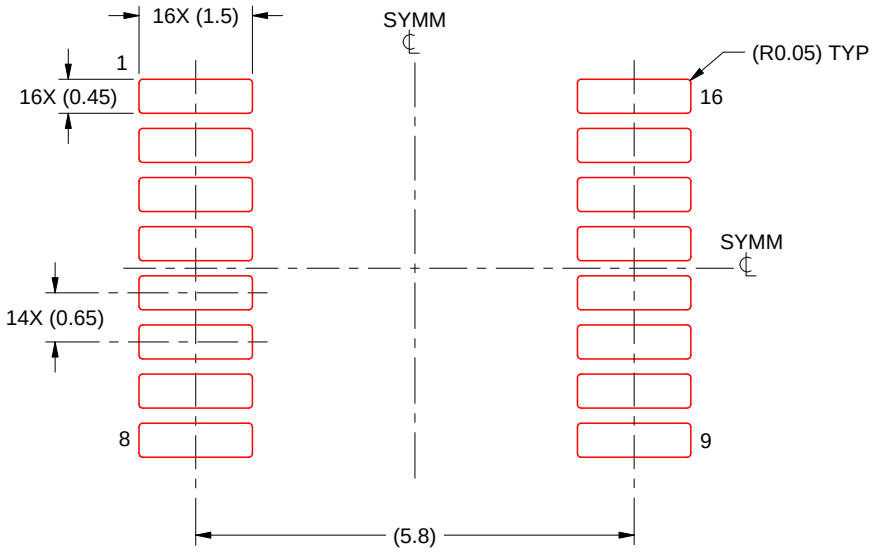
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265