- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  - N-Bit Encoding
  - Code Converters and Generators
- Typical Data Delay . . . 15 ns
- Typical Power Dissipation . . . 60 mW

description

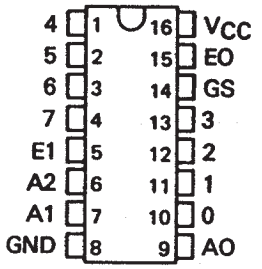
These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

FUNCTION TABLE

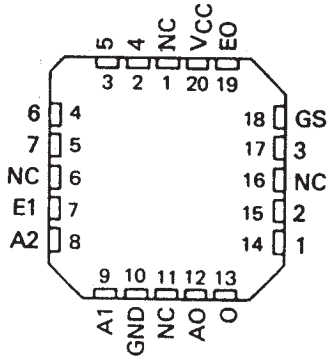
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance state

SN54LS348 . . . J OR W PACKAGE
SN74LS348 . . . D OR N PACKAGE
(TOP VIEW)

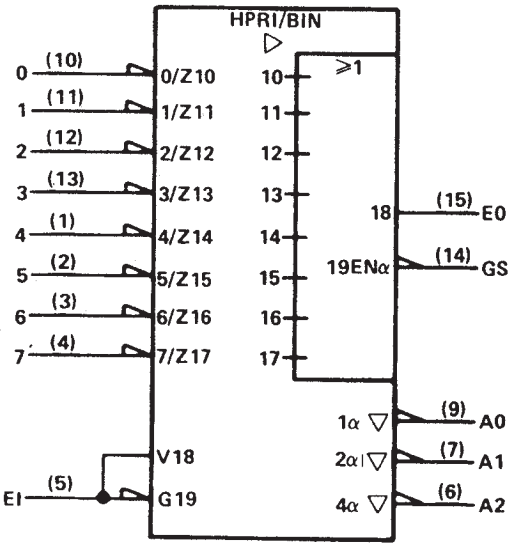


SN54LS348 . . . FK PACKAGE
(TOP VIEW)



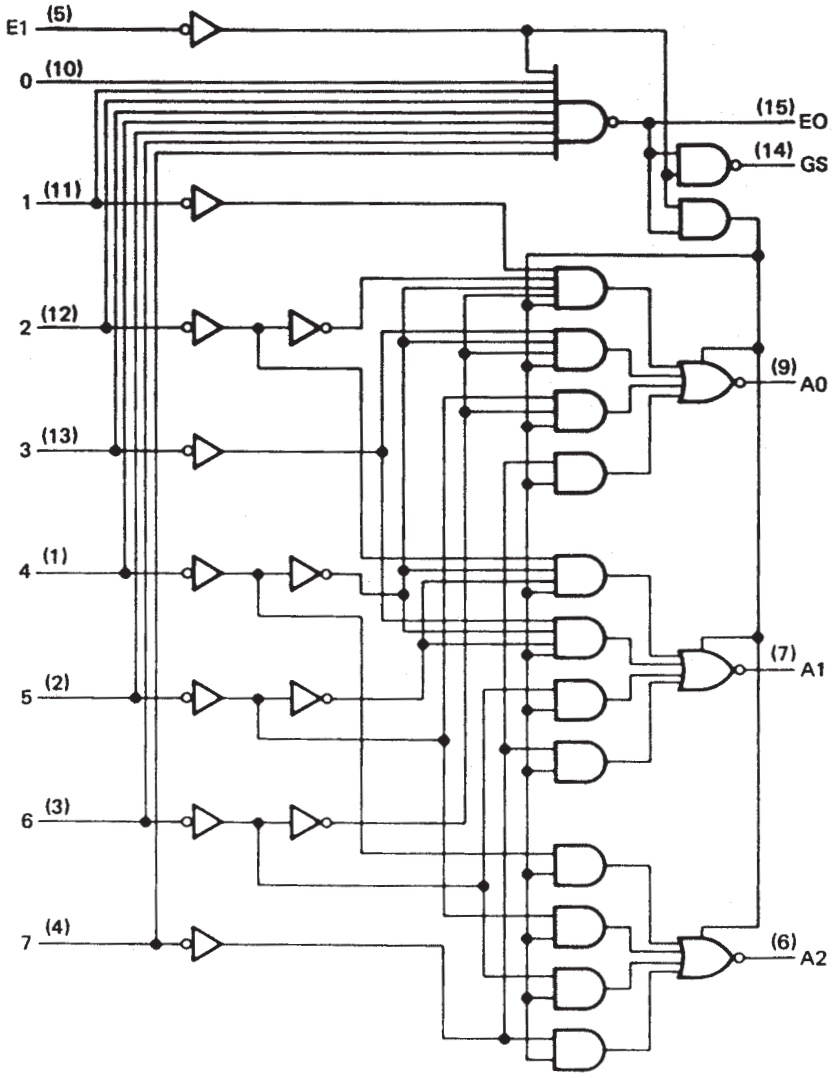
NC – No internal connection

logic symbol†



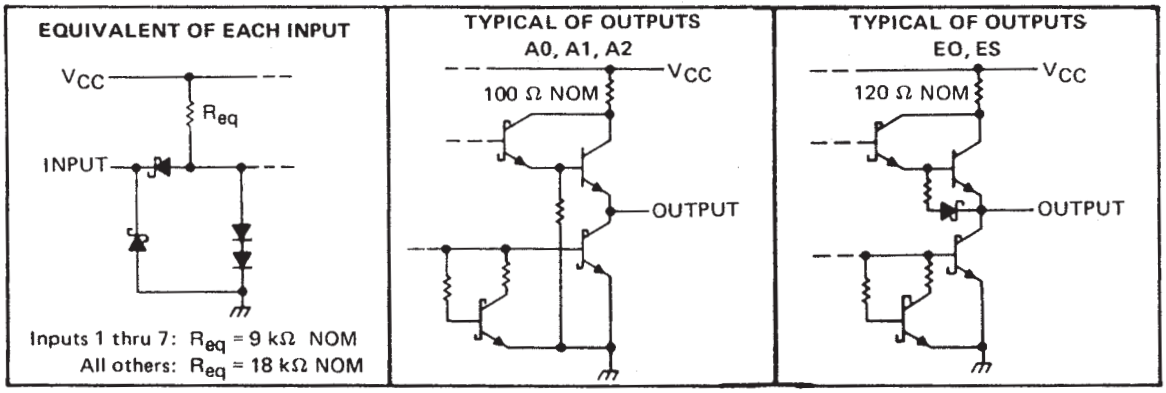
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS348 . . . . . −55°C to 125°C
SN74LS348 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS348			SN74LS348			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A0, A1, A2			−1			−2.6	mA
	EO, GS			−400			−400	μA
Low-level output current, I_{OL}	A0, A1, A2			12			24	mA
	EO, GS			4			8	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS348			SN74LS348			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.4	3.1					V
		EO, GS		I_{OH} = −2.6 mA				2.4	3.1		
				I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level Output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		EO, GS		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZ}	Off-State (high-impedance state) output current	A0, A1, A2	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
				V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		All other inputs					0.1			0.1	
I_{IH}	High-level input current	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		All other inputs					20			20	
I_{IL}	Low-level input current	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		All other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Outputs A0, A1, A2	V_{CC} = MAX		−30		−130	−30		−130	mA
		Outputs EO, GS			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition 1		13	25		13	25	mA
				Condition 2		12	23		12	23	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. I_{CC} (condition 2) is measured with all inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 45 pF, R_L = 667 Ω, See Note 3		11	17	ns
t_{PHL}						20	30	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			23	35	ns
t_{PHL}						23	35	
t_{PZH}	EI	A0, A1, or A2				25	39	ns
t_{PZL}						24	41	
t_{PLH}	0 thru 7	EO	Out-of-phase output	C_L = 15 pF R_L = 2 kΩ, See Note 3		11	18	ns
t_{PHL}						26	40	
t_{PLH}	0 thru 7	GS	In-phase output			38	55	ns
t_{PHL}						9	21	
t_{PLH}	EI	GS	In-phase output			11	17	ns
t_{PHL}						14	36	
t_{PLH}	EI	EO	In-phase output			17	26	ns
t_{PHL}						25	40	
t_{PHZ}	EI	A0, A1, or A2		C_L = 5 pF R_L = 667 Ω		18	27	ns
t_{PLZ}						23	35	

† t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

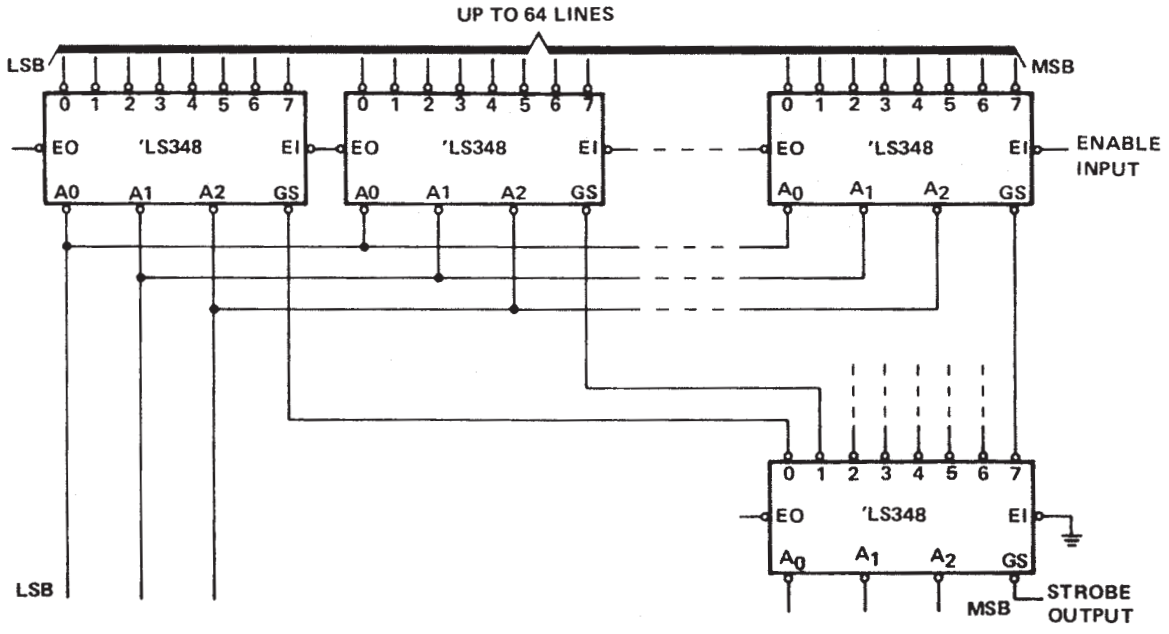


FIGURE 1–PRIORITY ENCODER WITH UP TO 64 INPUTS.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS348D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS348
SN74LS348D.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS348
SN74LS348N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS348N
SN74LS348N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS348N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

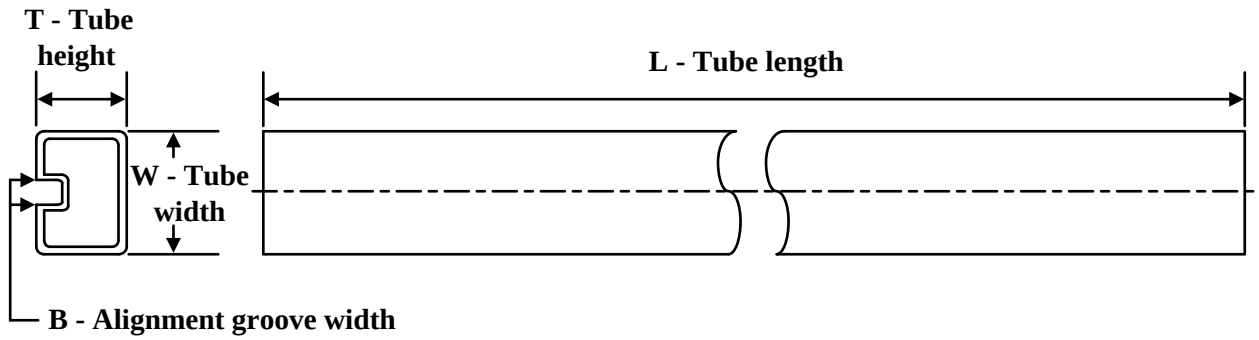
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

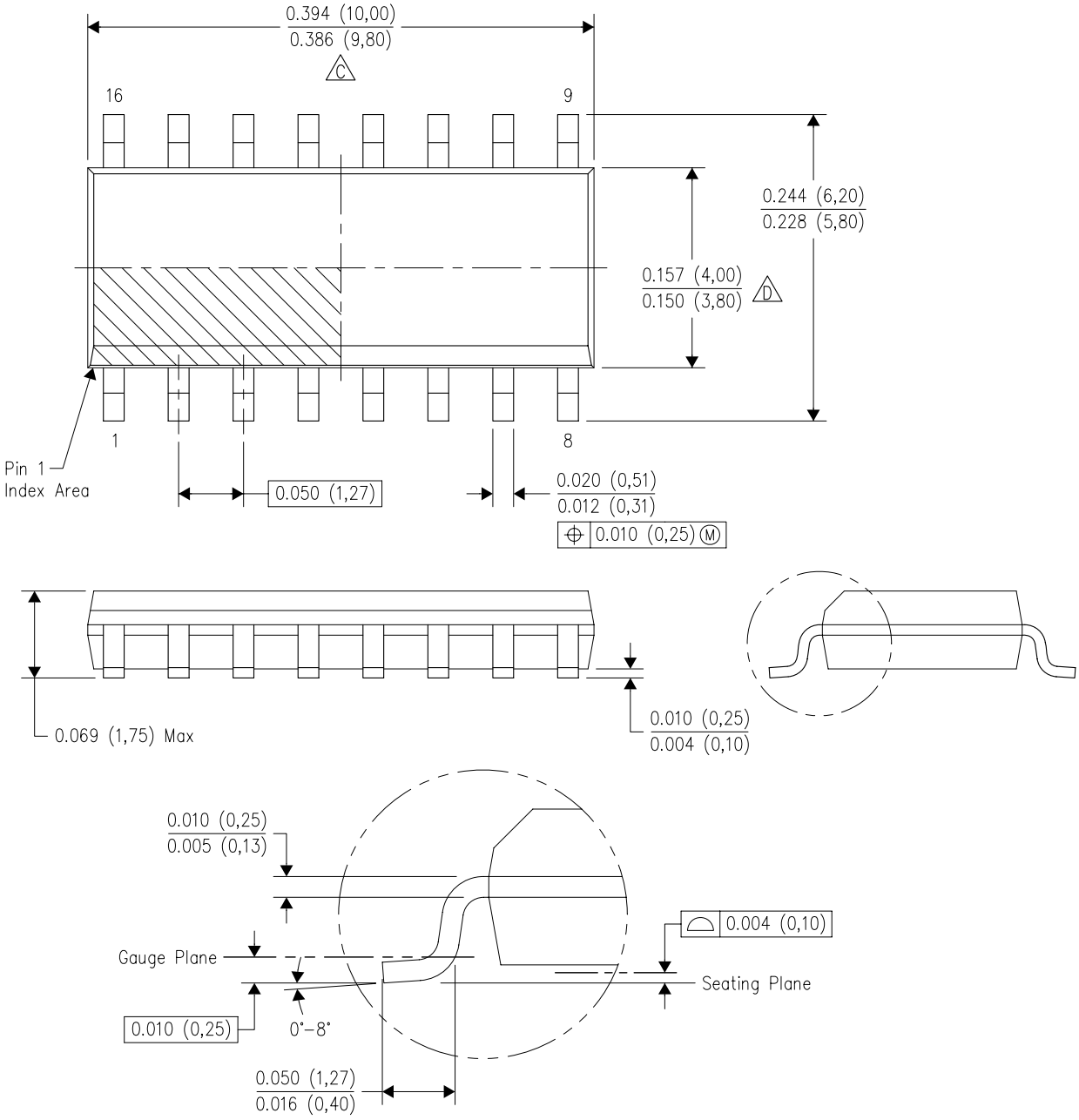
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS348D	D	SOIC	16	40	507	8	3940	4.32
SN74LS348D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS348N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS348N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS348N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS348N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

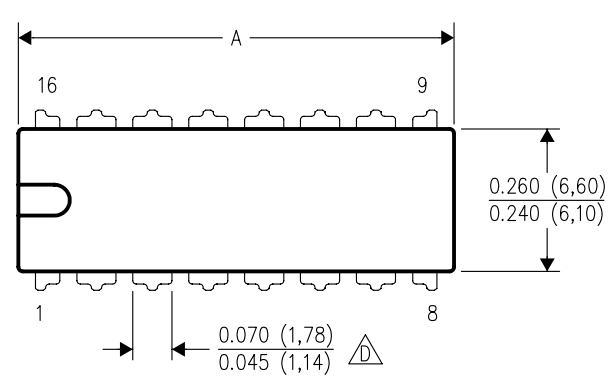


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

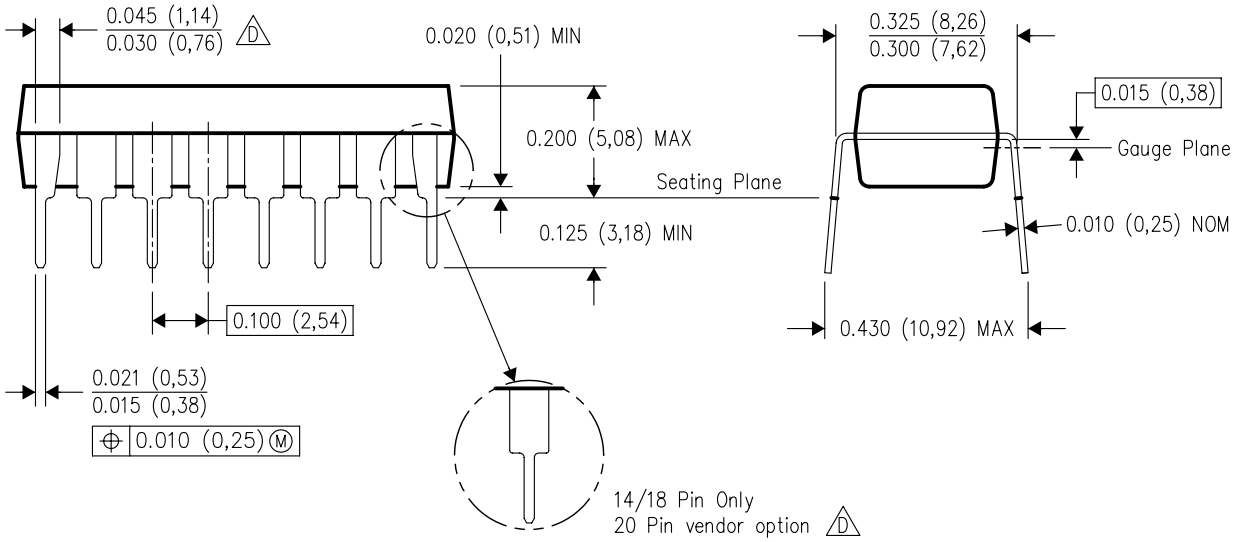
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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