具有三态输出寄存器的 SNx4HC595 8 位移位寄存器

1 特性

- 8 位串行输入/并行输出移位寄存器
- 2V 至 6V 的宽工作电压范围
- 高电流三态输出最多可驱动 15 个低功耗肖特基晶体管-晶体管逻辑器件 (LSTTL) 负载
- 低功耗：80 μA（最大值）I_{CC}
- t_{pd} = 13ns（典型值）
- 电压为 5V 时，输出驱动为 ±6mA
- 低输入电流：1 μA（最大值）
- 移位寄存器具有直接清零功能
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 网络交换机
- 电力基础设施
- LED 显示屏
- 服务器

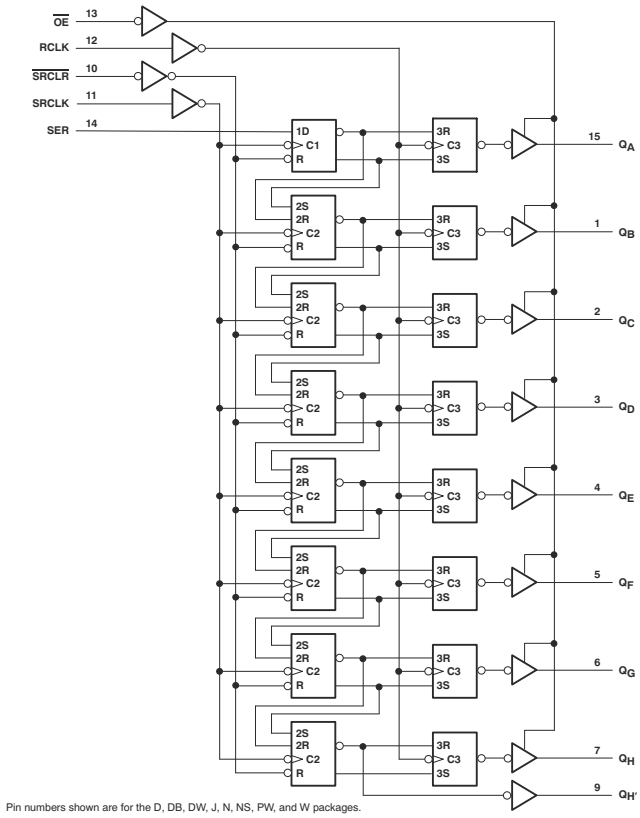
3 说明

SNx4HC595 器件包含对 8 位 D 类存储寄存器进行馈送的 8 位串行输入/并行输出移位寄存器。存储寄存器具有并行三态输出。移位寄存器和存储寄存器分别有单独的时钟。移位寄存器具有一个直接覆盖清零 ($\overline{SRCLR}$) 输入以及用于级联结构的串行 (SER) 输入和串行输出。当输出使能端 ($\overline{OE}$) 输入为高电平时，输出处于高阻抗状态。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
SN54HC595FK	LCCC (20)	8.89mm × 8.89mm
SN54HC595J	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm
SN74HC595N	PDIP (16)	19.31 mm × 6.35 mm
SN74HC595D	SOIC (16)	9.90mm × 3.90mm
SN74HC595DW	SOIC (16)	10.30mm x 7.50mm
SN74HC595DB	SSOP (16)	6.20mm x 5.30mm
SN74HC595PW	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

内容

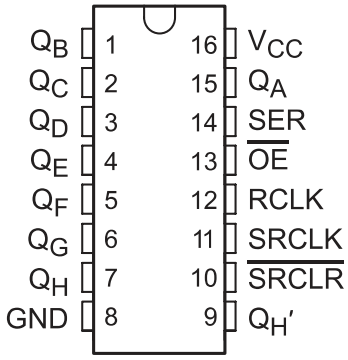
4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

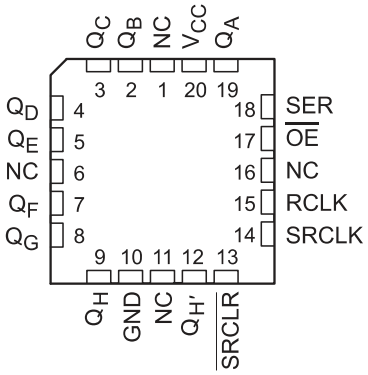
Changes from Revision H (November 2009) to Revision I (August 2015)	Page
• 添加了*应用* 部分、*器件信息* 表、*引脚配置和功能* 部分、*ESD 等级* 表、*热性能信息* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 删除了*订购信息* 表	1
• 向*特性* 列表中添加了“军用免责声明”。	1

Changes from Revision I (August 2015) to Revision J (October 2021)	Page
• 更新了器件信息表、ESD 等级表和器件功能模式表以符合现代数据表标准	1

5 引脚配置和功能



D、N、NS、J、DB 或 PW 封装
16 引脚 SOIC、PDIP、SO、CDIP、SSOP 或 TSSOP
顶视图



FK 封装
20 引脚 LCCC
顶视图

表 5-1. 引脚功能

引脚			I/O[1]	说明
名称	SOIC、PDIP、SO、CDIP、SSOP 或 TSSOP	LCCC		
GND	8	10	—	接地引脚
$\overline{OE}$	13	17	I	输出使能
Q_A	15	19	O	Q_A 输出
Q_B	1	2	O	Q_B 输出
Q_C	2	3	O	Q_C 输出
Q_D	3	4	O	Q_D 输出
Q_E	4	5	O	Q_E 输出
Q_F	5	7	O	Q_F 输出
Q_G	6	8	O	Q_G 输出
Q_H	7	9	O	Q_H 输出
$Q_{H'}$	9	12	O	$Q_{H'}$ 输出
RCLK	12	14	I	RCLK 输入
SER	14	18	I	SER 输入
SRCLK	11	14	I	SRCLK 输入
$\overline{SRCLR}$	10	13	I	$\overline{SRCLR}$ 输入
NC	—	1	—	无连接
		16		
		11		
		16		
V_{CC}	—	20	—	电源引脚

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出。

6 规格

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		–0.5	7	V
I_{IK}	输入钳位电流(2)	$V_I < 0$ 或 $V_I > V_{CC}$		±20	mA
I_{OK}	输出钳位电流 (2)	$V_O < 0$ 或 $V_O > V_{CC}$		±20	mA
I_O	持续输出电流	$V_O = 0$ 至 V_{CC}		±35	mA
	通过 V_{CC} 或 GND 的持续电流			±70	mA
T_J	结温			150	°C
T_{stg}	存储温度		–65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

6.2 ESD 等级

		值	单位
$V_{(ESD)}$ 静电放电	人体放电模型（HBM），符合 ANSI/ESDA/JEDEC JS-001(1)	2000	V
	充电器件模型 (CDM)，符合 ANSI/ESDA/JEDEC JS-002 标准(2)	1000	

(1) JEDEC 文件 JEP155 指出：500V HBM 可实现在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议的操作条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54HC595			SN74HC595			单位
			最小值	标称值	最大值	最小值	标称值	最大值	
V_{CC}	电源电压		2	5	6	2	5	6	V
V_{IH}	高电平输入电压	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	低电平输入电压	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	输入电压		0		V_{CC}	0		V_{CC}	V
V_O	输出电压		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	输入转换上升/下降时间(2)	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5V			500			500	
		V_{CC} = 6 V			400			400	
T_A	自然通风条件下的工作温度范围		-55		125	–40		85	°C

(1) 器件所有的未使用输入必须被保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告*慢速或浮点 CMOS 输入的影响*，SCBA004。
(2) 如果此器件用于阈值区域（从 V_{IL}max = 0.5V 至 V_{IH} min = 1.5V），感应接地有可能进入错误状态，导致双时钟。在 t_t = 1000ns 且 V_{CC} = 2V 的输入范围内工作不会损坏器件；但在功能上，在移位、计数或切换操作模式下不能确保 CLK 输入。

6.4 热性能信息

热指标(1)	SN74HC595						单位
	D (SOIC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	
$R_{\theta JA}$ 结至环境热阻	73	82	57	67	64	108	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

6.5 电气特性

在推荐的自然通风条件下的工作温度范围（除非另外注明）

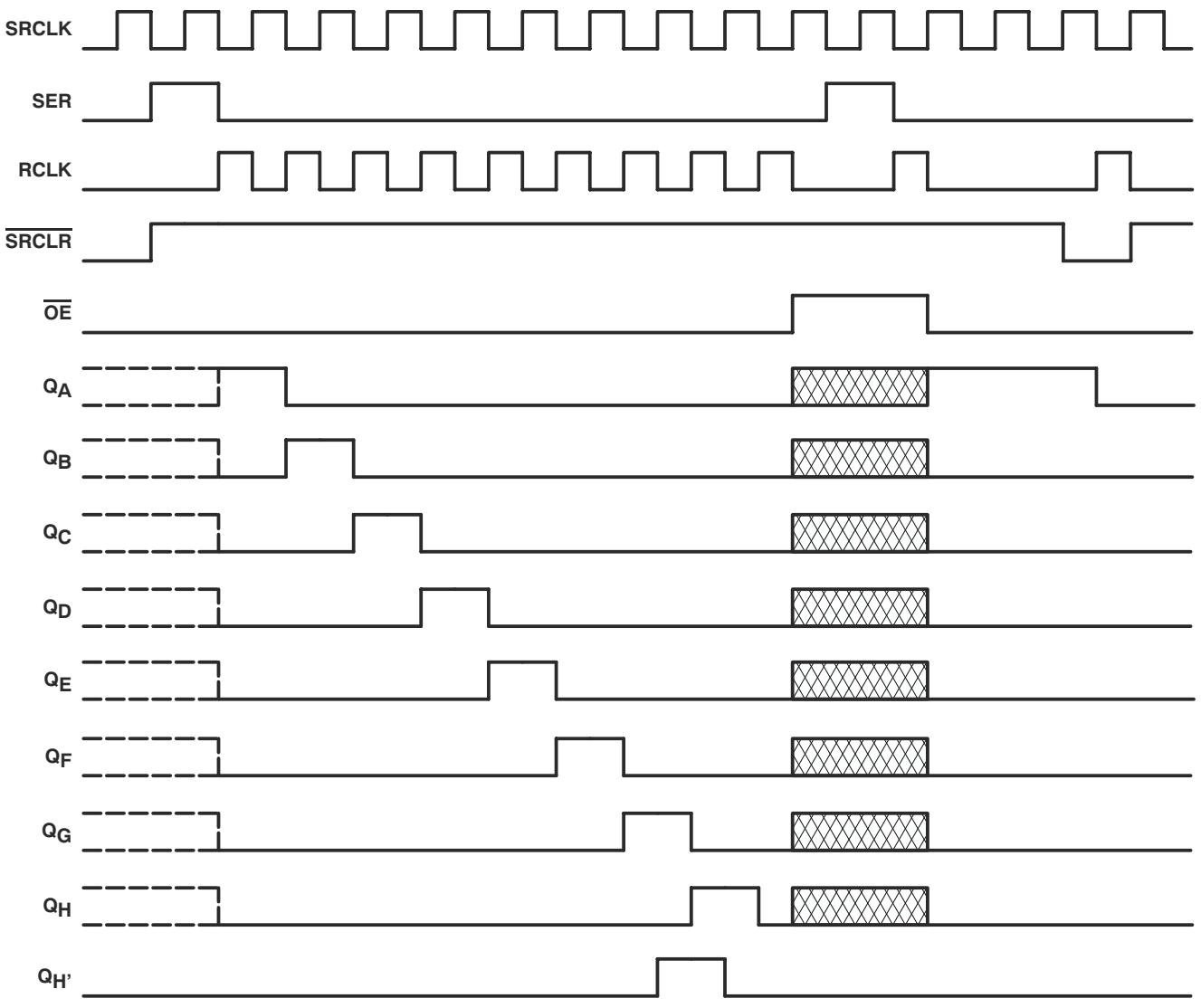
参数	测试条件		V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	V_I = V_{IH} 或 V_{IL}	I_{OH}=-20 μA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		$Q_{H'}$，I_{OH} = –4mA	4.5V	3.98	4.3		3.7		3.84		
		Q_A – Q_H，I_{OH} = –6mA		3.98	4.3		3.7		3.84		
		$Q_{H'}$，I_{OH} = −5.2mA	6V	5.48	5.8		5.2		5.34		
		Q_A – Q_H，I_{OH} = –7.8mA		5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} 或 V_{IL}	I_{OL} = 20 μA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6V		0.001	0.1		0.1		0.1	
		$Q_{H'}$，I_{OL} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		Q_A – Q_H，I_{OL} = 6mA			0.17	0.26		0.4		0.33	
		$Q_{H'}$，I_{OL} = 5.2mA	6V		0.15	0.26		0.4		0.33	
		Q_A – Q_H，I_{OL} = 7.8mA			0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} 或 0		6V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} 或 0，Q_A – Q_H		6V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} 或 0，I_O = 0		6V			8		160		80	μA
C_i			2V 至 6V		3	10		10		10	pF

6.6 时序要求

在自然通风条件下的工作温度范围内测得（除非另有说明）

			V_{CC}	T_A = 25°C		SN54HC595		SN74HC595		单位
				最小值	最大值	最小值	最大值	最小值	最大值	
f_{clock}	时钟频率		2V		6		4.2		5	MHz
			4.5V		31		21		25	
			6V		36		25		29	
t_w	脉冲持续时间	SRCLK 或 RCLK 为高电平或低电平	2V	80		120		100		ns
			4.5V	16		24		20		
			6V	14		20		17		
		$\overline{SRCLR}$ 为低电平	2V	80		120		100		
			4.5V	16		24		20		
			6V	14		20		17		
t_{su}	建立时间	SRCLK ↑ 之前的 SER	2V	100		150		125		ns
			4.5V	20		30		25		
			6V	17		25		21		
		SRCLK ↑ 在 RCLK ↑ 之前(1)	2V	75		113		94		
			4.5V	15		23		19		
			6V	13		19		16		
		$\overline{SRCLR}$ 在 RCLK ↑ 之前为低电平	2V	50		75		65		
			4.5V	10		15		13		
			6V	9		13		11		
		$\overline{SRCLR}$ 在 SRCLK ↑ 之前为高电平（无效）	2V	50		75		60		
			4.5V	10		15		12		
			6V	9		13		11		
t_h	保持时间，SER 在 SRCLK ↑ 之后		2V	0		0		0		ns
			4.5V	0		0		0		
			6V	0		0		0		

(1) 该建立时间允许存储寄存器从移位寄存器接收稳定的数据。时钟可以捆绑在一起，在这种情况下，移位寄存器比存储寄存器提前一个时钟脉冲。



NOTE: ▨ implies that the output is in 3-State mode.

图 6-1. 时序图

6.7 开关特性

在建议的自然通风条件下的工作温度范围内。

参数	从（输入）	至（输出）	负载电容	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		单位
					最小值	典型值	最大值	最小值	最大值	最小值	最大值	
f_{max}			50pF	2V	6	26		4.2		5		MHz
				4.5V	31	38		21		25		
				6V	36	42		25		29		
t_{pd}	SRCLK	$Q_{H'}$	50pF	2V		50	160		240		200	ns
				4.5V		17	32		48		40	
				6V		14	27		41		34	
	RCLK	Q_A – Q_H	50pF	2V		50	150		225		187	
				4.5V		17	30		45		37	
				6V		14	26		38		32	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	50pF	2V		51	175		261		219	ns
				4.5V		18	35		52		44	
				6V		15	30		44		37	
t_{en}	$\overline{OE}$	Q_A – Q_H	50pF	2V		40	150		255		187	ns
				4.5V		15	30		45		37	
				6V		13	26		38		32	
t_{dis}	$\overline{OE}$	Q_A – Q_H	50pF	2V		42	200		300		250	ns
				4.5V		23	40		60		50	
				6V		20	34		51		43	
t_t		Q_A – Q_H	50pF	2V		28	60		90		75	ns
				4.5V		8	12		18		15	
				6V		6	10		15		13	
		$Q_{H'}$	50pF	2V		28	75		110		95	
				4.5V		8	15		22		19	
				6V		6	13		19		16	
t_{pd}	RCLK	Q_A – Q_H	150pf	2V		60	200		300		250	ns
				4.5V		22	40		60		50	
				6V		19	34		51		43	
t_{en}	$\overline{OE}$	Q_A – Q_H	150pF	2V		70	200		298		250	ns
				4.5V		23	40		60		50	
				6V		19	34		51		43	
t_t		Q_A – Q_H	150pF	2V		45	210		315		265	ns
				4.5V		17	42		63		53	
				6V		13	36		53		45	

6.8 工作特性

T_A = 25°C

参数		测试条件	典型值	单位
C_{pd}	功率耗散电容	无负载	400	pF

6.9 典型特性

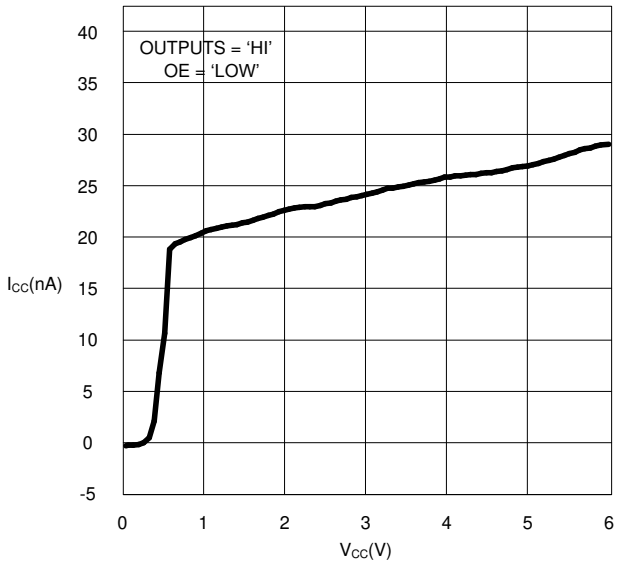
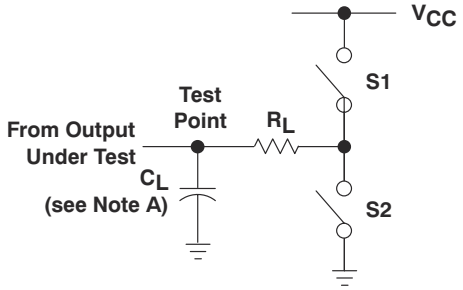


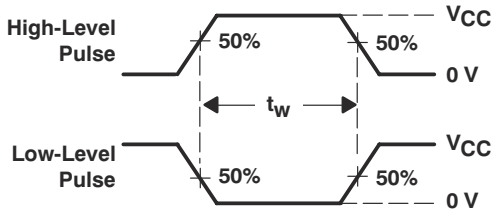
图 6-2. SN74HC595 I_{CC} 与 V_{CC} 间的关系

7 参数测量信息

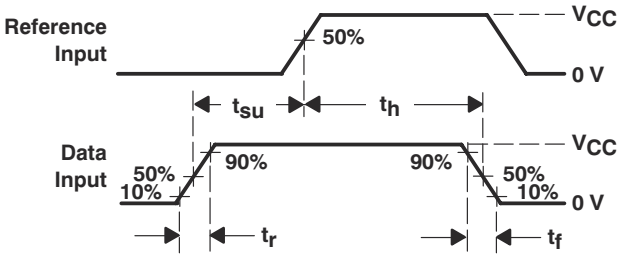


LOAD CIRCUIT

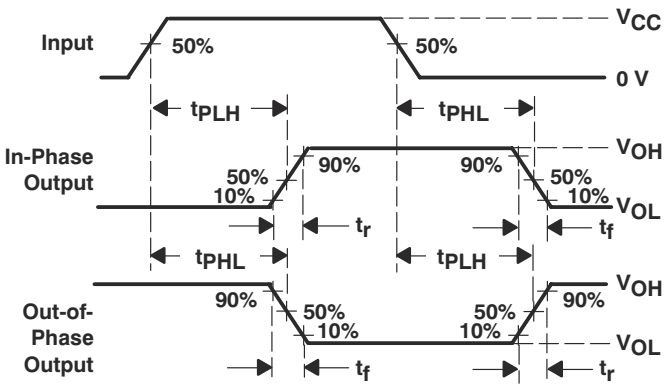
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t			50 pF or 150 pF	Open	Open



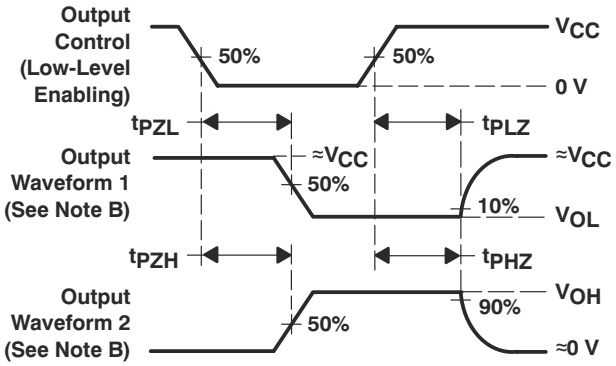
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 7-1. 负载电路和电压波形

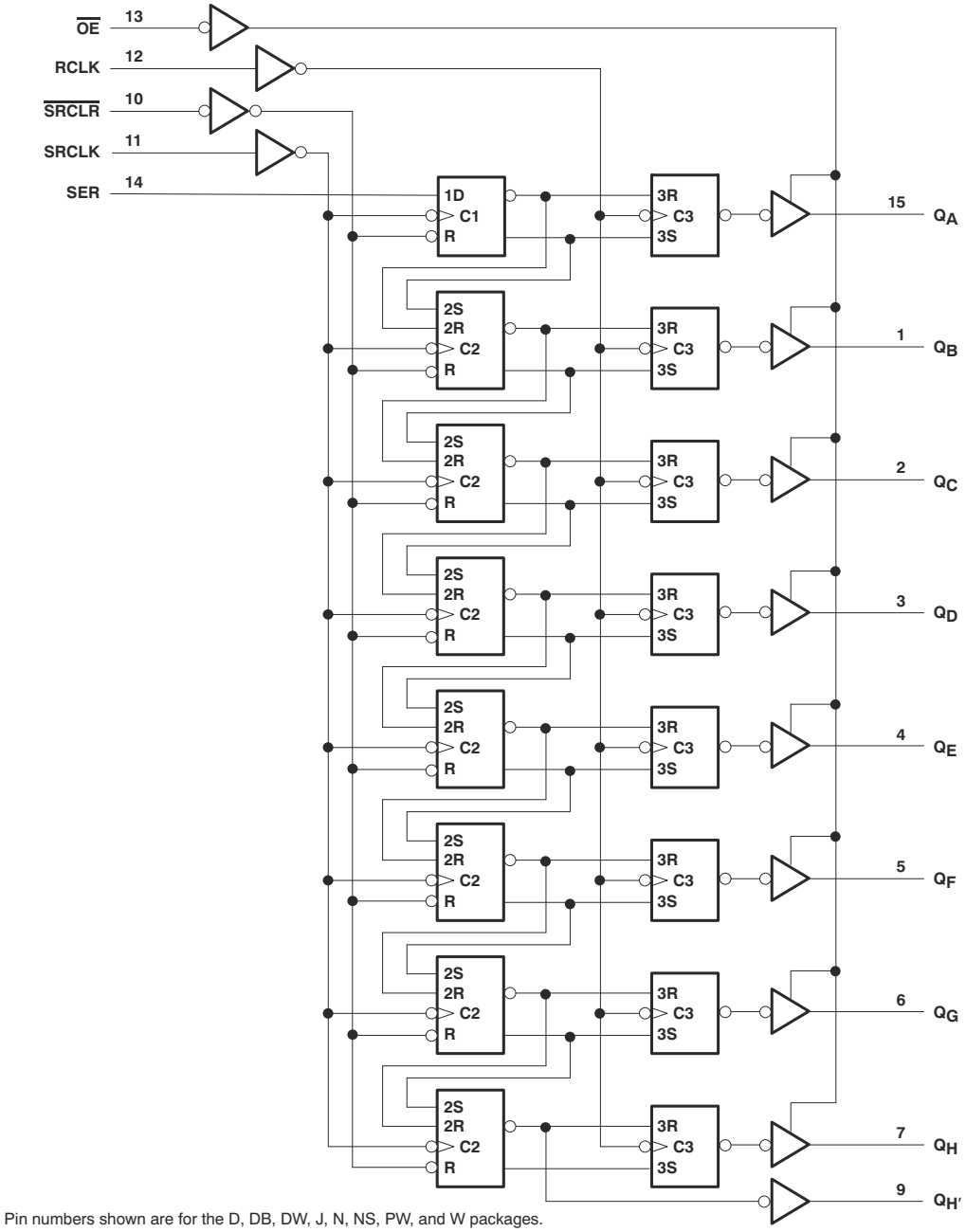
8 详细说明

8.1 概述

SNx4HC595 是用于 CMOS 应用的 HC 系列逻辑器件中的一部分。SNx4HC595 器件包含对 8 位 D 类存储寄存器进行馈送的 8 位串行输入/并行输出移位寄存器。

移位寄存器时钟 (SRCLK) 和存储寄存器时钟 (RCLK) 均为正边沿触发。如果将两个时钟连接在一起，则移位寄存器始终比存储寄存器早一个时钟脉冲。

8.2 功能方框图



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

8.3 特性说明

SNx4HC595 器件是 8 位串行输入、并行输出移位寄存器。它们具有 2V 至 6V 的宽工作电流，大电流三态输出可驱动多达 15 个 LSTTL 负载。这些器件具有 80 μA（最大值）I_{CC} 的低功耗。此外，这些器件具有 1 μA（最大值）的低输入电流和 5V 时的 ±6mA 输出驱动。

8.4 器件功能模式

表 8-1 列出了 SNx4HC595 器件的功能模式。

表 8-1. 功能表

输入					功能
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	H	输出 Q_A - Q_H 被禁用。
X	X	X	X	L	输出 Q_A - Q_H 被启用。
X	X	L	X	X	移位寄存器清零。
L	↑	H	X	X	移位寄存器的第一级变低。 其他阶段分别存储前一阶段的数据。
H	↑	H	X	X	移位寄存器的第一级变高。 其他阶段分别存储前一阶段的数据。
X	X	X	↑	X	移位寄存器数据存储在存储寄存器中。

9 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 应用信息

SNx4HC595 是一款低驱动 CMOS 器件，可用于需要考虑输出振铃的多种总线接口类型应用。低驱动和慢速边沿速率将更大限度地减少输出上的过冲和下冲。

9.2 典型应用

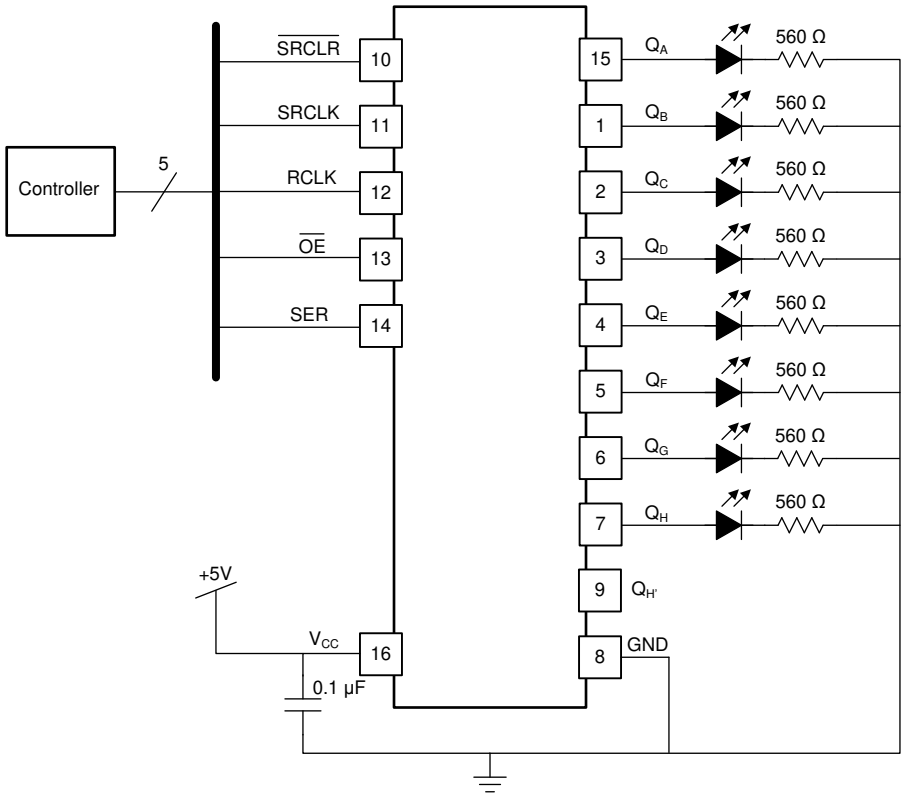


图 9-1. 典型应用原理图

9.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

9.2.2 详细设计过程

- 建议的输入条件
  - 指定了高电平和低电平。请参阅 *节 6.3* 表中的（V_{IH} 和 V_{IL}）。
  - 指定了高电平和低电平。请参阅 *节 6.3* 表中的（V_{IH} 和 V_{IL}）。
  - 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 5.5V
- 建议的输出条件
  - 每个输出的负载电流不应超过 35mA，该器件的总电流不应超过 70mA
  - 输出不应被拉至高于 V_{CC}

9.2.3 应用曲线

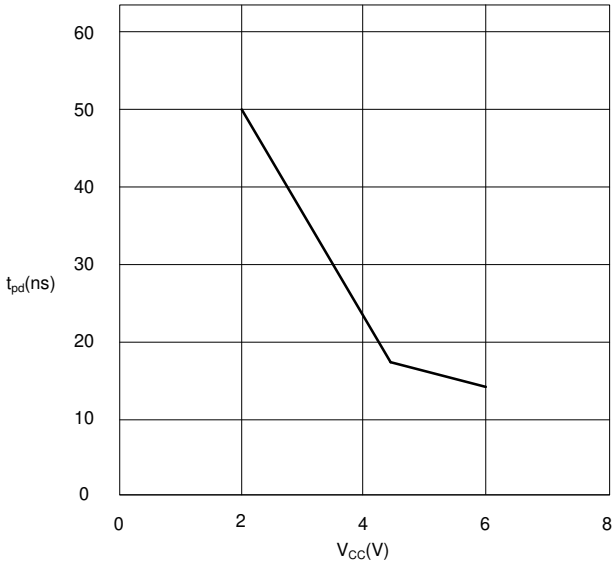


图 9-2. SN75HC595 t_{pd} 与 V_{CC}

10 电源相关建议

电源可以是 *节 6.3* 表中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 μf；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01 μf 或 0.022 μf。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 μf 和 1 μf 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

11 布局

11.1 布局指南

当使用多位逻辑器件时，输入不应悬空。

在许多情况下，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时，未使用数字逻辑器件的功能或部分功能。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。图 11-1 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须被连接至一个高或低偏置以防止它们悬空。应应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们将连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。浮动输出通常是可以接受的，除非该器件是收发器。如果收发器有一个输出使能引脚，它会在置位时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此它们在禁用后不能浮动。

11.2 布局示例

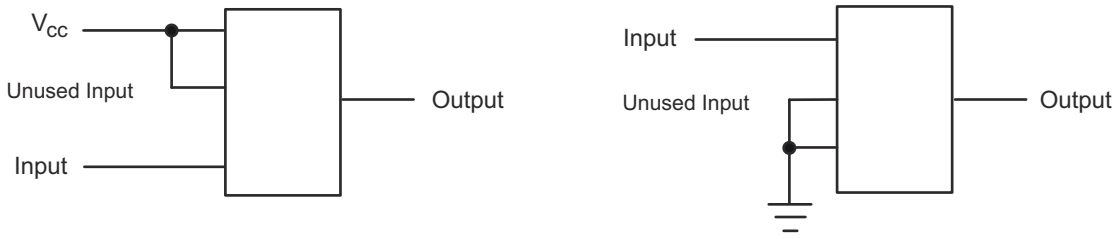


图 11-1. 布局图

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*慢速或浮点 CMOS 输入的影响* 应用简介

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-86816012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86816012A SNJ54HC595FK
5962-8681601EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601EA SNJ54HC595J
5962-8681601VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601VEA SNV54HC595J
5962-8681601VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601VEA SNV54HC595J
5962-8681601VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601VFA SNV54HC595W
5962-8681601VFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601VFA SNV54HC595W
SN54HC595J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC595J
SN54HC595J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC595J
SN74HC595DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DBRE4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DBRG4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DRE4	Active	Production	null (null) |	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN74HC595DRG3	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DRG3.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	HC595

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC595DW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	HC595
SN74HC595DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC595N
SN74HC595N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC595N
SN74HC595NE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC595N
SN74HC595NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	HC595
SN74HC595PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SN74HC595PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595
SNJ54HC595FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86816012A SNJ54HC595FK
SNJ54HC595FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86816012A SNJ54HC595FK
SNJ54HC595J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601EA SNJ54HC595J
SNJ54HC595J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681601EA SNJ54HC595J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54HC595, SN54HC595-SP, SN74HC595 :

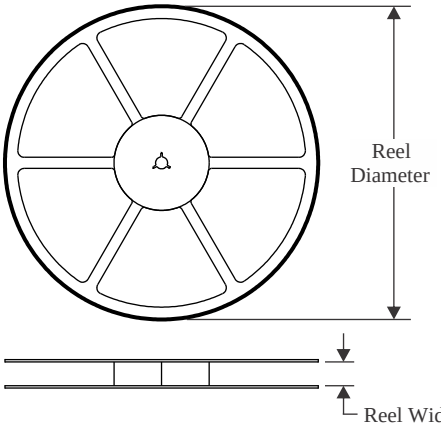
- Catalog : SN74HC595, SN54HC595
- Enhanced Product : SN74HC595-EP, SN74HC595-EP
- Military : SN54HC595
- Space : SN54HC595-SP

NOTE: Qualified Version Definitions:

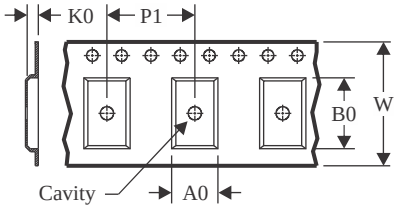
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

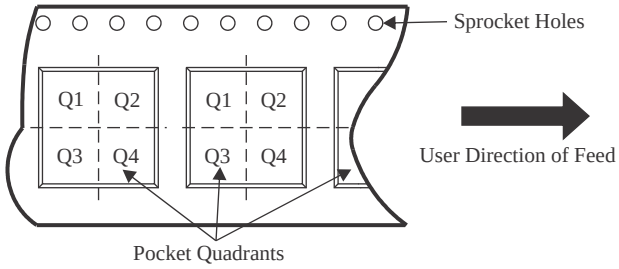


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

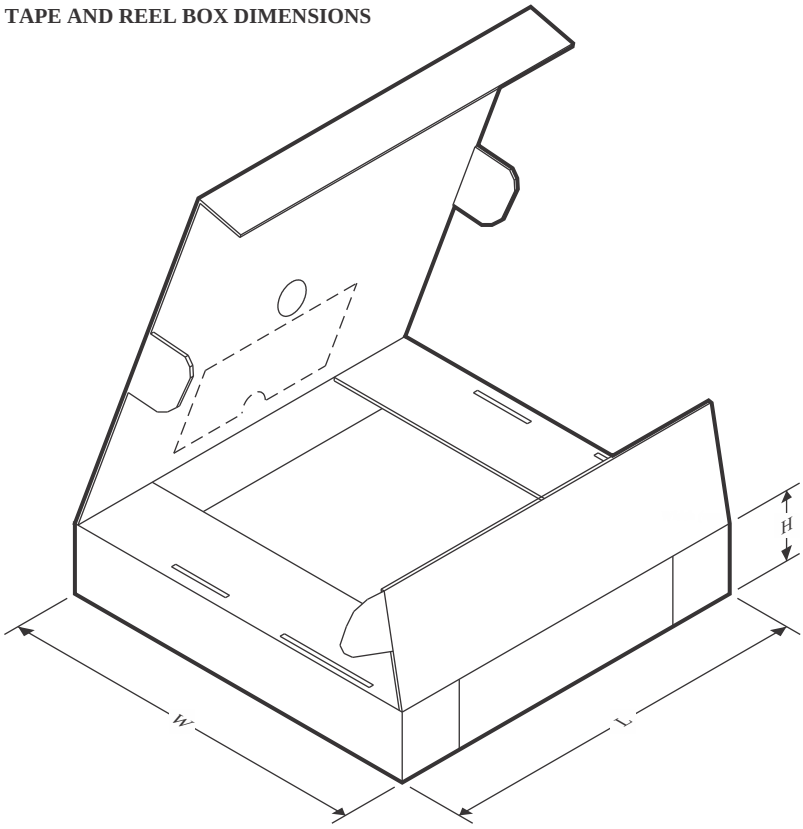
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DRG3	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HC595DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74HC595NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC595NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC595PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

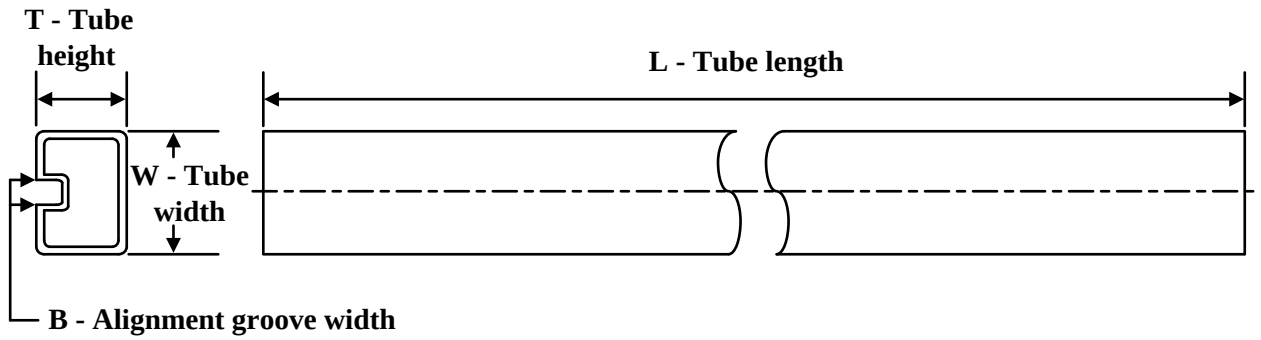
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

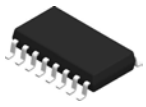
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC595DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC595DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC595DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC595DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC595DRG3	SOIC	D	16	2500	366.0	364.0	50.0
SN74HC595DRG4	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC595DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN74HC595NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74HC595NSR	SOP	NS	16	2000	367.0	367.0	38.0
SN74HC595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC595PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-86816012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8681601EA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8681601VEA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8681601VEA.A	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8681601VFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-8681601VFA.A	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC595FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC595FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC595J	J	CDIP	16	25	506.98	15.24	13440	NA
SNJ54HC595J.A	J	CDIP	16	25	506.98	15.24	13440	NA

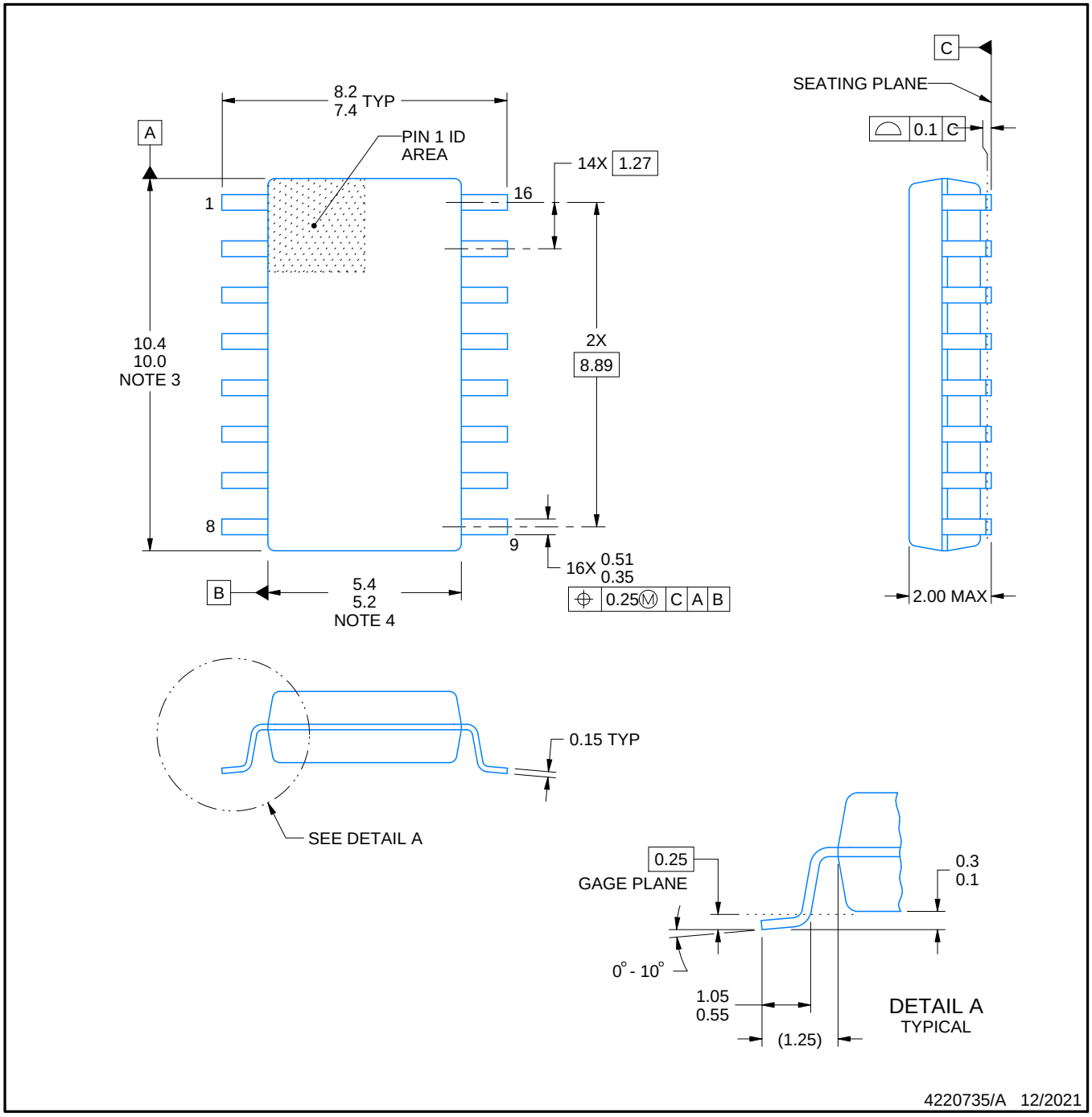


PACKAGE OUTLINE

NS0016A

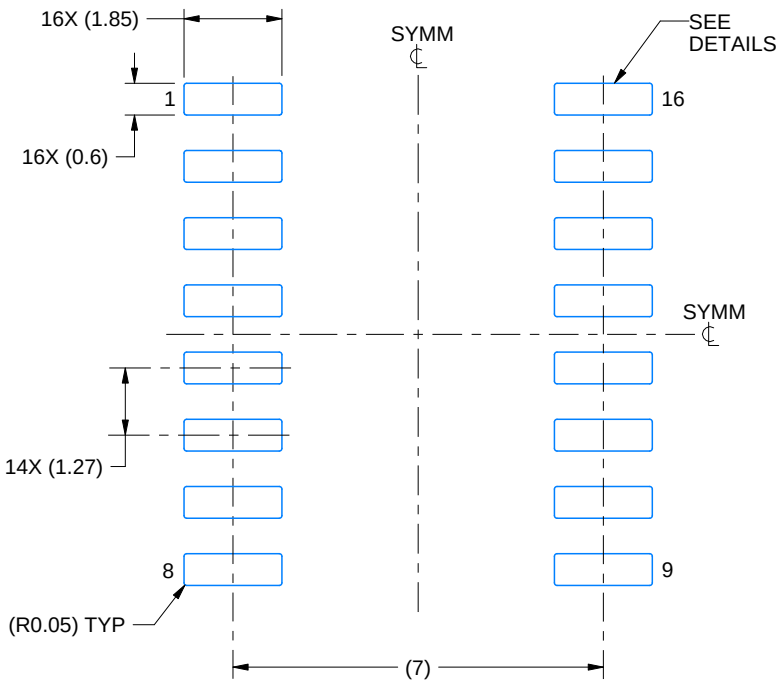
SOP - 2.00 mm max height

SOP

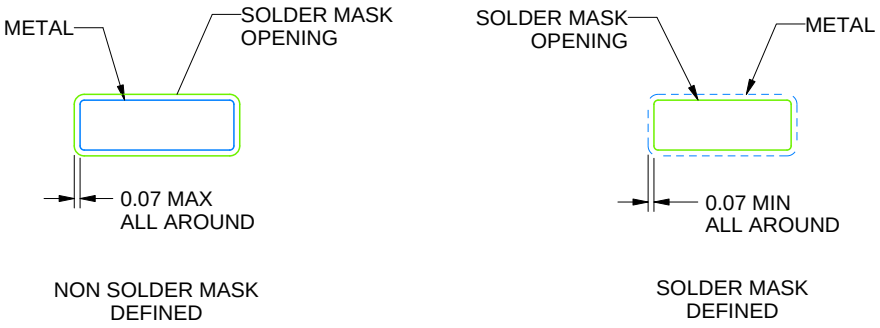


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

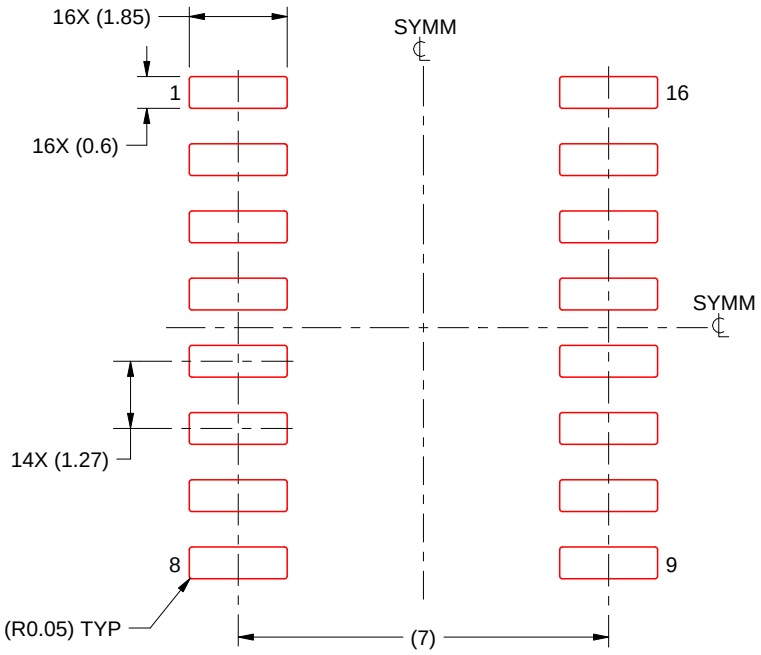
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



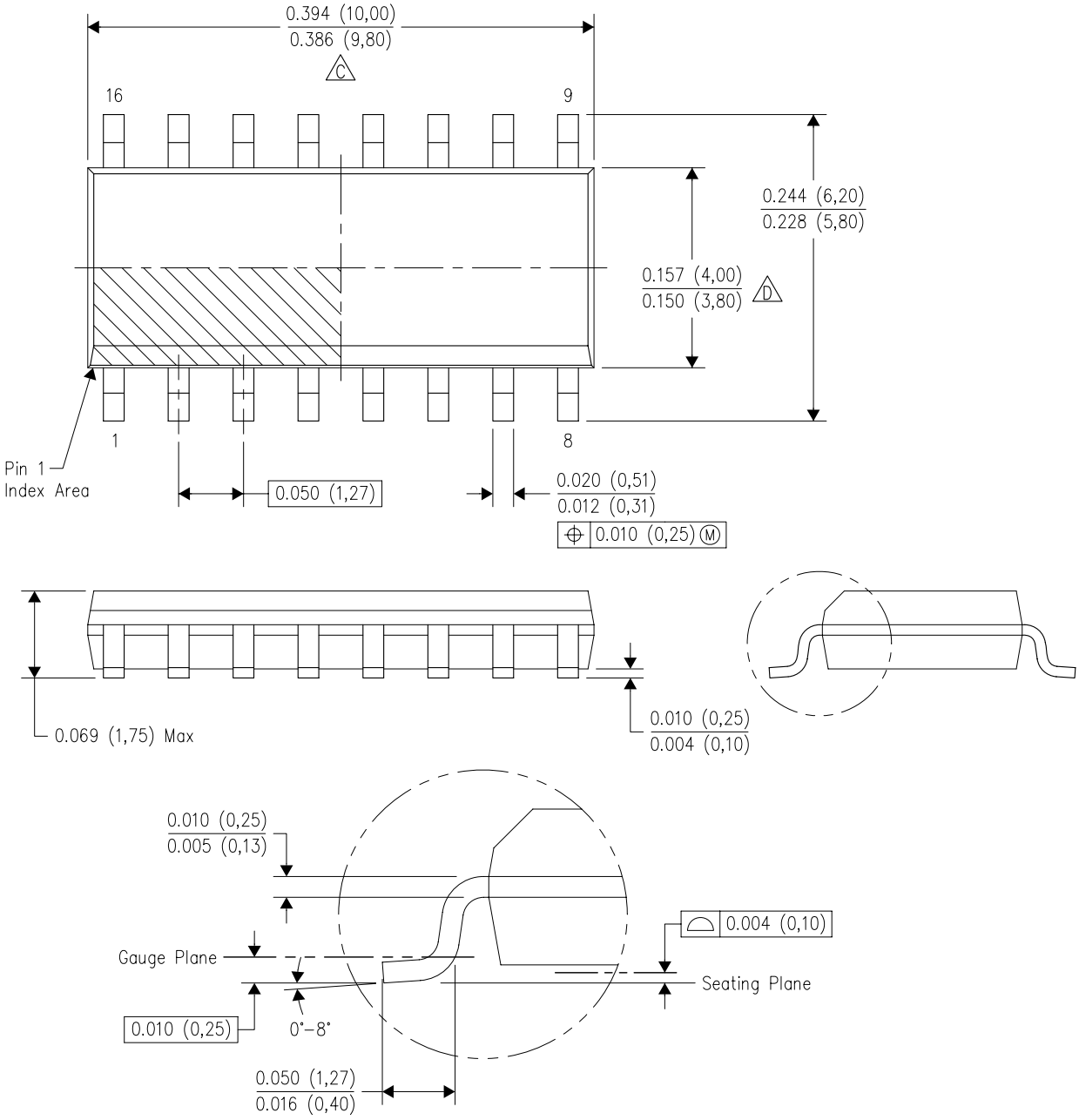
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



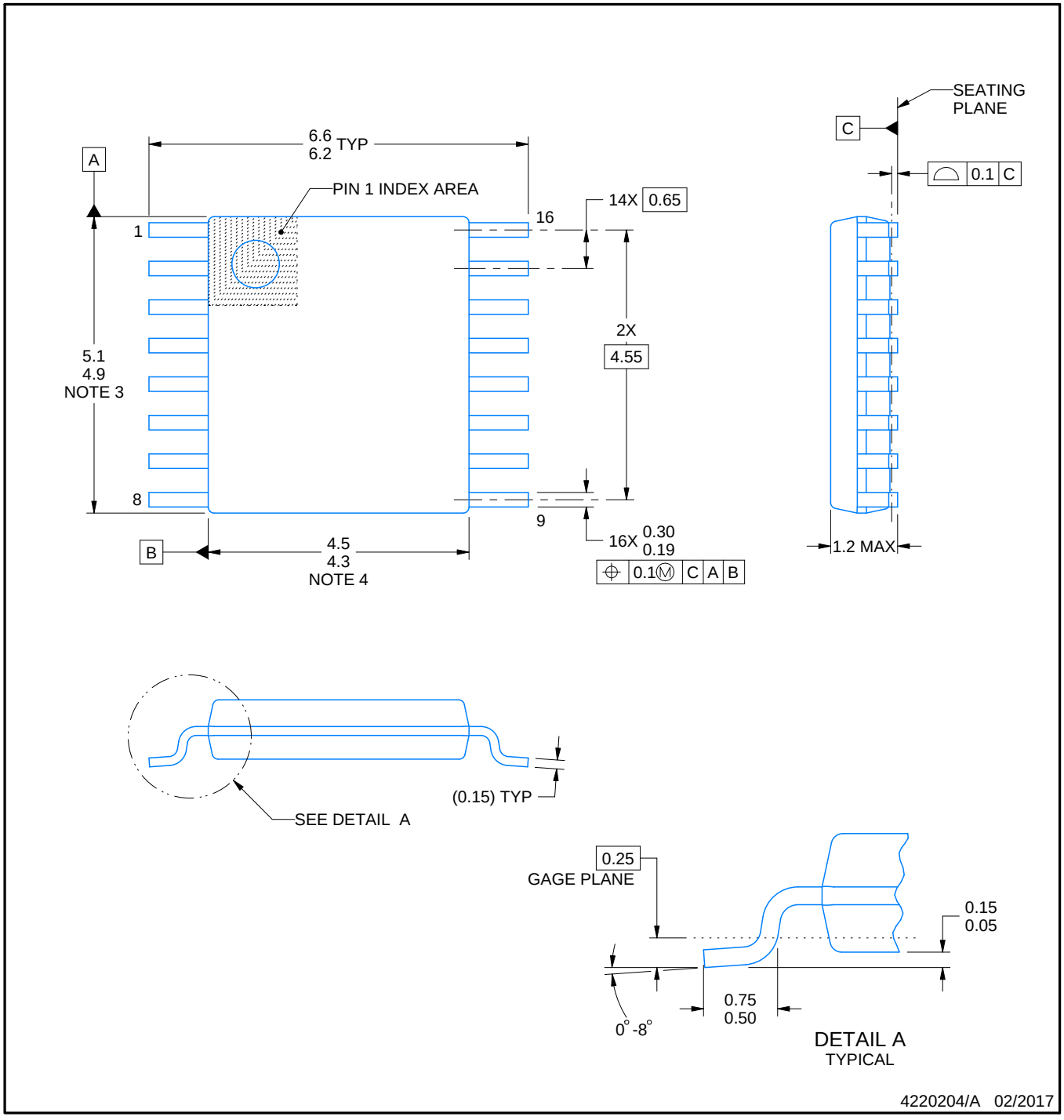
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

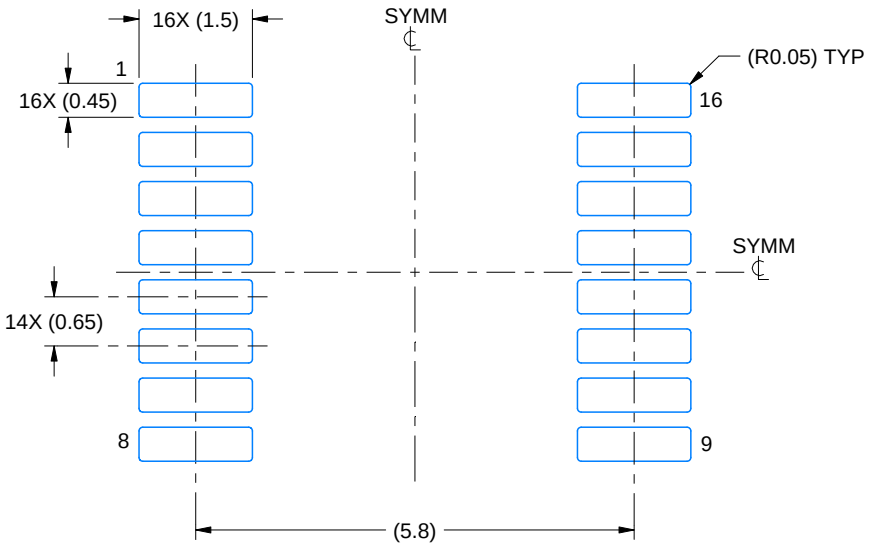
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

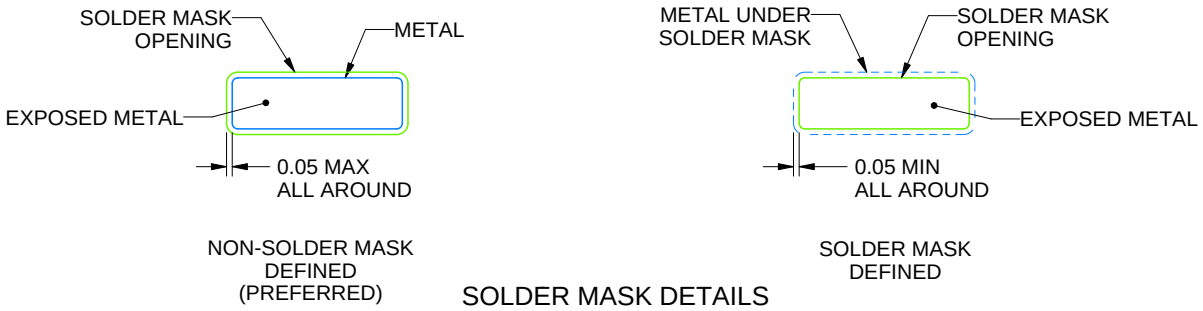


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

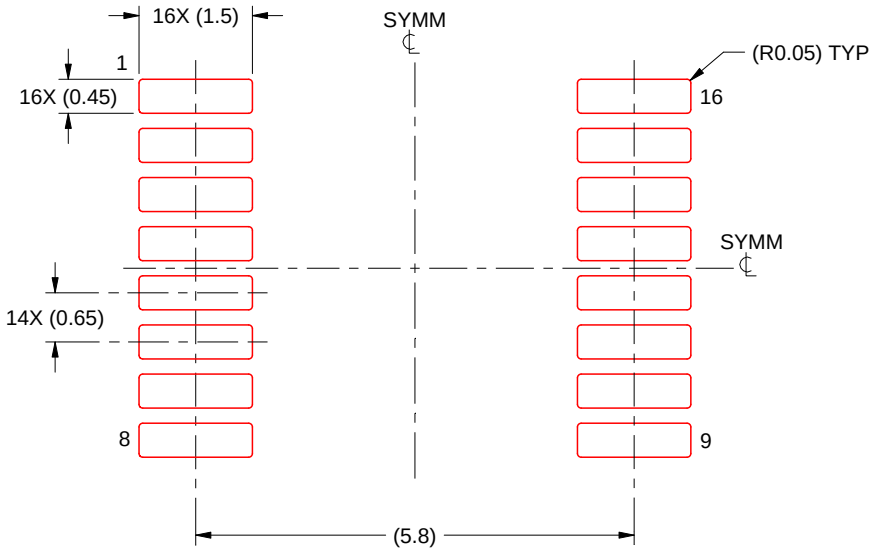


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

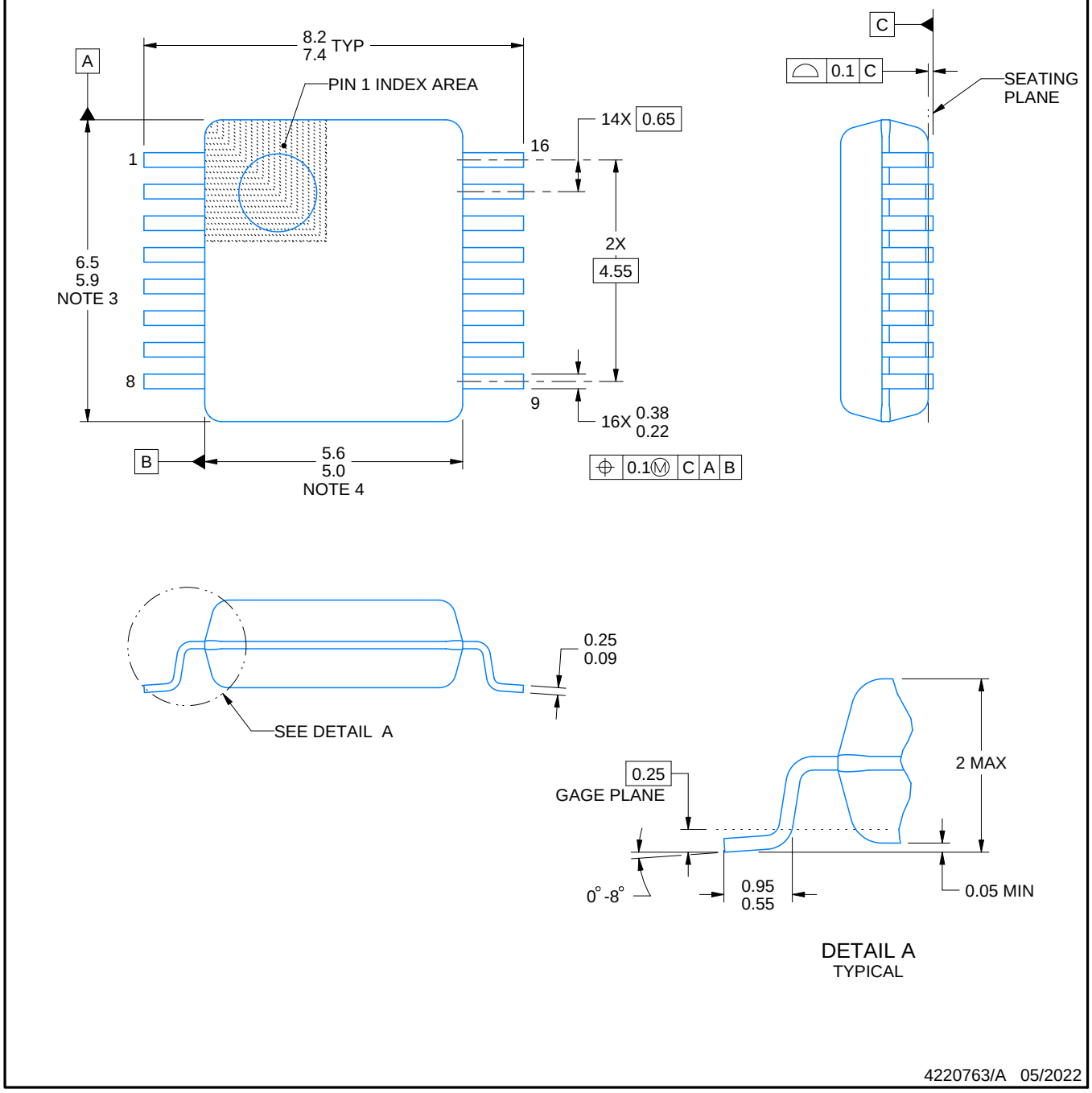
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

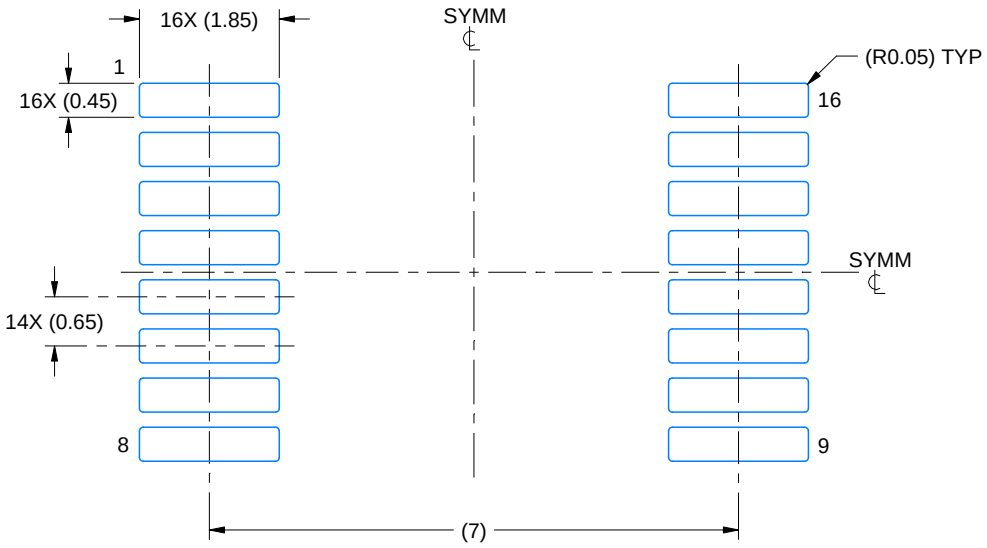
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

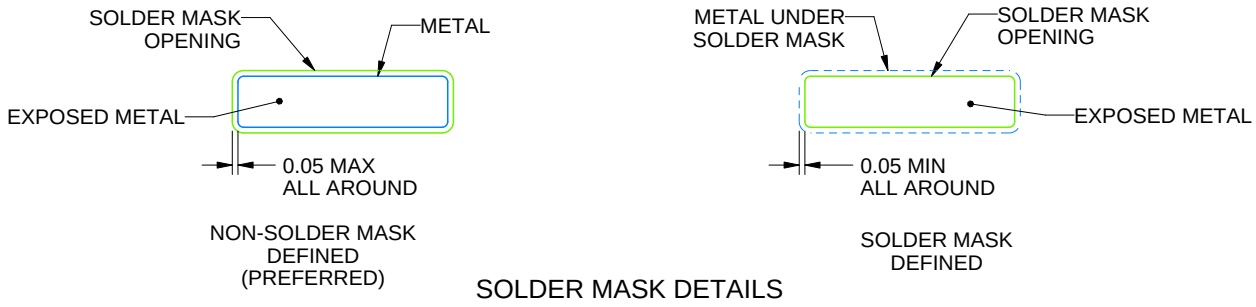


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

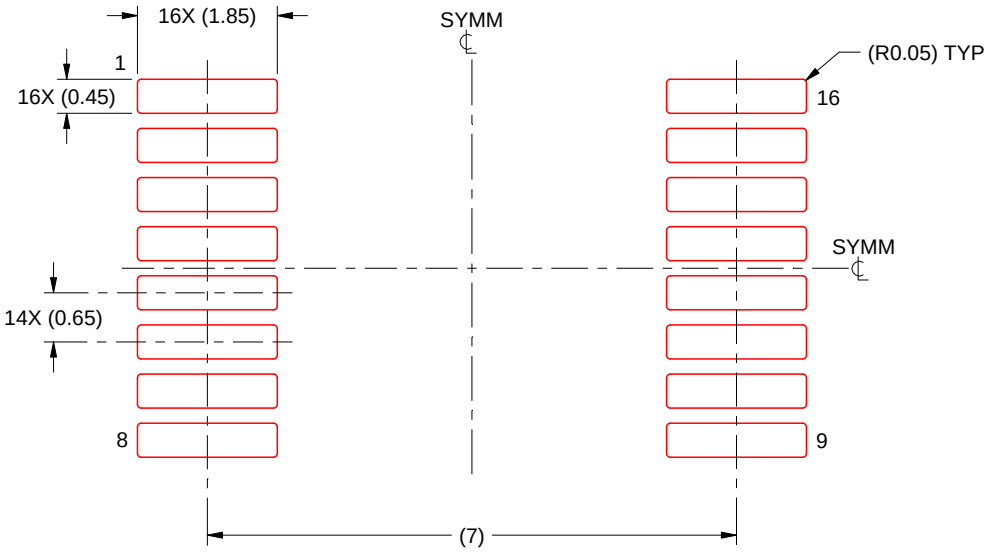


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

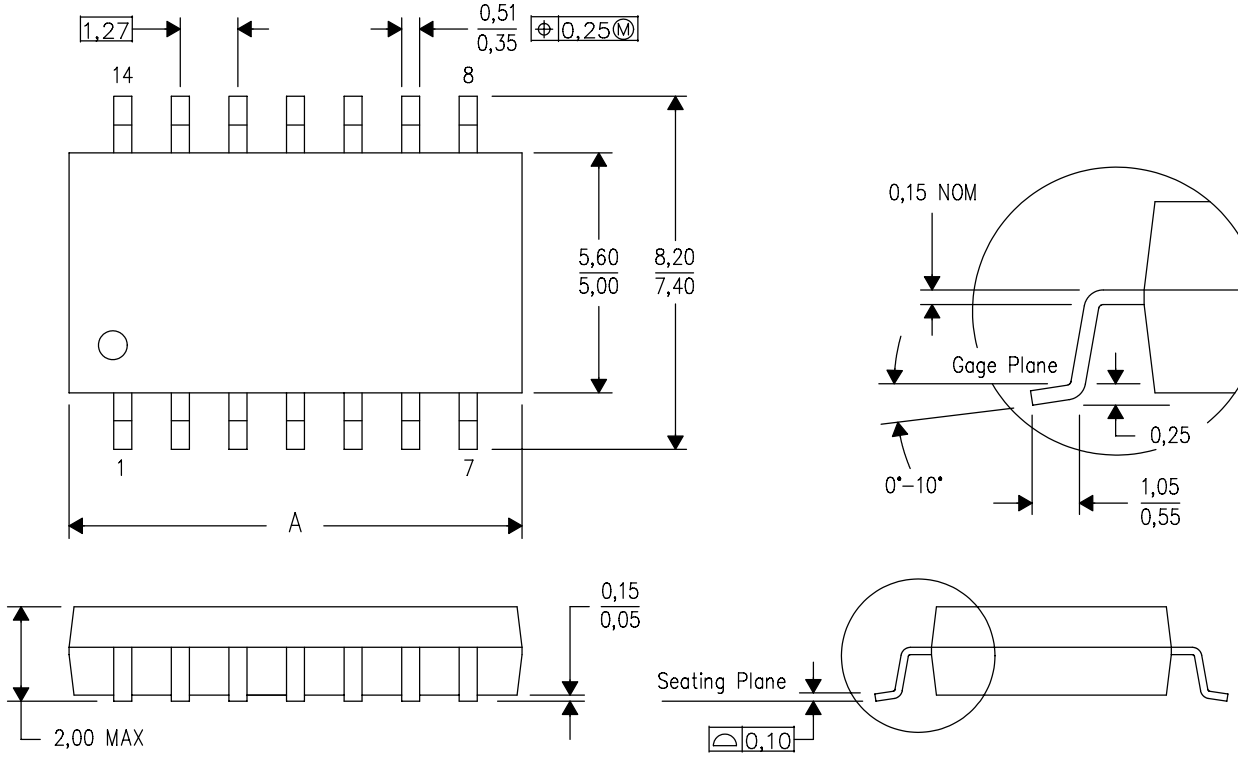
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

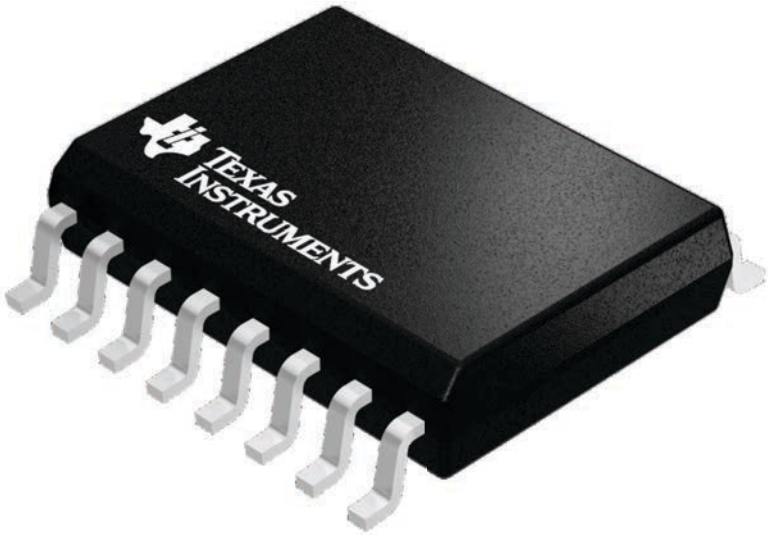
DW 16

SOIC - 2.65 mm max height

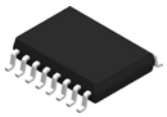
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

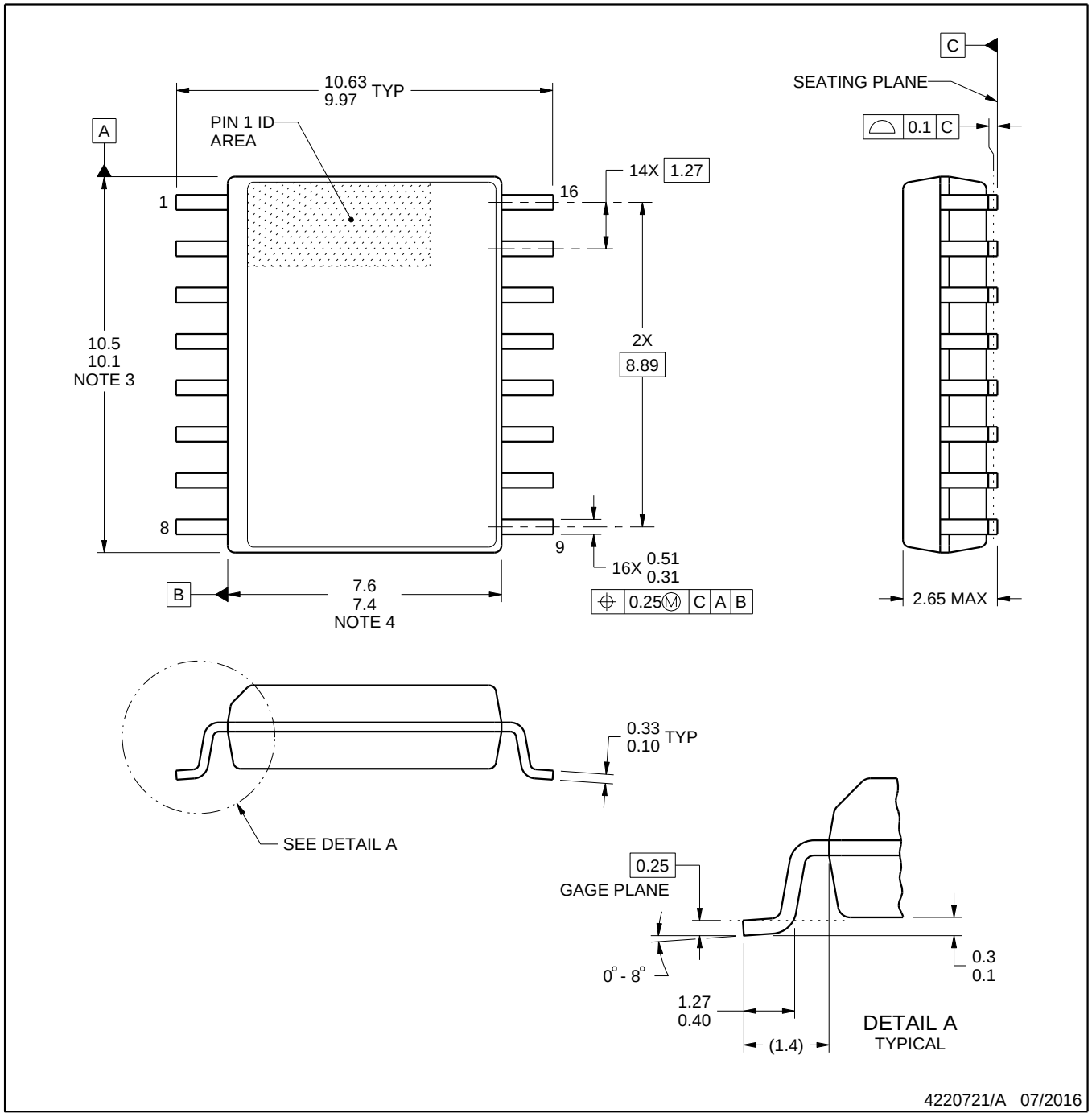


PACKAGE OUTLINE

DW0016A

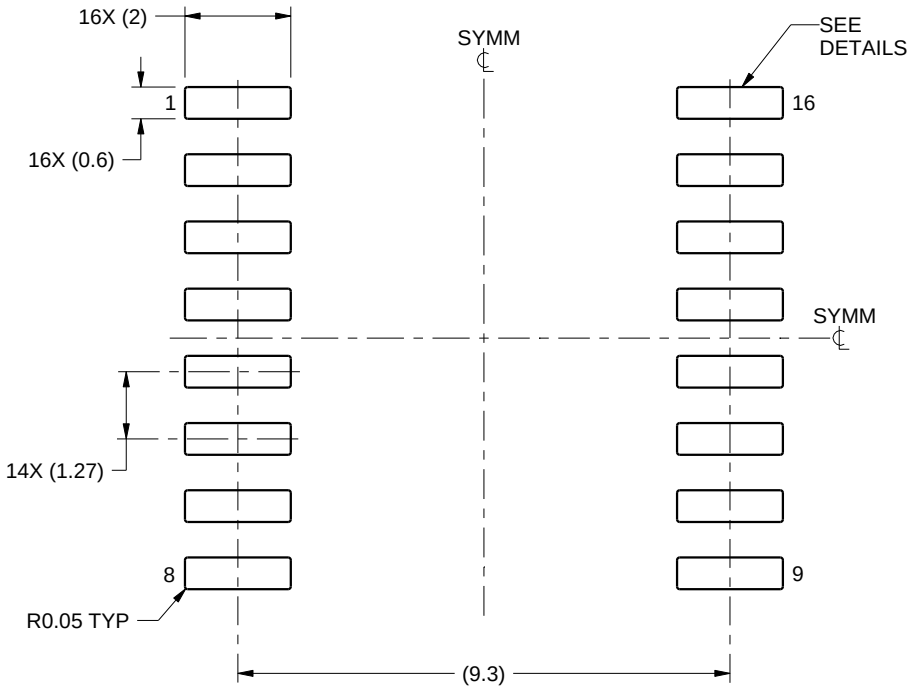
SOIC - 2.65 mm max height

SOIC

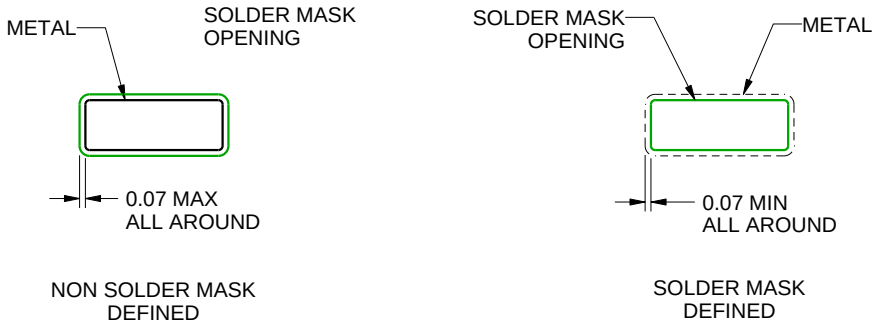


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

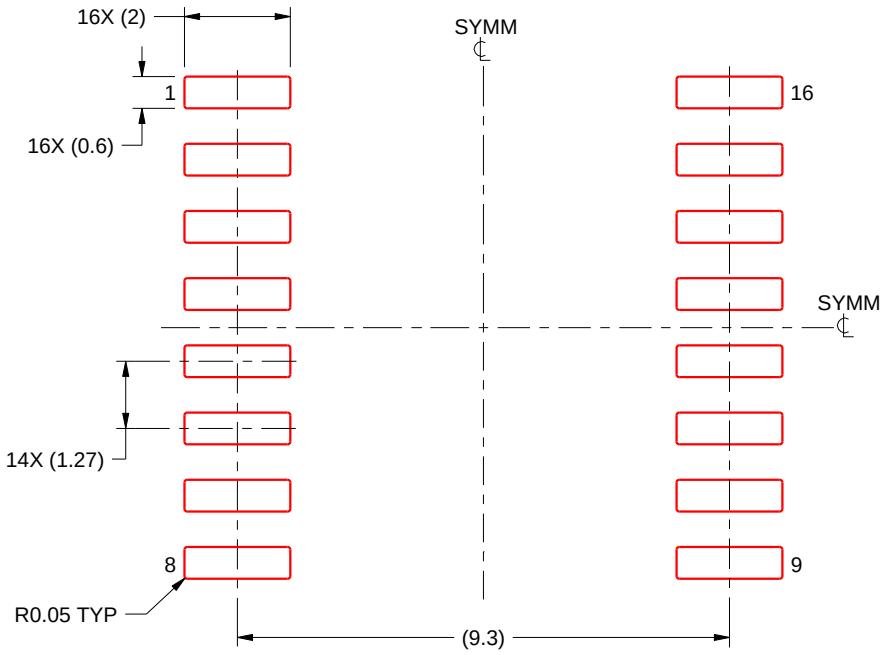


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



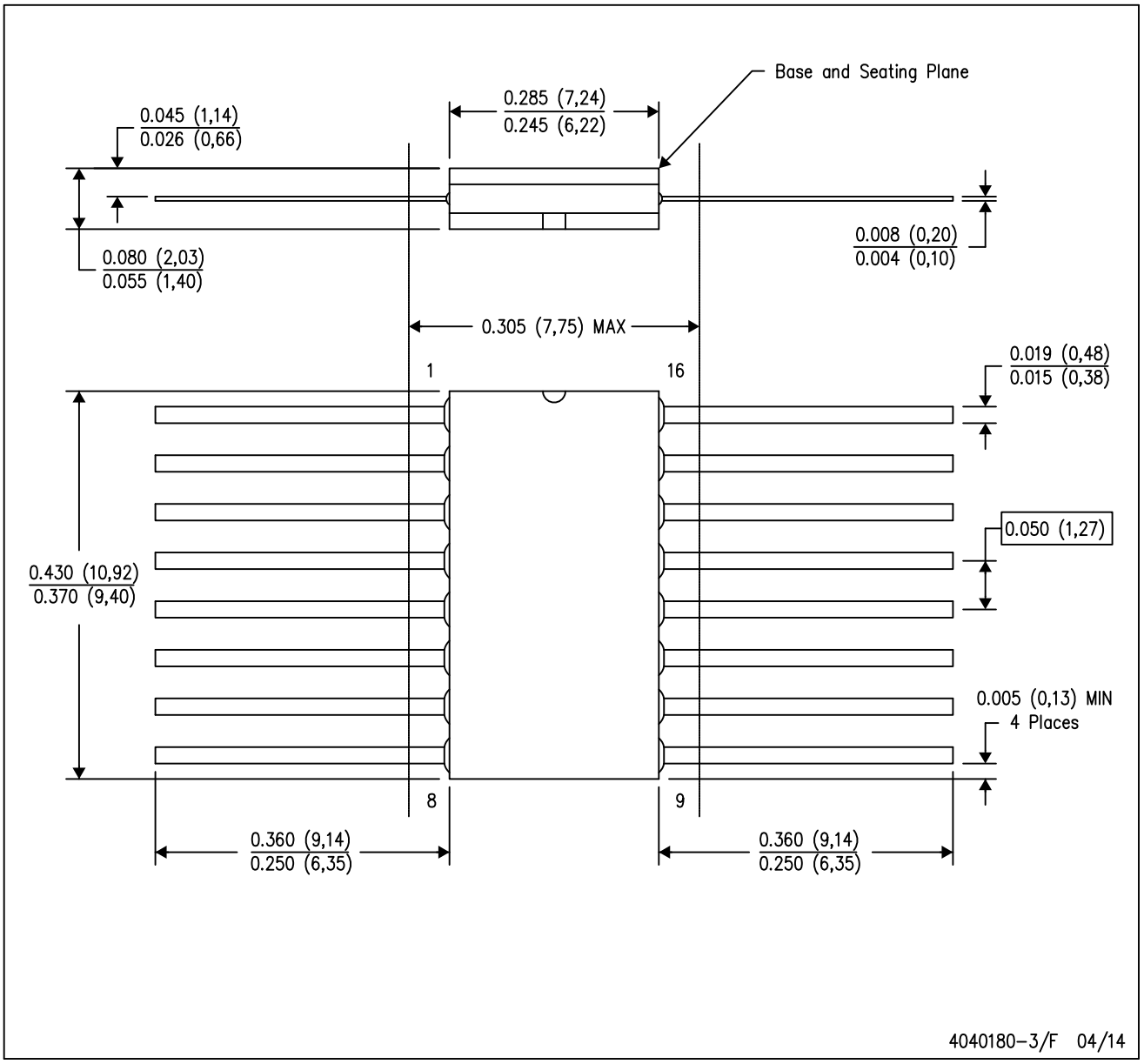
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

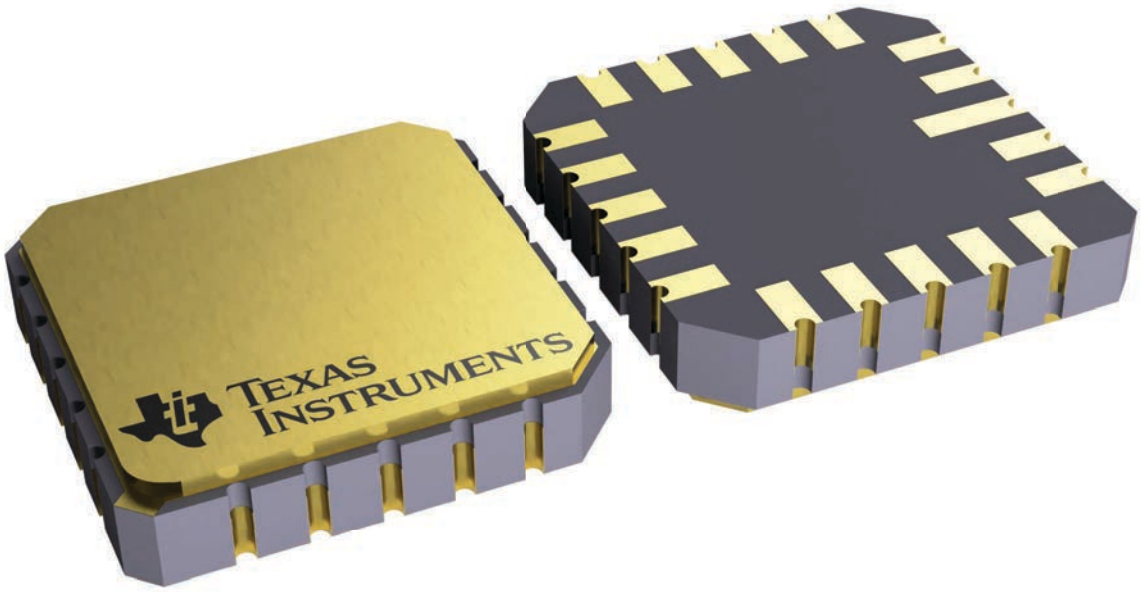
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

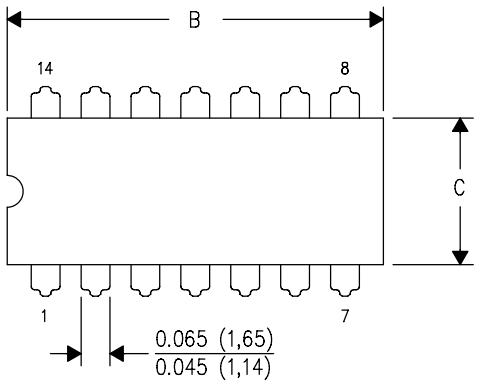


4229370VA\

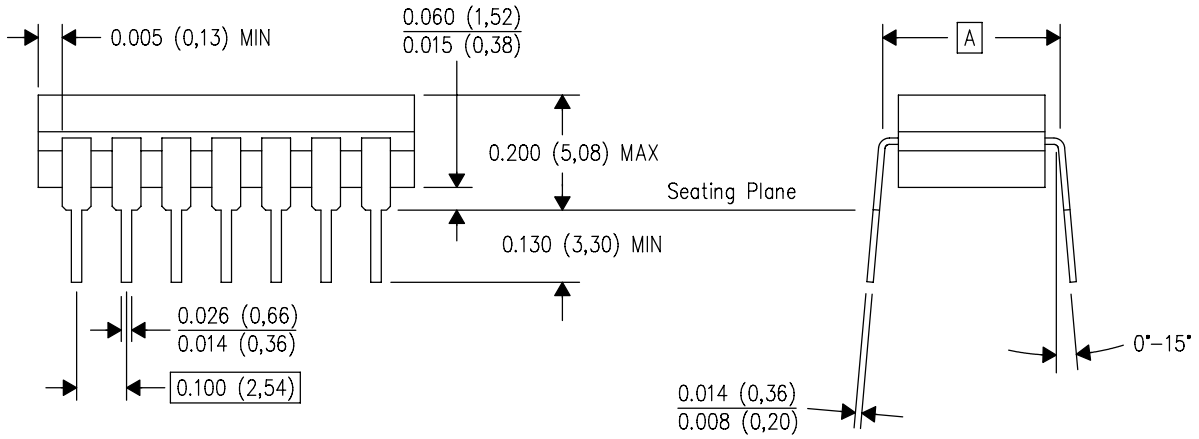
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



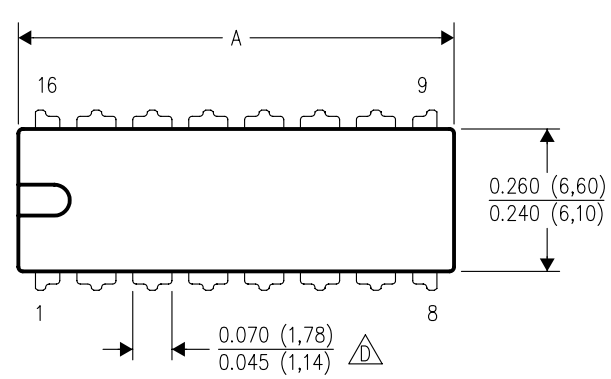
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

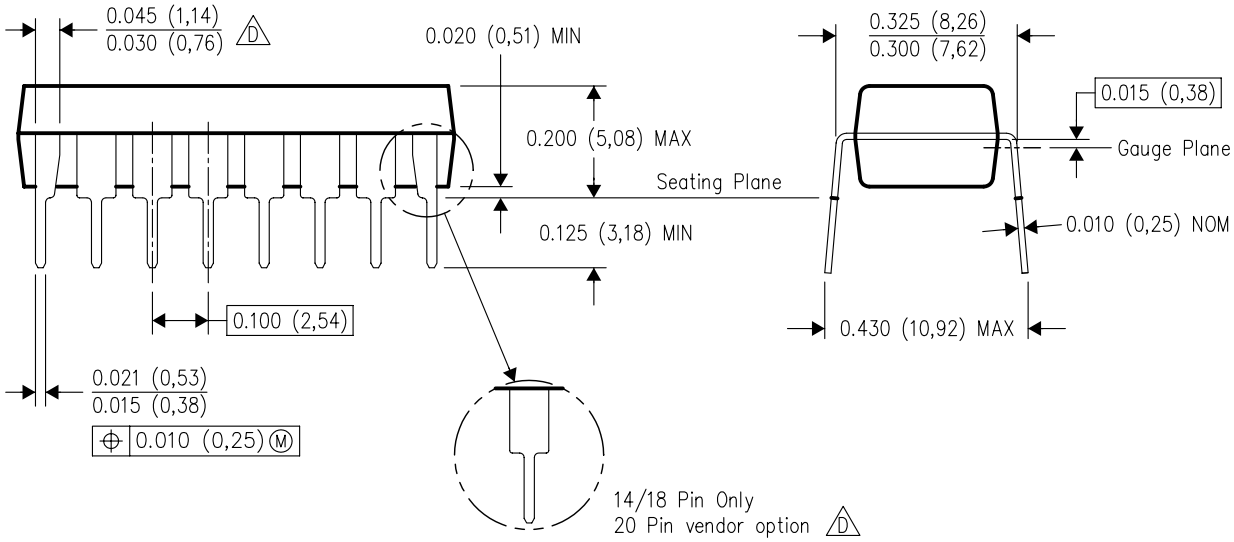
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265