

SNx4HC241 具有三态输出的八路缓冲器和线路驱动器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流输出可驱动多达 15 个 LSTTL 负载
- 低功耗， I_{CC} 最大值为 80 μ A
- 典型值 $t_{pd} = 11$ ns
- 电压为 5V 时，输出驱动为 ± 6 mA
- 低输出电流，最大值 1 μ A
- 三态输出驱动总线或缓冲存储器地址寄存器

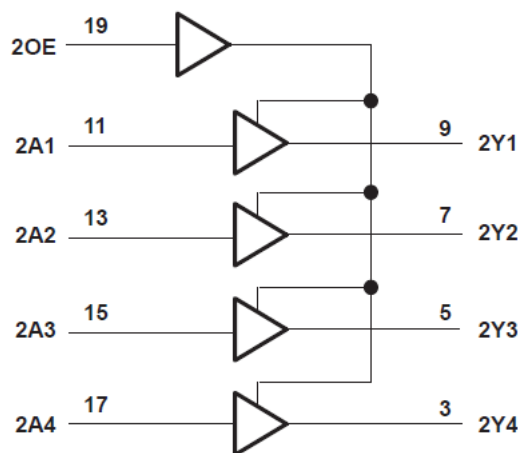
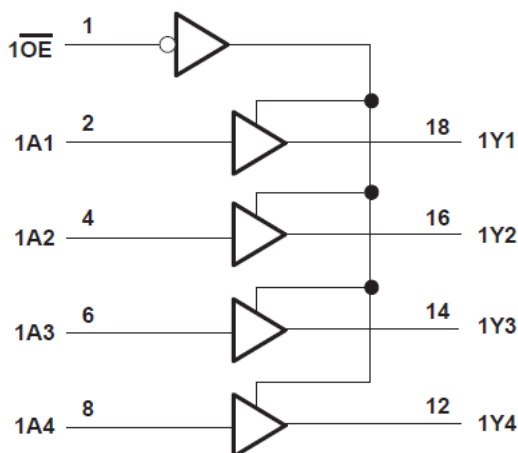
2 说明

这些八路缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。'HC241 器件可配置为两个具有独立输出使能 ($\overline{1OE}$ 和 $2OE$) 输入的 4 位缓冲器/驱动器。当 $\overline{1OE}$ 为低电平或 $2OE$ 为高电平时，该器件将来自 A 输入的同相数据传递到 Y 输出。当 $\overline{1OE}$ 为高电平或 $2OE$ 为低电平时，相应缓冲器/驱动器的输出处于高阻抗状态。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN74HC241DW	SOIC (20)	12.80mm × 7.50mm
SN74HC241N	PDIP (20)	25.40mm × 6.35mm
SN74HC241NSR	SO (20)	15.00mm × 5.30mm
SN74HC241PW	TSSOP (20)	6.50mm × 4.40mm
SN54HC241J	CDIP (20)	26.92mm × 6.92mm
SNJ54HC241FK	LCCC (20)	8.89mm × 8.45mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



Table of Contents

1 特性	1	7.1 Overview.....	8
2 说明	1	7.2 Functional Block Diagram.....	8
3 Revision History	2	7.3 Device Functional Modes.....	8
4 Pin Configuration and Functions	3	8 Power Supply Recommendations	9
5 Specifications	4	9 Layout	9
5.1 Absolute Maximum Ratings.....	4	9.1 Layout Guidelines.....	9
5.2 Recommended Operating Conditions ⁽¹⁾	4	10 Device and Documentation Support	10
5.3 Thermal Information.....	4	10.1 接收文档更新通知.....	10
5.4 Electrical Characteristics.....	5	10.2 支持资源.....	10
5.5 Switching Characteristics.....	5	10.3 Trademarks.....	10
5.6 Switching Characteristics.....	6	10.4 Electrostatic Discharge Caution.....	10
5.7 Operating Characteristics.....	6	10.5 术语表.....	10
6 Parameter Measurement Information	7	11 Mechanical, Packaging, and Orderable Information	10
7 Detailed Description	8		

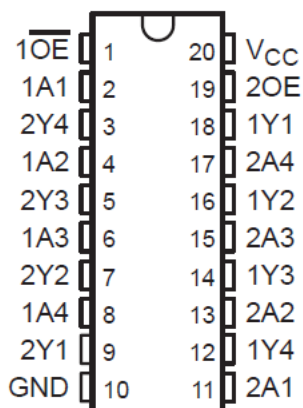
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

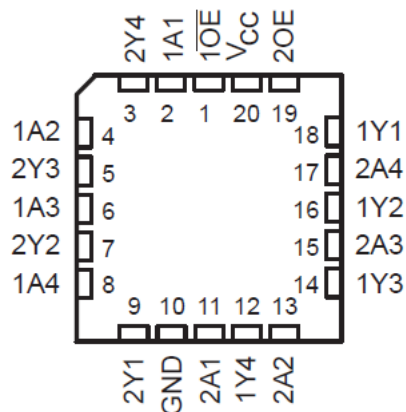
Changes from Revision D (January 2022) to Revision E (May 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, NS was 60 is now 113.4, PW was 83 is now 131.8.....	4

Changes from Revision C (August 2003) to Revision D (January 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1

4 Pin Configuration and Functions



J, DW, N, NS, or PW package
20-Pin CDIP, SOIC, PDIP, SO, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		- 0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 35	mA
	Continuous current through V_{CC} or GND			± 70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HC241			SN74HC241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5			1.5			V
		$V_{CC} = 4.5\text{ V}$	3.15			3.15			
		$V_{CC} = 6\text{ V}$	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5			0.5	V
		$V_{CC} = 4.5\text{ V}$			1.35			1.35	
		$V_{CC} = 6\text{ V}$			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t / \Delta v$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$			1000			1000	ns
		$V_{CC} = 4.5\text{ V}$			500			500	
		$V_{CC} = 6\text{ V}$			400			400	
T_A	Operating free-air temperature		-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	109.1	84.6	113.4	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	78.4	82.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	47.1	21.5	°C/W
ψ_{JB}	Junction-to-top characterization parameter	77.1	65.2	78.1	82.4	°C/W

5.3 Thermal Information (continued)

THERMAL METRIC		DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC} \text{ or } 0$		6 V		± 0.1	± 100		± 1000		± 1000	nA
I_{OZ}	$V_O = V_{CC} \text{ or } 0$		6 V		± 0.01	± 0.5		± 10		± 5	μA
I_{CC}	$V_I = V_{CC} \text{ or } 0$	$I_O = 0$	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

5.5 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		39	115		170		145	ns
			4.5 V		12	23		34		29	
			6 V		11	20		29		25	
t_{en}	$\overline{OE}$ or OE	Y	2 V		60	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		15	26		38		32	
t_{dis}	$\overline{OE}$ or OE	Y	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	165		245		210	ns
			4.5 V		16	33		49		42	
			6 V		14	28		42		35	
t_{en}	$\overline{OE}$ or OE	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

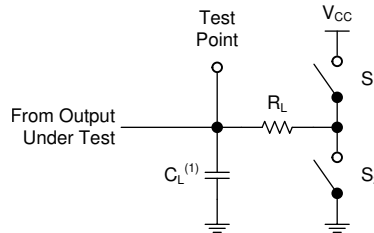
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f < 6 \text{ ns}$.

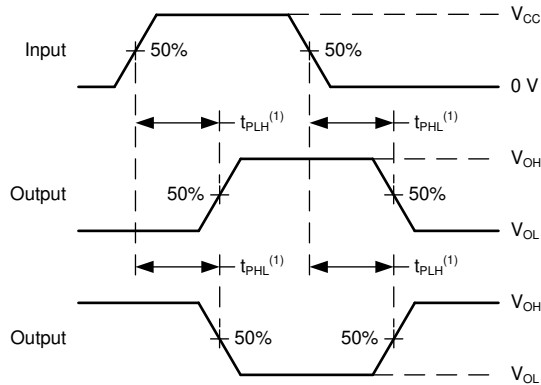
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



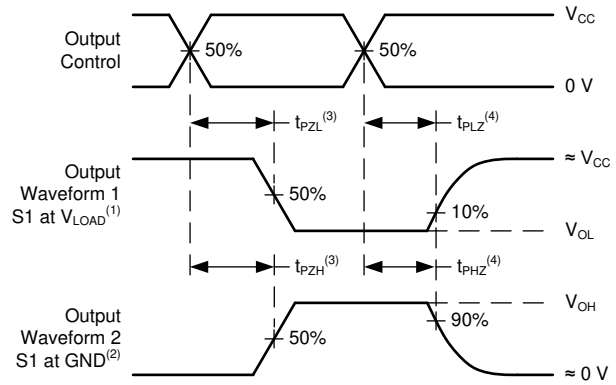
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

图 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



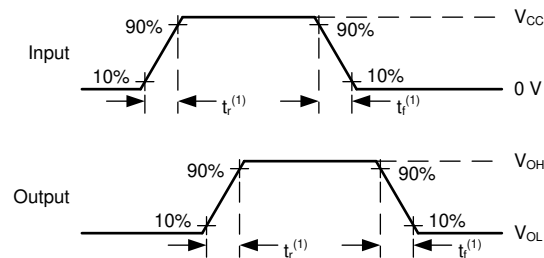
(1) S1 = CLOSED; S2 = OPEN.

(2) S1 = OPEN; S2 = CLOSED.

(3) t_{PZL} and t_{PHZ} are the same as t_{dis} .

(4) t_{PZL} and t_{PHZ} are the same as t_{en} .

图 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

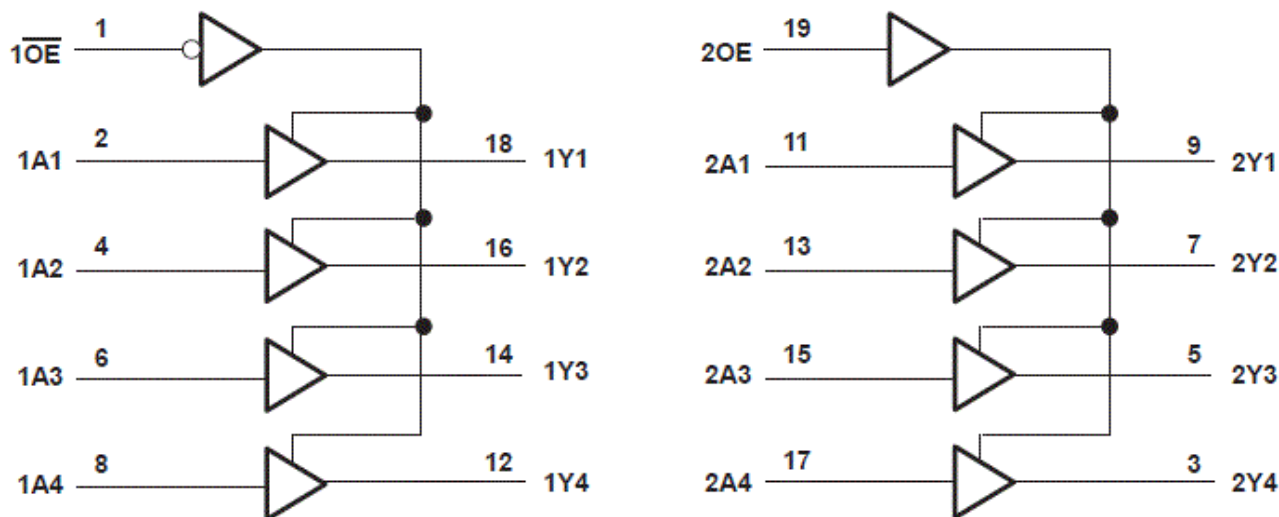
图 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

7 Detailed Description

7.1 Overview

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The ' HC241 devices are organized as two 4-bit buffers/drivers with separate output-enable ($1\overline{OE}$ and $2OE$) inputs. When $1\overline{OE}$ is low or $2OE$ is high, the device passes noninverted data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or $2OE$ is low, the outputs for the respective buffers/drivers are in the high-impedance state.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table

INPUTS		OUTPUT 1Y
$1\overline{OE}$	1A	
L	H	H
L	L	L
H	X	Z

表 7-2. Function Table

INPUTS		OUTPUT 2Y
$2OE$	2A	
H	H	H
H	L	L
L	X	Z

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/65704BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65704BRA
JM38510/65704BRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65704BRA
M38510/65704BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65704BRA
SN54HC241J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC241J
SN54HC241J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC241J
SN74HC241DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	HC241
SN74HC241DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241DWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC241N
SN74HC241N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC241N
SN74HC241NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HC241
SN74HC241PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SN74HC241PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC241
SNJ54HC241FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC 241FK
SNJ54HC241FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC 241FK
SNJ54HC241J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC241J
SNJ54HC241J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC241J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC241, SN74HC241 :

- Catalog : [SN74HC241](#)
- Military : [SN54HC241](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

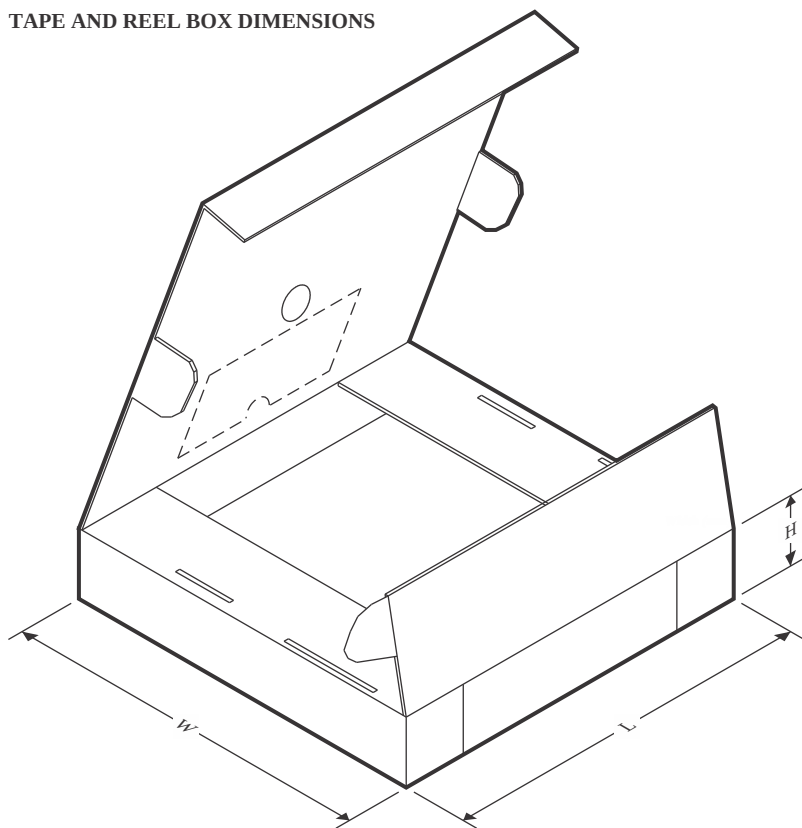
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC241DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC241NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC241PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

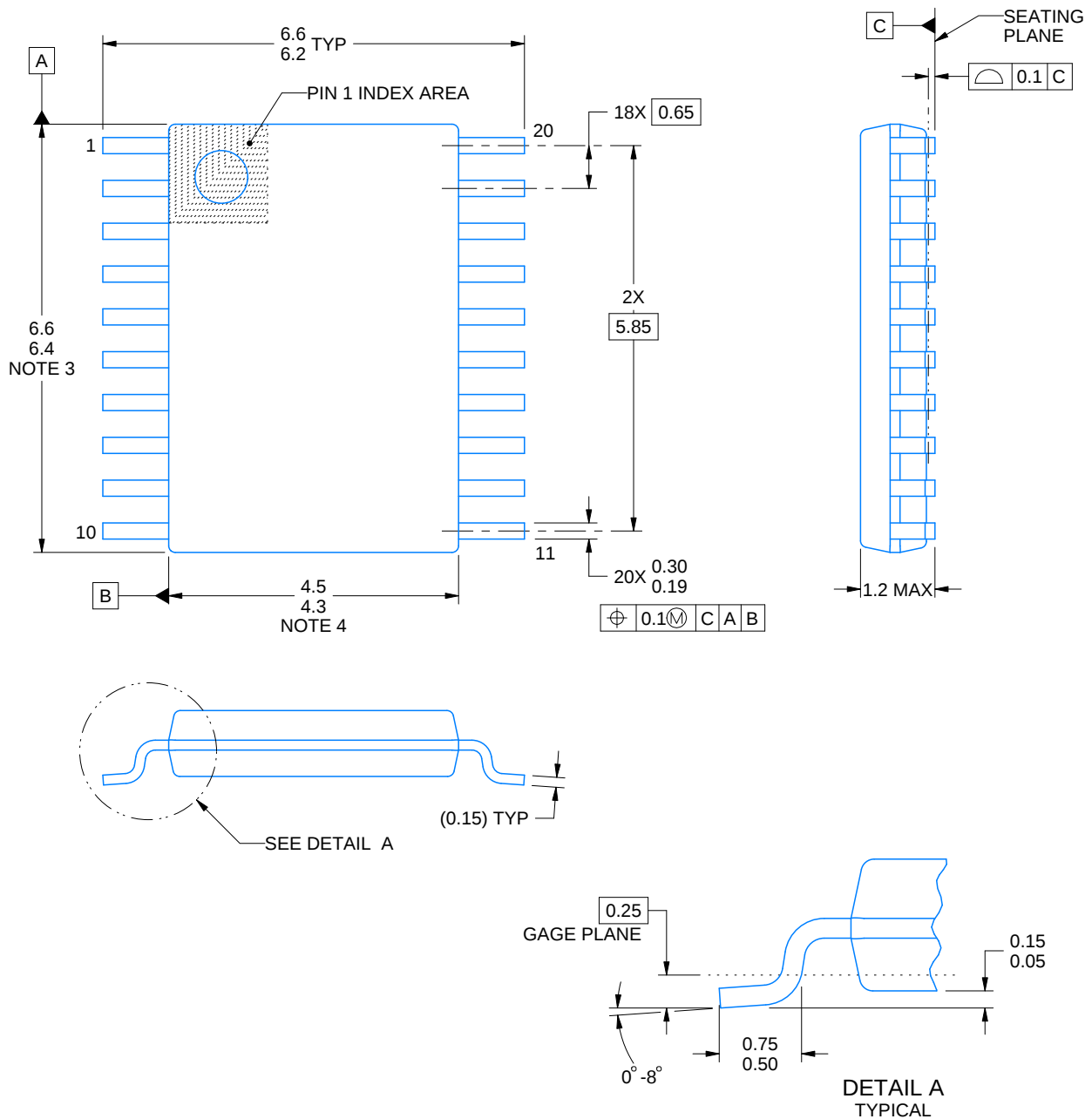
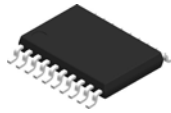
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC241DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC241DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC241NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74HC241PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC241N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC241N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC241FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC241FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA



4220206/A 02/2017

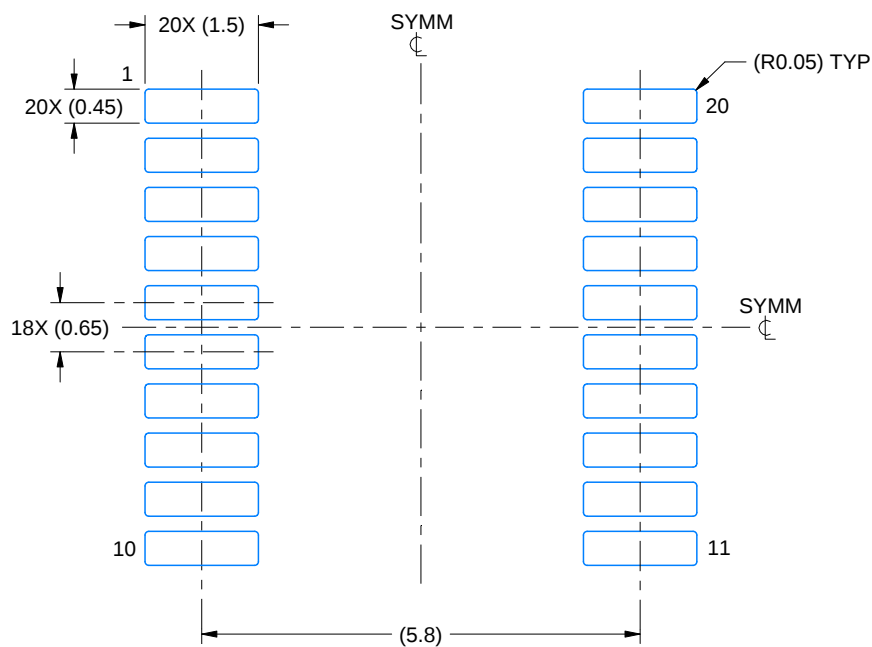
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

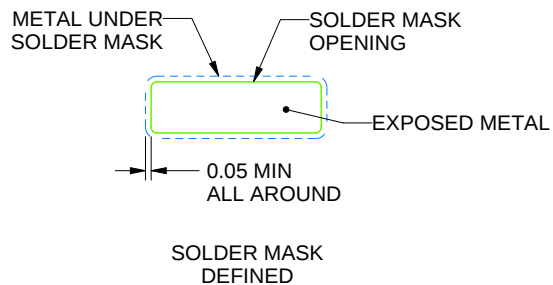
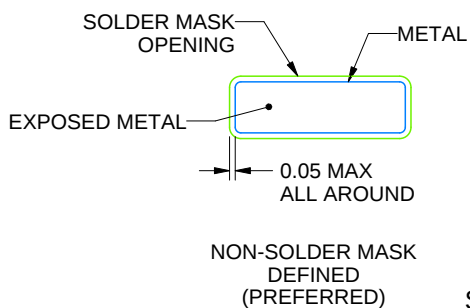
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

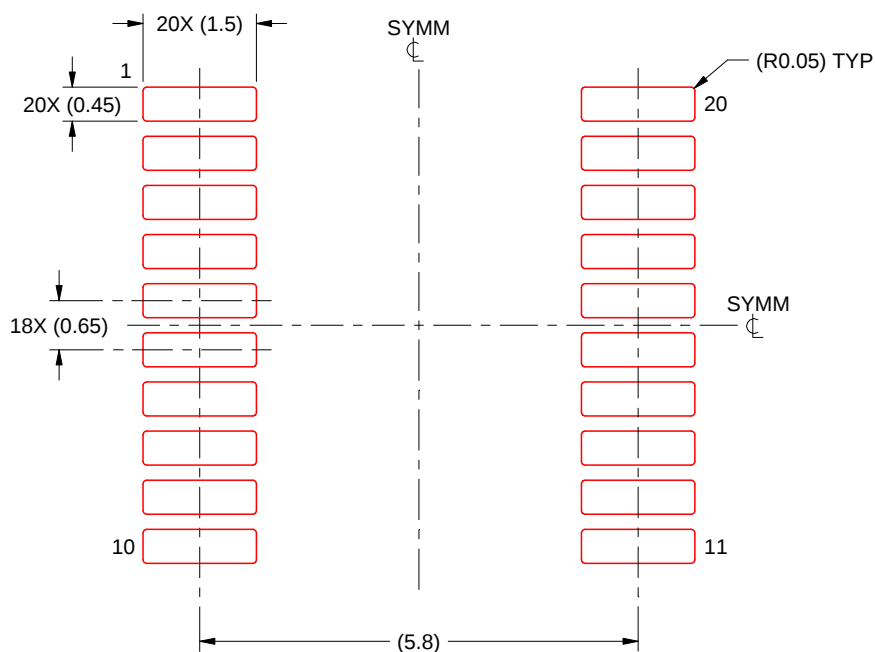
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

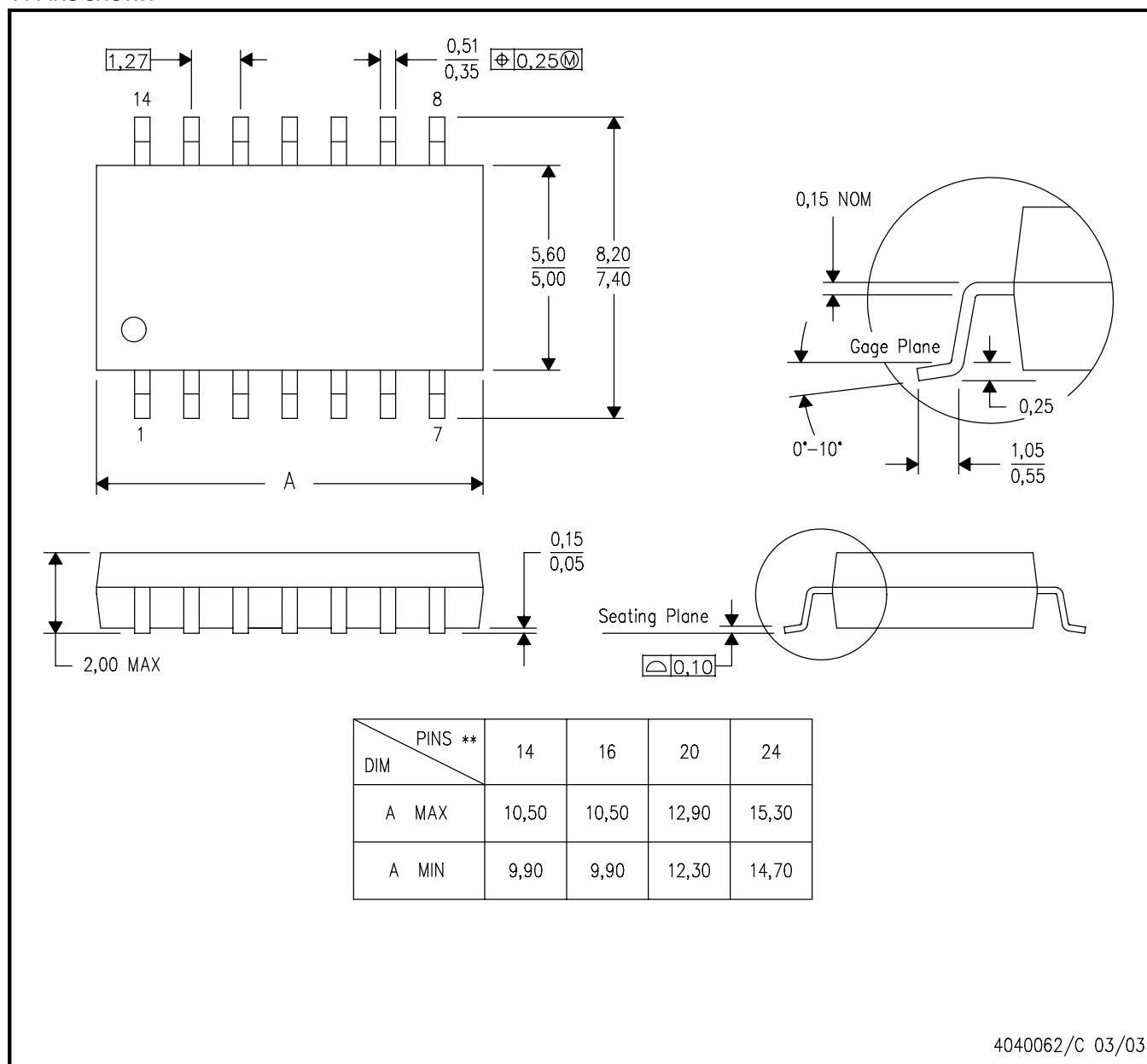
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

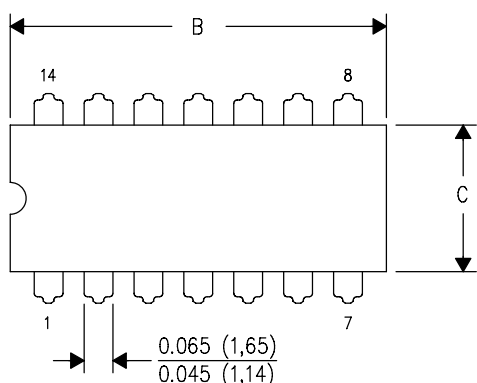


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

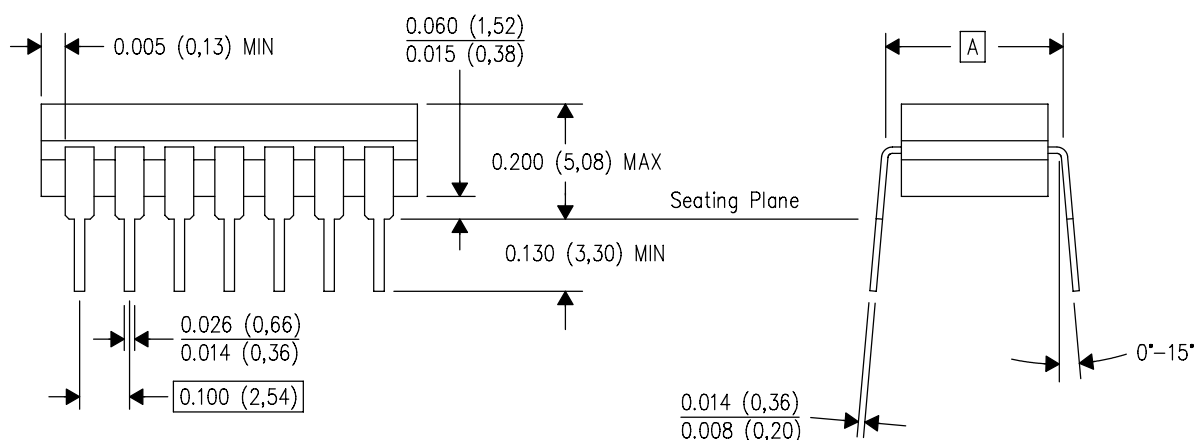
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

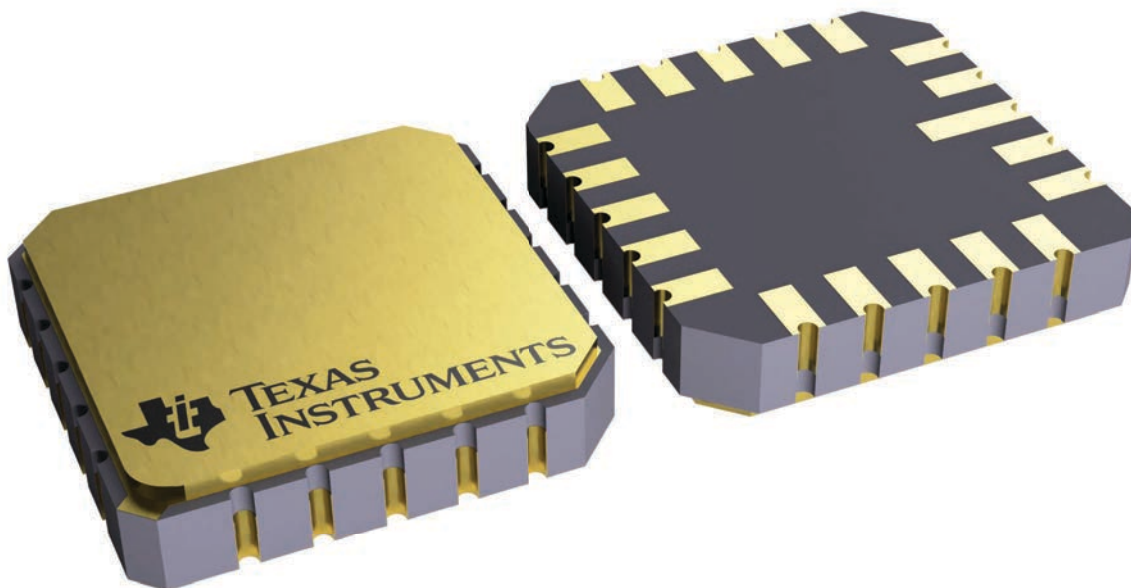
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

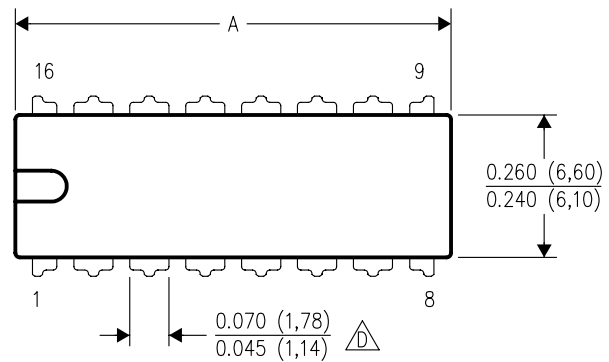


4229370VA\

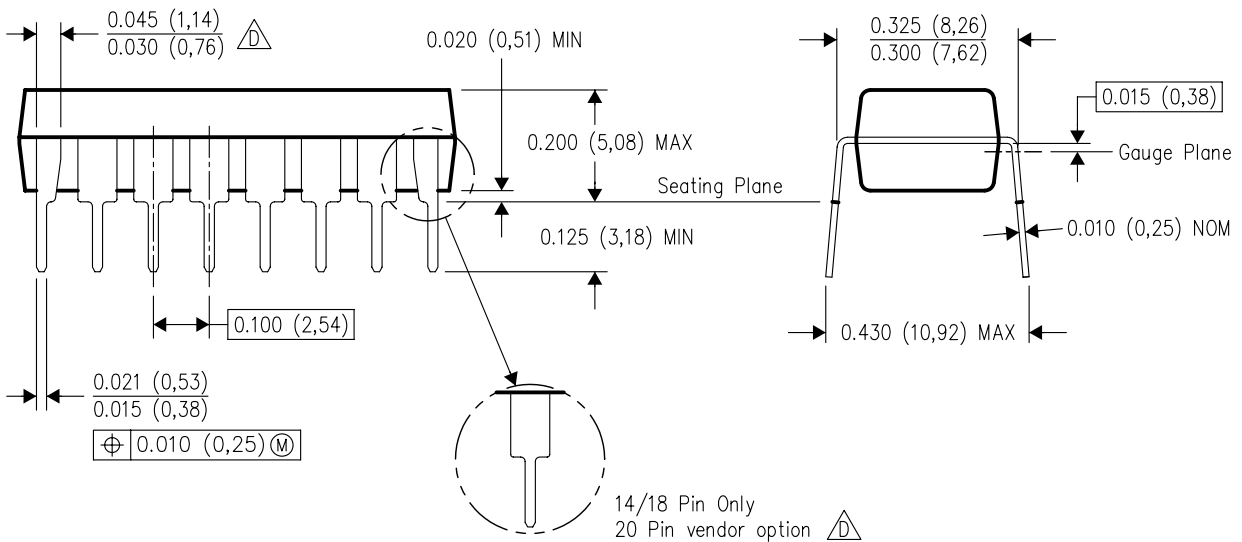
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



SOIC - 2.65 mm max height

Technical drawing of a 20-pin connector showing top, side, and detail views with dimensions and callouts.

Top View:

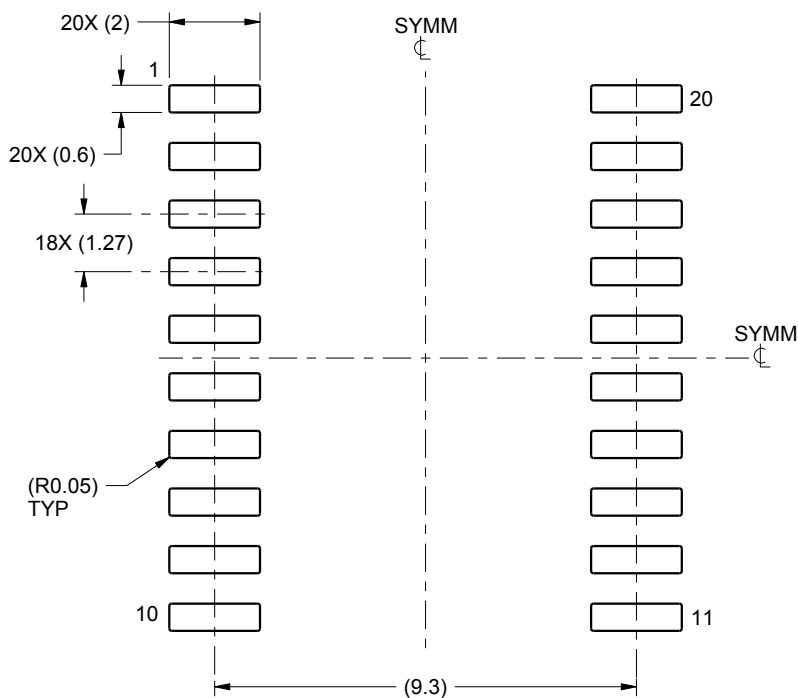
- Overall width: 10.63 (9.97 TYP)
- Overall height: 13.0 (12.6 NOTE 3)
- Pin 1 ID AREA (dotted pattern)
- Pin 1 location: 1
- Pin 10 location: 10
- Pin 11 location: 11
- Pin 20 location: 20
- Pin 18 location: 18X 1.27
- Pin 2 location: 2X 11.43
- Pin 20X location: 20X 0.51 0.31
- Pin 7.6 location: 7.6 (7.4 NOTE 4)
- Pin 10.63 location: 10.63 (9.97 TYP)
- Pin 13.0 location: 13.0 (12.6 NOTE 3)
- Pin 16.5 location: 16.5 (16.0 NOTE 3)
- Pin 19.5 location: 19.5 (19.0 NOTE 3)
- Pin 22.5 location: 22.5 (22.0 NOTE 3)
- Pin 25.5 location: 25.5 (25.0 NOTE 3)
- Pin 28.5 location: 28.5 (28.0 NOTE 3)
- Pin 31.5 location: 31.5 (31.0 NOTE 3)
- Pin 34.5 location: 34.5 (34.0 NOTE 3)
- Pin 37.5 location: 37.5 (37.0 NOTE 3)
- Pin 40.5 location: 40.5 (40.0 NOTE 3)
- Pin 43.5 location: 43.5 (43.0 NOTE 3)
- Pin 46.5 location: 46.5 (46.0 NOTE 3)
- Pin 49.5 location: 49.5 (49.0 NOTE 3)
- Pin 52.5 location: 52.5 (52.0 NOTE 3)
- Pin 55.5 location: 55.5 (55.0 NOTE 3)
- Pin 58.5 location: 58.5 (58.0 NOTE 3)
- Pin 61.5 location: 61.5 (61.0 NOTE 3)
- Pin 64.5 location: 64.5 (64.0 NOTE 3)
- Pin 67.5 location: 67.5 (67.0 NOTE 3)
- Pin 70.5 location: 70.5 (70.0 NOTE 3)
- Pin 73.5 location: 73.5 (73.0 NOTE 3)
- Pin 76.5 location: 76.5 (76.0 NOTE 3)
- Pin 79.5 location: 79.5 (79.0 NOTE 3)
- Pin 82.5 location: 82.5 (82.0 NOTE 3)
- Pin 85.5 location: 85.5 (85.0 NOTE 3)
- Pin 88.5 location: 88.5 (88.0 NOTE 3)
- Pin 91.5 location: 91.5 (91.0 NOTE 3)
- Pin 94.5 location: 94.5 (94.0 NOTE 3)
- Pin 97.5 location: 97.5 (97.0 NOTE 3)
- Pin 100.5 location: 100.5 (100.0 NOTE 3)
- Pin 103.5 location: 103.5 (103.0 NOTE 3)
- Pin 106.5 location: 106.5 (106.0 NOTE 3)
- Pin 109.5 location: 109.5 (109.0 NOTE 3)
- Pin 112.5 location: 112.5 (112.0 NOTE 3)
- Pin 115.5 location: 115.5 (115.0 NOTE 3)
- Pin 118.5 location: 118.5 (118.0 NOTE 3)
- Pin 121.5 location: 121.5 (121.0 NOTE 3)
- Pin 124.5 location: 124.5 (124.0 NOTE 3)
- Pin 127.5 location: 127.5 (127.0 NOTE 3)
- Pin 130.5 location: 130.5 (130.0 NOTE 3)
- Pin 133.5 location: 133.5 (133.0 NOTE 3)
- Pin 136.5 location: 136.5 (136.0 NOTE 3)
- Pin 139.5 location: 139.5 (139.0 NOTE 3)
- Pin 142.5 location: 142.5 (142.0 NOTE 3)
- Pin 145.5 location: 145.5 (145.0 NOTE 3)
- Pin 148.5 location: 148.5 (148.0 NOTE 3)
- Pin 151.5 location: 151.5 (151.0 NOTE 3)
- Pin 154.5 location: 154.5 (154.0 NOTE 3)
- Pin 157.5 location: 157.5 (157.0 NOTE 3)
- Pin 160.5 location: 160.5 (160.0 NOTE 3)
- Pin 163.5 location: 163.5 (163.0 NOTE 3)
- Pin 166.5 location: 166.5 (166.0 NOTE 3)
- Pin 169.5 location: 169.5 (169.0 NOTE 3)
- Pin 172.5 location: 172.5 (172.0 NOTE 3)
- Pin 175.5 location: 175.5 (175.0 NOTE 3)
- Pin 178.5 location: 178.5 (178.0 NOTE 3)
- Pin 181.5 location: 181.5 (181.0 NOTE 3)
- Pin 184.5 location: 184.5 (184.0 NOTE 3)
- Pin 187.5 location: 187.5 (187.0 NOTE 3)
- Pin 190.5 location: 190.5 (190.0 NOTE 3)
- Pin 193.5 location: 193.5 (193.0 NOTE 3)
- Pin 196.5 location: 196.5 (196.0 NOTE 3)
- Pin 199.5 location: 199.5 (199.0 NOTE 3)
- Pin 202.5 location: 202.5 (202.0 NOTE 3)
- Pin 205.5 location: 205.5 (205.0 NOTE 3)
- Pin 208.5 location: 208.5 (208.0 NOTE 3)
- Pin 211.5 location: 211.5 (211.0 NOTE 3)
- Pin 214.5 location: 214.5 (214.0 NOTE 3)
- Pin 217.5 location: 217.5 (217.0 NOTE 3)
- Pin 220.5 location: 220.5 (220.0 NOTE 3)
- Pin 223.5 location: 223.5 (223.0 NOTE 3)
- Pin 226.5 location: 226.5 (226.0 NOTE 3)
- Pin 229.5 location: 229.5 (229.0 NOTE 3)
- Pin 232.5 location: 232.5 (232.0 NOTE 3)
- Pin 235.5 location: 235.5 (235.0 NOTE 3)
- Pin 238.5 location: 238.5 (238.0 NOTE 3)
- Pin 241.5 location: 241.5 (241.0 NOTE 3)
- Pin 244.5 location: 244.5 (244.0 NOTE 3)
- Pin 247.5 location: 247.5 (247.0 NOTE 3)
- Pin 250.5 location: 250.5 (250.0 NOTE 3)
- Pin 253.5 location: 253.5 (253.0 NOTE 3)
- Pin 256.5 location: 256.5 (256.0 NOTE 3)
- Pin 259.5 location: 259.5 (259.0 NOTE 3)
- Pin 262.5 location: 262.5 (262.0 NOTE 3)
- Pin 265.5 location: 265.5 (265.0 NOTE 3)
- Pin 268.5 location: 268.5 (268.0 NOTE 3)
- Pin 271.5 location: 271.5 (271.0 NOTE 3)
- Pin 274.5 location: 274.5 (274.0 NOTE 3)
- Pin 277.5 location: 277.5 (277.0 NOTE 3)
- Pin 280.5 location: 280.5 (280.0 NOTE 3)
- Pin 283.5 location: 283.5 (283.0 NOTE 3)
- Pin 286.5 location: 286.5 (286.0 NOTE 3)
- Pin 289.5 location: 289.5 (289.0 NOTE 3)
- Pin 292.5 location: 292.5 (292.0 NOTE 3)
- Pin 295.5 location: 295.5 (295.0 NOTE 3)
- Pin 298.5 location: 298.5 (298.0 NOTE 3)
- Pin 301.5 location: 301.5 (301.0 NOTE 3)
- Pin 304.5 location: 304.5 (304.0 NOTE 3)
- Pin 307.5 location: 307.5 (307.0 NOTE 3)
- Pin 310.5 location: 310.5 (310.0 NOTE 3)
- Pin 313.5 location: 313.5 (313.0 NOTE 3)
- Pin 316.5 location: 316.5 (316.0 NOTE 3)
- Pin 319.5 location: 319.5 (319.0 NOTE 3)
- Pin 322.5 location: 322.5 (322.0 NOTE 3)
- Pin 325.5 location: 325.5 (325.0 NOTE 3)
- Pin 328.5 location: 328.5 (328.0 NOTE 3)
- Pin 331.5 location: 331.5 (331.0 NOTE 3)
- Pin 334.5 location: 334.5 (334.0 NOTE 3)
- Pin 337.5 location: 337.5 (337.0 NOTE 3)
- Pin 340.5 location: 340.5 (340.0 NOTE 3)
- Pin 343.5 location: 343.5 (343.0 NOTE 3)
- Pin 346.5 location: 346.5 (346.0 NOTE 3)
- Pin 349.5 location: 349.5 (349.0 NOTE 3)
- Pin 352.5 location: 352.5 (352.0 NOTE 3)
- Pin 355.5 location: 355.5 (355.0 NOTE 3)
- Pin 358.5 location: 358.5 (358.0 NOTE 3)
- Pin 361.5 location: 361.5 (361.0 NOTE 3)
- Pin 364.5 location: 364.5 (364.0 NOTE 3)
- Pin 367.5 location: 367.5 (367.0 NOTE 3)
- Pin 370.5 location: 370.5 (370.0 NOTE 3)
- Pin 373.5 location: 373.5 (373.0 NOTE 3)
- Pin 376.5 location: 376.5 (376.0 NOTE 3)
- Pin 379.5 location: 379.5 (379.0 NOTE 3)
- Pin 382.5 location: 382.5 (382.0 NOTE 3)
- Pin 385.5 location: 385.5 (385.0 NOTE 3)
- Pin 388.5 location: 388.5 (388.0 NOTE 3)
- Pin 391.5 location: 391.5 (391.0 NOTE 3)
- Pin 394.5 location: 394.5 (394.0 NOTE 3)
- Pin 397.5 location: 397.5 (397.0 NOTE 3)
- Pin 4

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

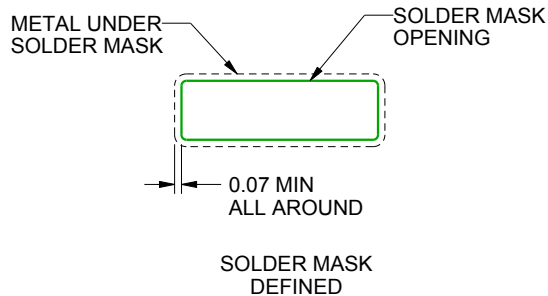
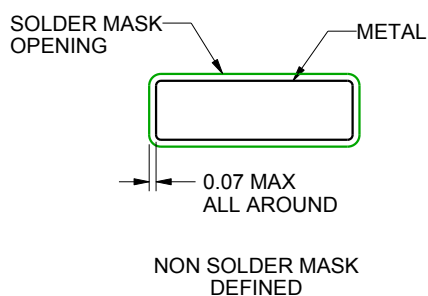
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

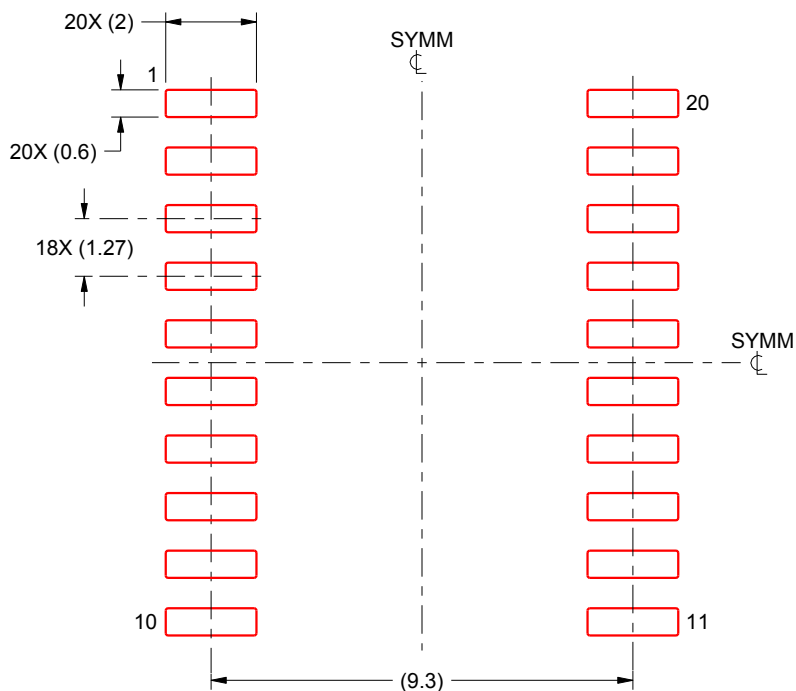
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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