

# SN74HC193-Q1

## 4-BIT SYNCHRONOUS UP/DOWN COUNTER (DUAL CLOCK WITH CLEAR)

SCLS594A – NOVEMBER 2004 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 20$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

### description/ordering information

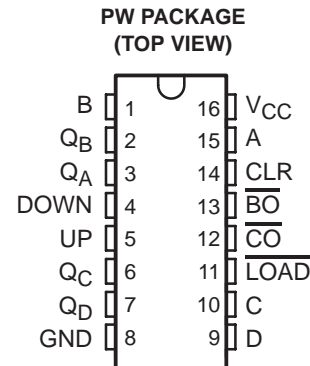
The SN74HC193 device is a 4-bit synchronous, reversible, up/down binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously with each other when dictated by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ( $\overline{LOAD}$ ) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and  $\overline{LOAD}$  inputs.

This counter was designed to be cascaded without the need for external circuitry. The borrow ( $\overline{BO}$ ) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ( $\overline{CO}$ ) output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counter then can be cascaded easily by feeding  $\overline{BO}$  and  $\overline{CO}$  to DOWN and UP, respectively, of the succeeding counter.



### ORDERING INFORMATION<sup>†</sup>

T <sub>A</sub>	PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC193QPWRQ1	HC193Q
-40°C to 85°C	TSSOP – PW	Reel of 2000	SN74HC193IPWRQ1	HC193I

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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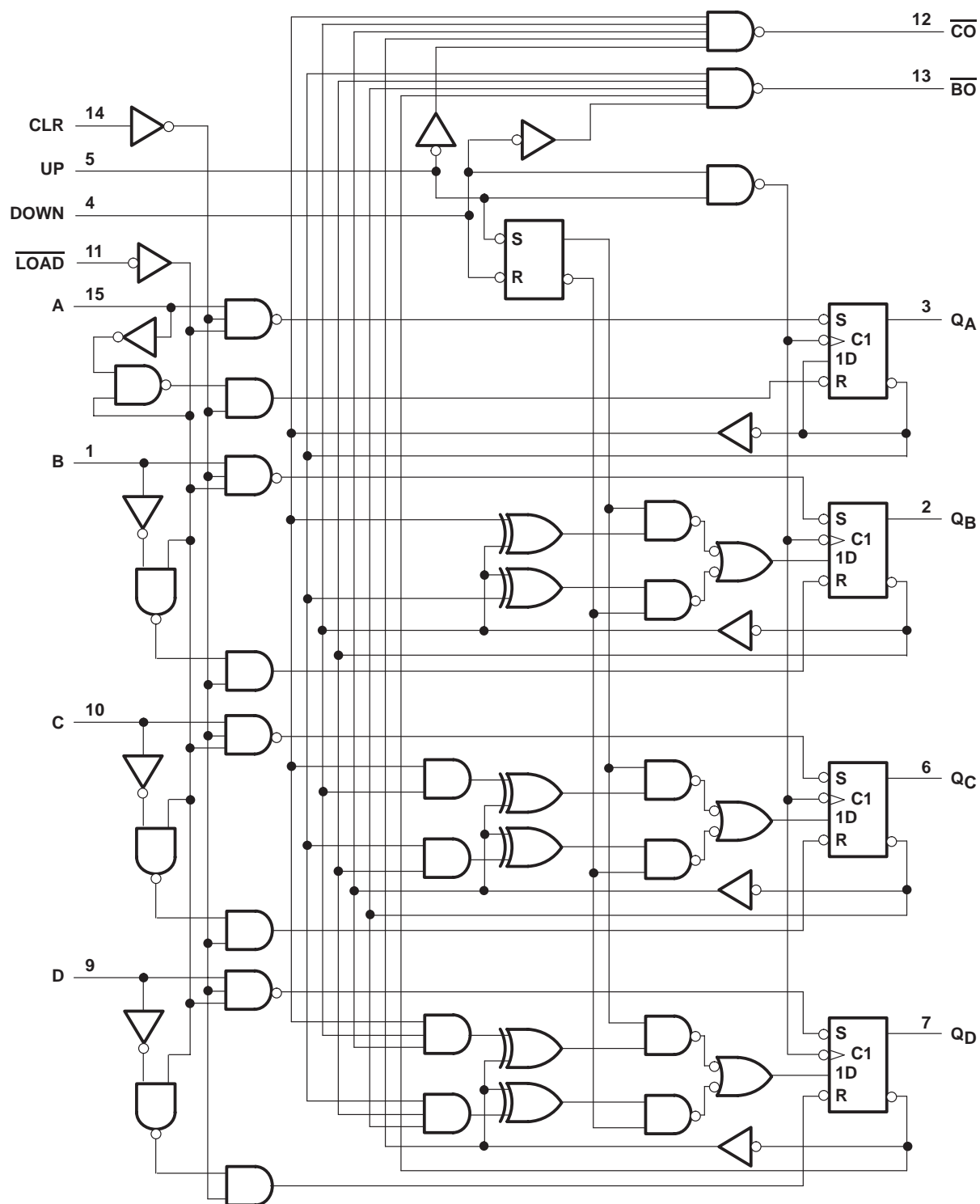
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# SN74HC193-Q1

## 4-BIT SYNCHRONOUS UP/DOWN COUNTER (DUAL CLOCK WITH CLEAR)

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logic diagram (positive logic)



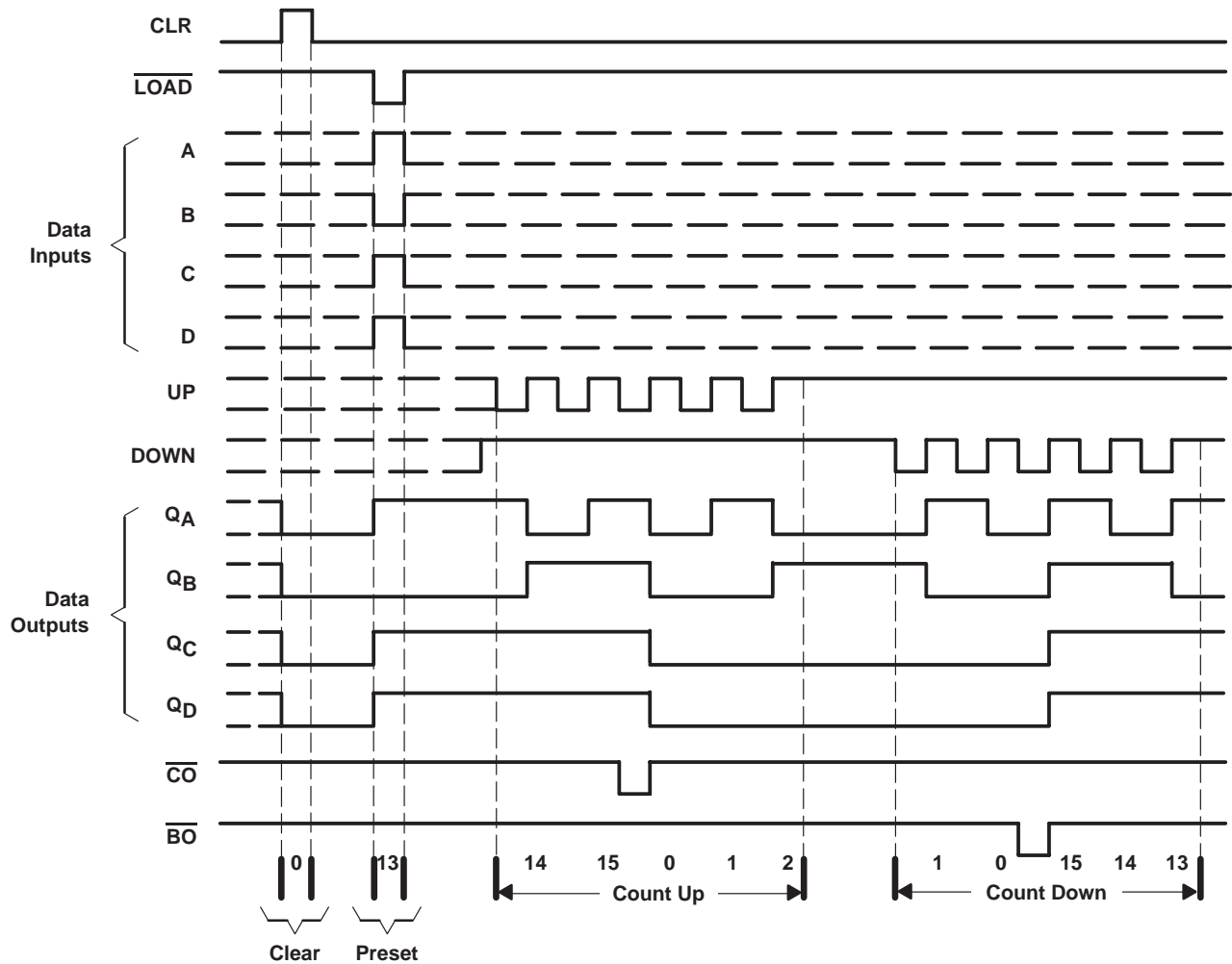
**SN74HC193-Q1**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTER**  
**(DUAL CLOCK WITH CLEAR)**

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**typical clear, load, and count sequence**

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides  $\overline{\text{LOAD}}$ , data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

# SN74HC193-Q1

## 4-BIT SYNCHRONOUS UP/DOWN COUNTER

### (DUAL CLOCK WITH CLEAR)

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$\Delta t/\Delta v^\ddagger$	Input transition rise/fall time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
$T_A$	Operating free-air temperature	Q-suffix devices	–40	125	°C
		I-suffix devices	–40	85	

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

<sup>‡</sup> If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



**SN74HC193-Q1**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTER**  
**(DUAL CLOCK WITH CLEAR)**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C TO 125°C		T <sub>A</sub> = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	µA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

# SN74HC193-Q1

## 4-BIT SYNCHRONOUS UP/DOWN COUNTER

### (DUAL CLOCK WITH CLEAR)

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = –40°C TO 125°C		T <sub>A</sub> = –40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		4.2		2.8		3.3	MHz
		4.5 V		21		14		17	
		6 V		24		16		19	
t <sub>w</sub>	CLR high	2 V	120		180		150		ns
		4.5 V	24		36		30		
		6 V	21		31		26		
	$\overline{\text{LOAD}}$ low	2 V	120		180		150		
		4.5 V	24		36		30		
		6 V	21		31		26		
	UP or DOWN, high or low	2 V	120		180		150		
		4.5 V	24		36		30		
		6 V	21		31		26		
t <sub>su</sub>	Data before $\overline{\text{LOAD}}$ inactive	2 V	110		165		140		ns
		4.5 V	22		33		28		
		6 V	19		28		24		
	CLR inactive before UP↑ or DOWN↓	2 V	110		165		140		
		4.5 V	22		33		28		
		6 V	19		28		24		
	$\overline{\text{LOAD}}$ inactive before UP↑ or DOWN↓	2 V	110		165		140		
		4.5 V	22		33		28		
		6 V	19		28		24		
t <sub>h</sub>	Data after $\overline{\text{LOAD}}$ inactive	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

**SN74HC193-Q1**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTER**  
**(DUAL CLOCK WITH CLEAR)**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
$t_{pd}$	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	DOWN	$\overline{BO}$	2 V		75	165		250		205	
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	UP or DOWN	Any Q	2 V		190	250		375		315	
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
$t_{PHL}$	CLR	Any Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
$t_t$		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	14		19		17	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	50	pF

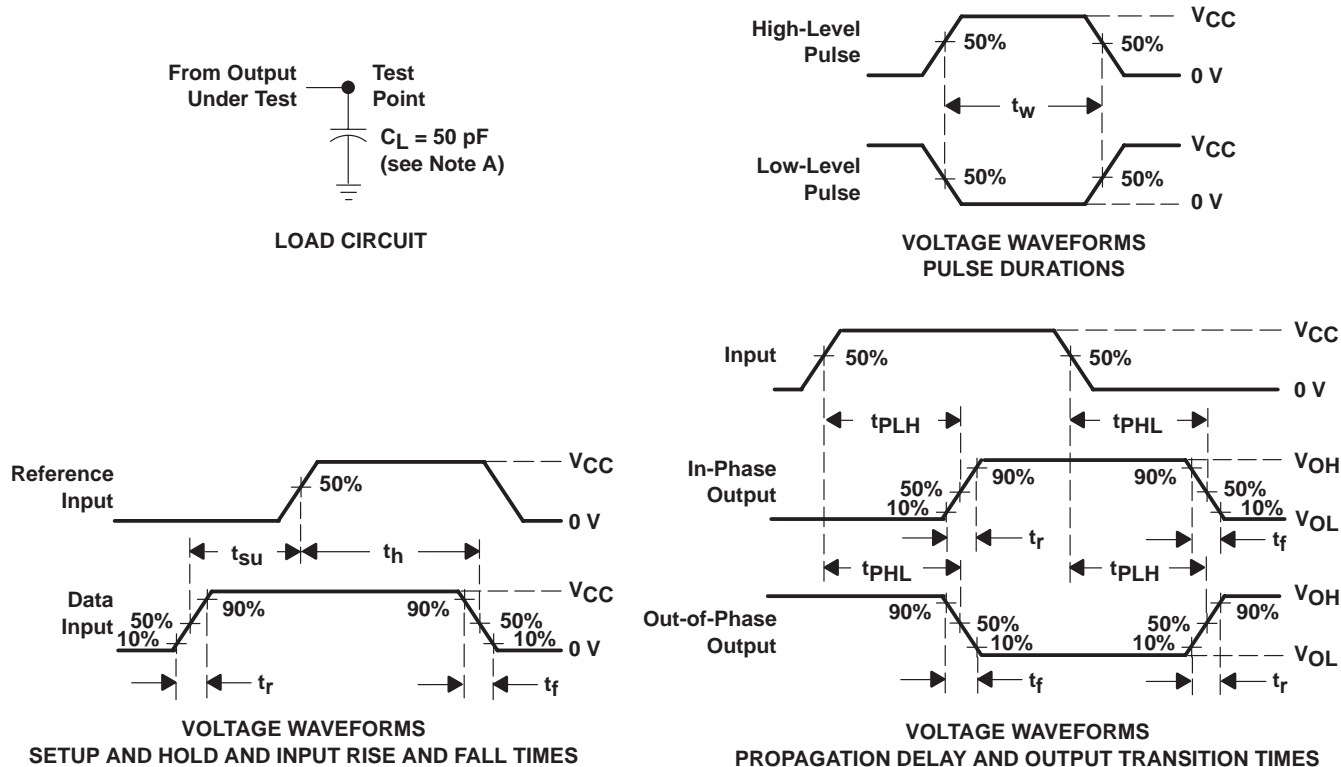
# SN74HC193-Q1

## 4-BIT SYNCHRONOUS UP/DOWN COUNTER

### (DUAL CLOCK WITH CLEAR)

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74HC193QPWRG4Q1</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC193Q
SN74HC193QPWRG4Q1.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC193Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN74HC193-Q1 :

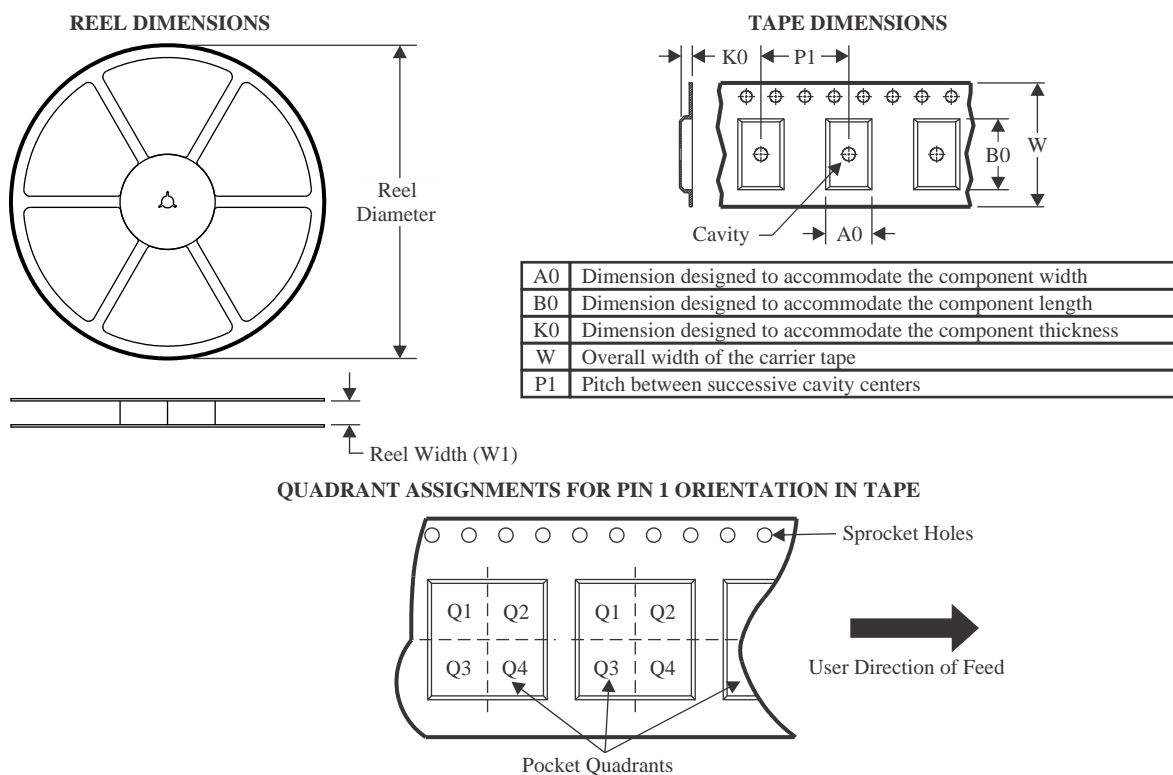
- Catalog : [SN74HC193](#)

- Military : [SN54HC193](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

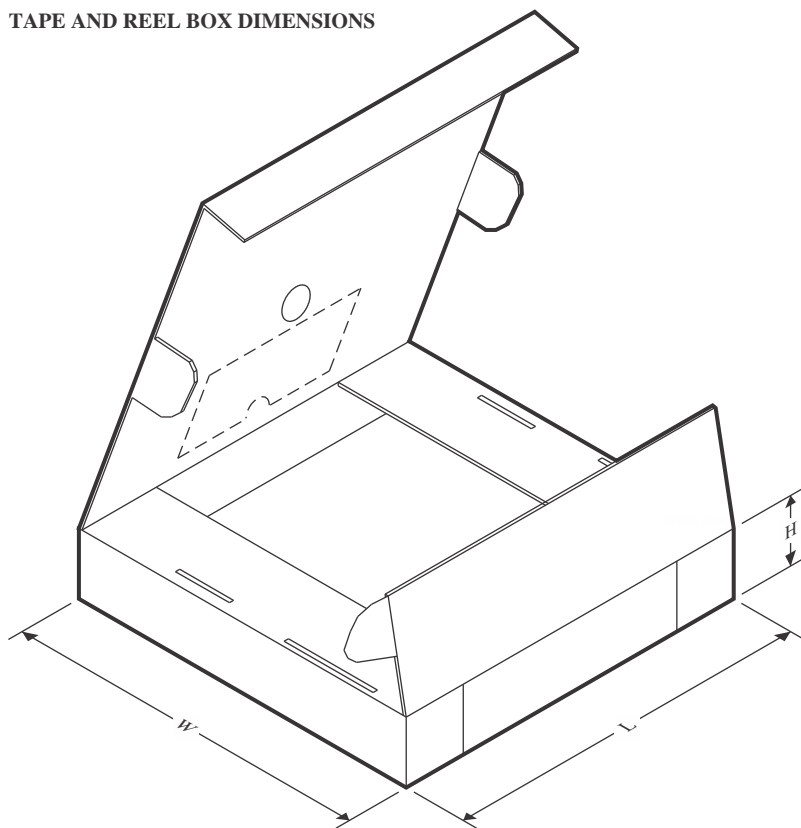
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

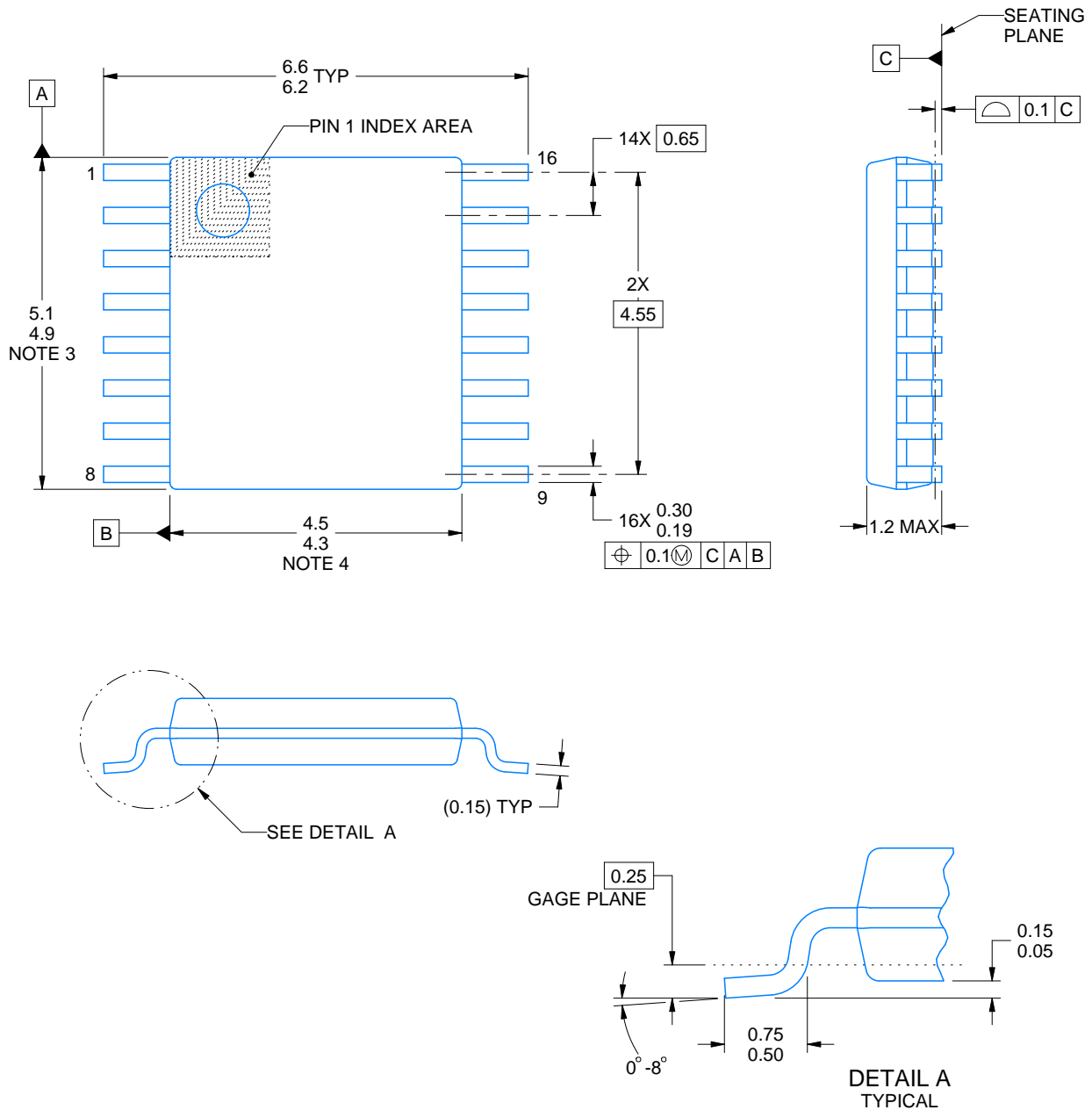
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC193QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC193QPWRG4Q1	TSSOP	PW	16	2000	356.0	356.0	35.0



4220204/A 02/2017

## NOTES:

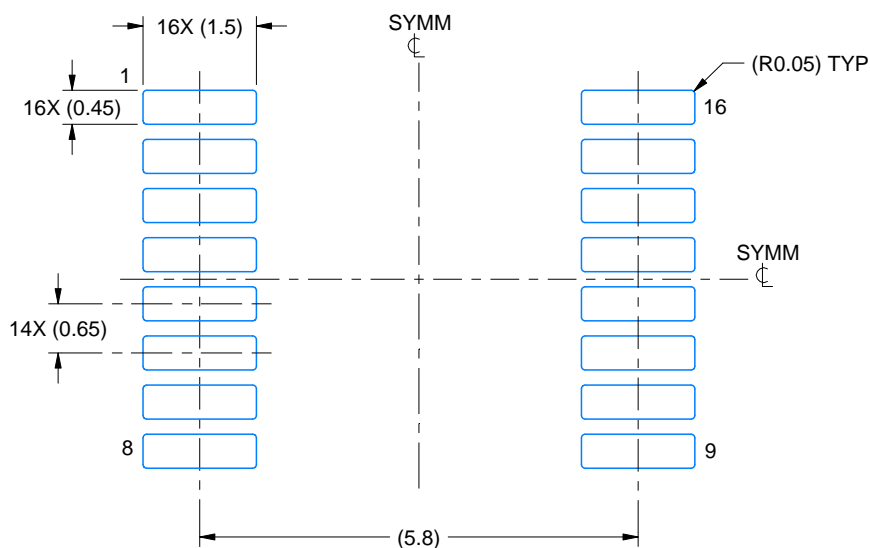
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

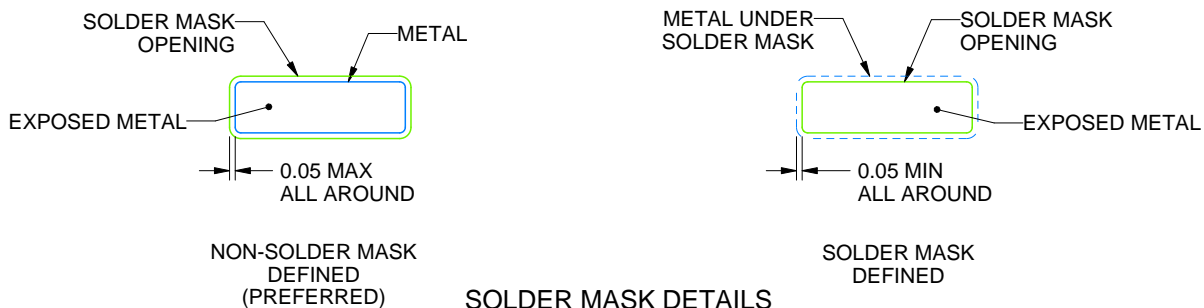
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

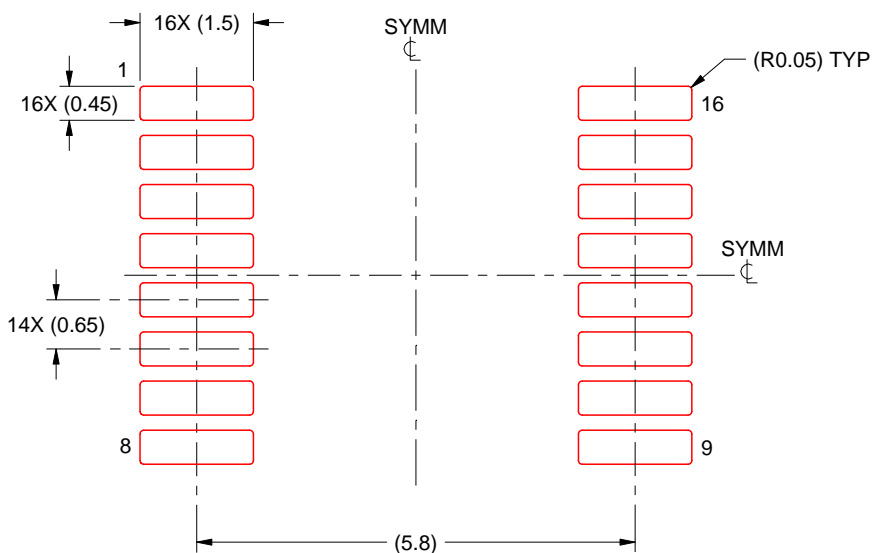
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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