

SN74HC139-Q1

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

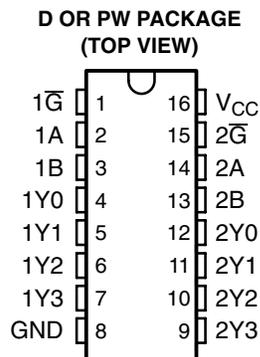
SCLS598B – NOVEMBER 2004 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Targeted Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to Ten LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- ESD Protection Level per AEC-Q100 Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

description/ordering information

The SN74HC139 device is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of this decoder and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The SN74HC139 device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable (\bar{G}) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.



ORDERING INFORMATION[†]

| T _A | PACKAGE [‡] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Reel of 2500 | SN74HC139QDRQ1 | HC139Q |
| | TSSOP – PW | Reel of 2000 | SN74HC139QPWRQ1 | HC139Q |

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|-----------|--------|---|---------|----|----|----|
| \bar{G} | SELECT | | Y0 | Y1 | Y2 | Y3 |
| | B | A | | | | |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |



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recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------------|-------------------------|-----------------|-----|------|
| V _{CC} | Supply voltage | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | V |
| | | V _{CC} = 4.5 V | 3.15 | | |
| | | V _{CC} = 6 V | 4.2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | 0.5 | | V |
| | | V _{CC} = 4.5 V | 1.35 | | |
| | | V _{CC} = 6 V | 1.8 | | |
| V _I | Input voltage | 0 | V _{CC} | | V |
| V _O | Output voltage | 0 | V _{CC} | | V |
| Δt/Δv | Input transition rise/fall time | V _{CC} = 2 V | 1000 | | ns |
| | | V _{CC} = 4.5 V | 500 | | |
| | | V _{CC} = 6 V | 400 | | |
| T _A | Operating free-air temperature | -40 | 125 | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | T _A = -40°C TO 125°C | | T _A = -40°C TO 85°C | | UNIT |
|-----------------|---|---------------------------|-----------------------|------|-------|---------------------------------|-------|--------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | 1.9 | 1.9 | | | V |
| | | | 4.5 V | 4.4 | 4.499 | 4.4 | 4.4 | | | |
| | | | 6 V | 5.9 | 5.999 | 5.9 | 5.9 | | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | 3.7 | 3.84 | | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | 5.2 | 5.34 | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | 0.1 | 0.1 | | V |
| | | | 4.5 V | | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | | 6 V | | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | 0.4 | 0.33 | | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | 0.4 | 0.33 | | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | ±1000 | ±1000 | | nA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | 160 | 80 | | μA | |
| C _i | | 2 V to 6 V | | 3 | 10 | 10 | 10 | | pF | |



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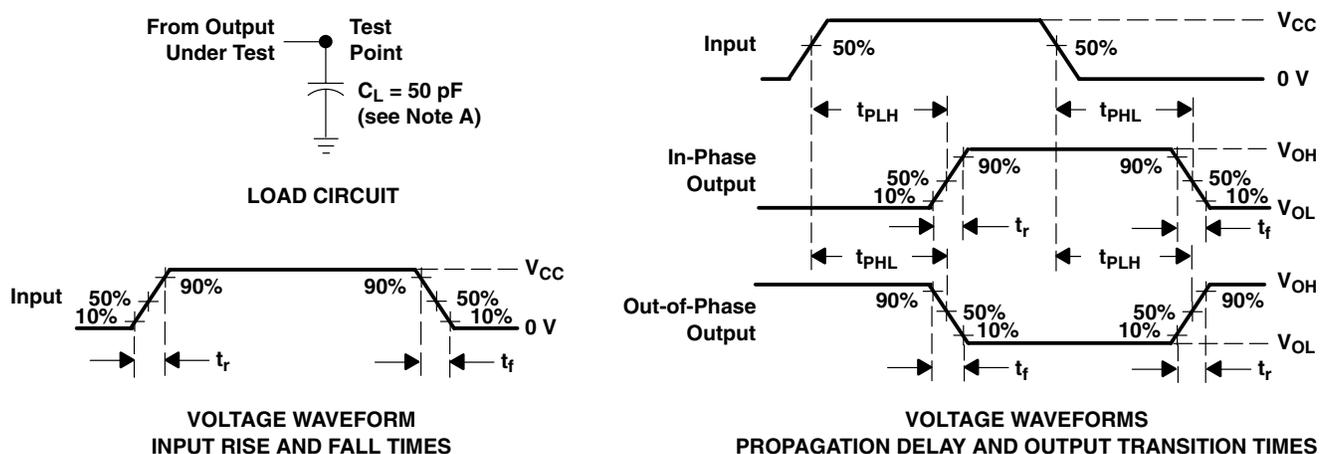
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C}$ TO 125°C | | $T_A = -40^\circ\text{C}$ TO 85°C | | UNIT |
|-----------|--------------|-------------|----------|--------------------------|-----|-----|---|-----|--|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | 2 V | | 47 | 175 | | 255 | | 220 | ns |
| | | | 4.5 V | | 14 | 35 | | 51 | | 44 | |
| | | | 6 V | | 12 | 30 | | 44 | | 38 | |
| | \bar{G} | Y | 2 V | | 39 | 175 | | 255 | | 220 | |
| | | | 4.5 V | | 11 | 35 | | 51 | | 44 | |
| | | | 6 V | | 10 | 30 | | 44 | | 38 | |
| t_t | | Y | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per decoder | No load | 25 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. The outputs are measured one at a time, with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74HC139QDRG4Q1 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QDRG4Q1.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QDRQ1 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QDRQ1.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QPWRG4Q1 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QPWRG4Q1.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC139Q |
| SN74HC139QPWRQ1 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HC139Q |
| SN74HC139QPWRQ1.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HC139Q |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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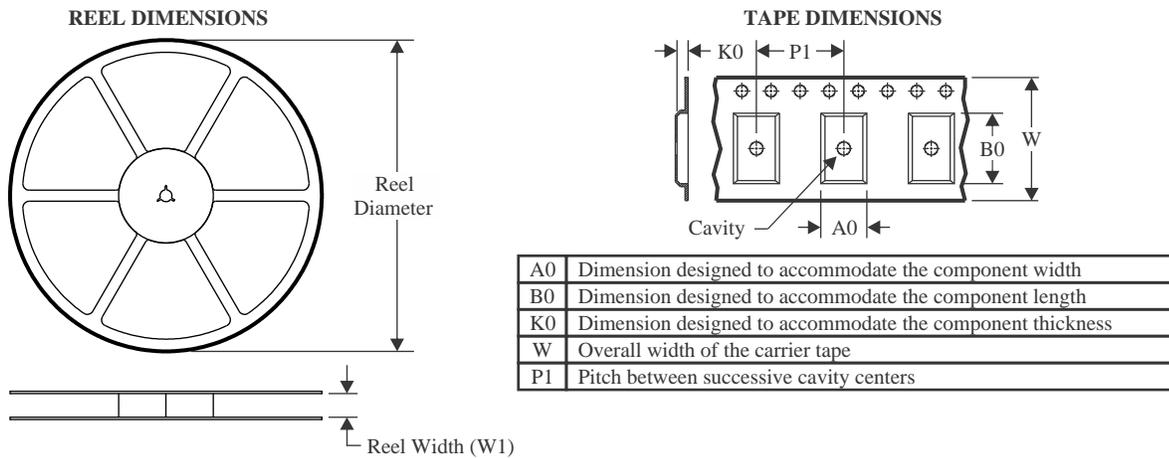
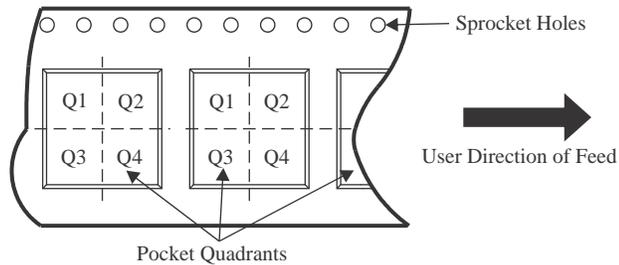
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OTHER QUALIFIED VERSIONS OF SN74HC139-Q1 :

- Catalog : [SN74HC139](#)
- Military : [SN54HC139](#)

NOTE: Qualified Version Definitions:

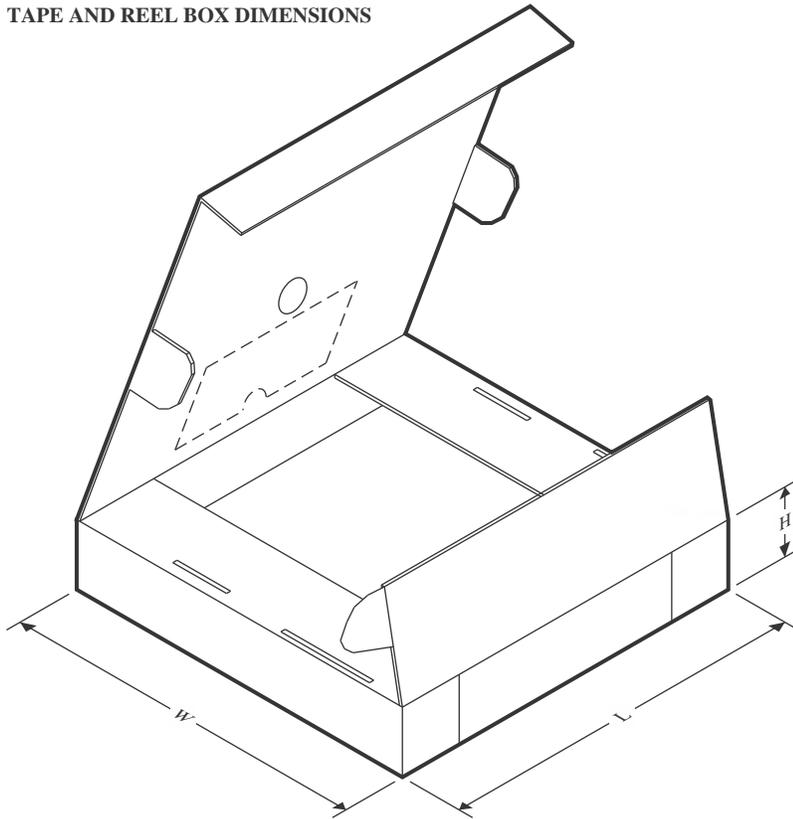
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

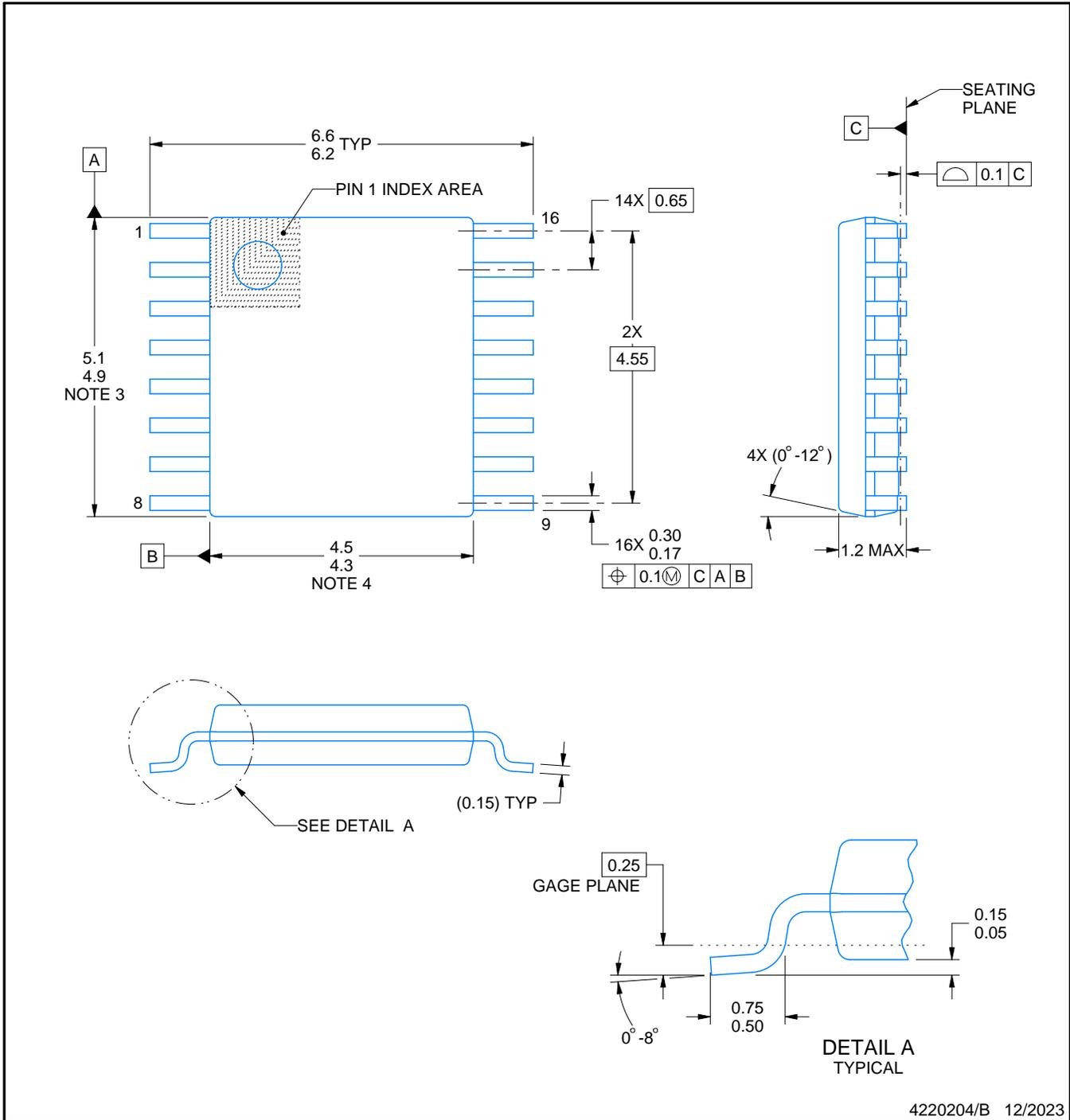
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC139QDRQ1 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC139QPWRG4Q1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC139QPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC139QDRQ1 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC139QPWRG4Q1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC139QPWRQ1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |



NOTES:

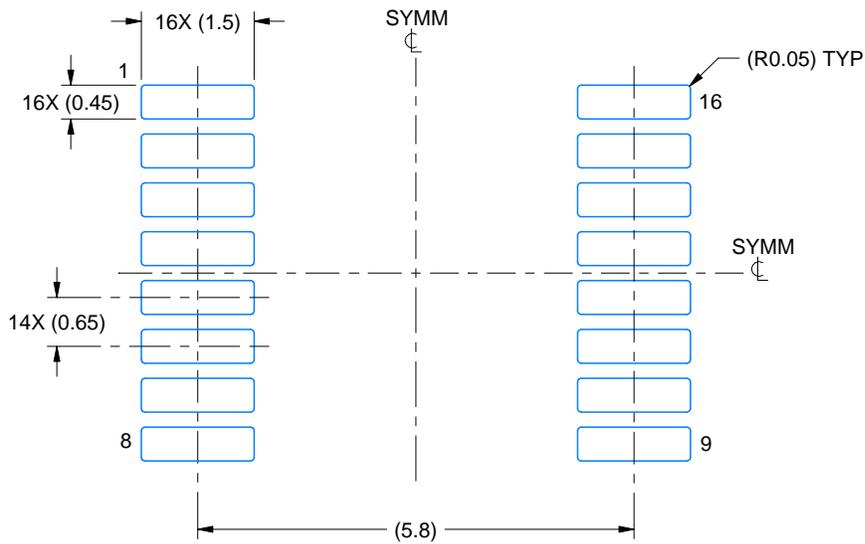
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

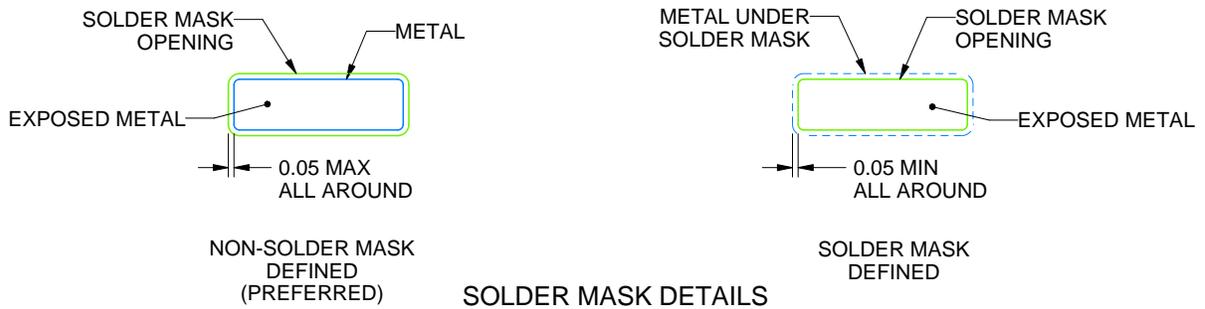
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

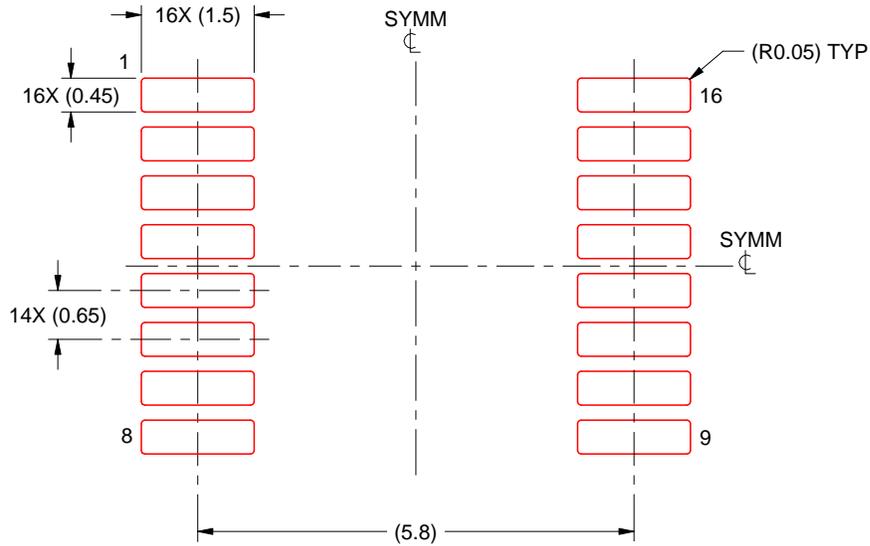
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

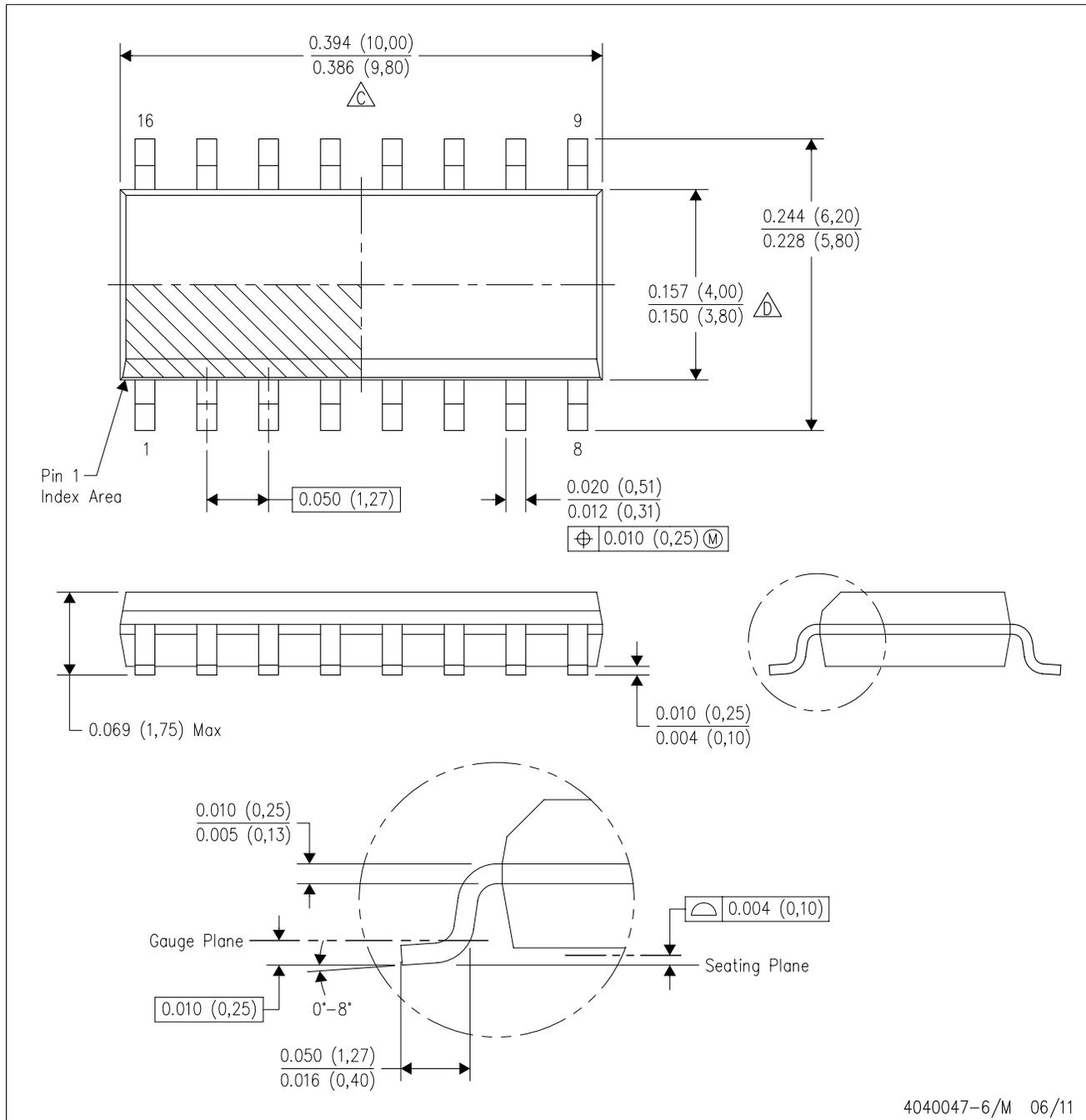
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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