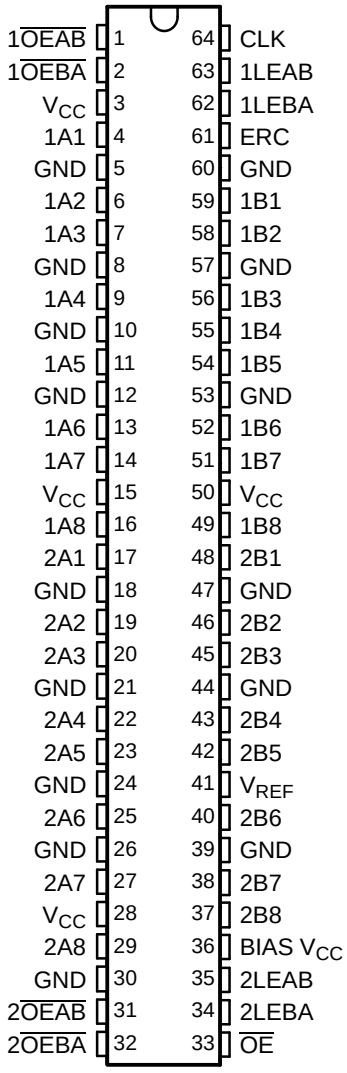
SN74GTLPH1655
16-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE UNIVERSAL BUS TRANSCEIVER

SCES294C – OCTOBER 1999 – REVISED MAY 2005

FEATURES

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Partitioned as Two 8-Bit Transceivers With Individual Latch Timing and Output Control, but With a Common Clock**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION

The SN74GTLPH1655 is a high-drive, 16-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers and allows for transparent, latched, and clocked modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

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DESCRIPTION (CONTINUED)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1655 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1655DGGR	GTLPH1655

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLPH1655 is a high-drive (100 mA), 16-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or clocked modes. The device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output signals and a common clock for both transceiver words. It can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1655 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541
Latched transceiver	'543			'16543
Latch	'373, '573	'843	'841	'16373
Registered transceiver	'646, '652			'16646, '16652
Flip-flop	'374, '574		'821	'16374
SN74GTLPH1655 UBT transceiver replaces all above functions				

FUNCTIONAL DESCRIPTION (CONTINUED)

Data flow for each word is determined by the respective latch enables (xLEAB and xLEBA), output enables (x$\overline{\text{OEAB}}$ and x$\overline{\text{OEBA}}$), and clock (CLK). The output enables (1$\overline{\text{OEAB}}$, 1$\overline{\text{OEBA}}$, 2$\overline{\text{OEAB}}$, and 2$\overline{\text{OEBA}}$) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively. Note that CLK is common to both directions and both 8-bit words. $\overline{\text{OE}}$ also is common and disables all I/O ports simultaneously.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When $\overline{\text{OEAB}}$ is low, the outputs are active. With $\overline{\text{OEAB}}$ high, the outputs are in the high-impedance state.

The data flow for the B-to-A direction is identical, except $\overline{\text{OEBA}}$, LEBA, and CLK are used.

FUNCTION TABLES

FUNCTION(1)

INPUTS				OUTPUT B	MODE
$\overline{\text{OEAB}}$	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	L	H	X	B_0(2)	Latched storage of A data
L	L	L	X	B_0(3)	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

(1) A-to-B data flow is shown. B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and CLK. The condition when $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ are both low at the same time is not recommended.
(2) Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

OUTPUT ENABLE

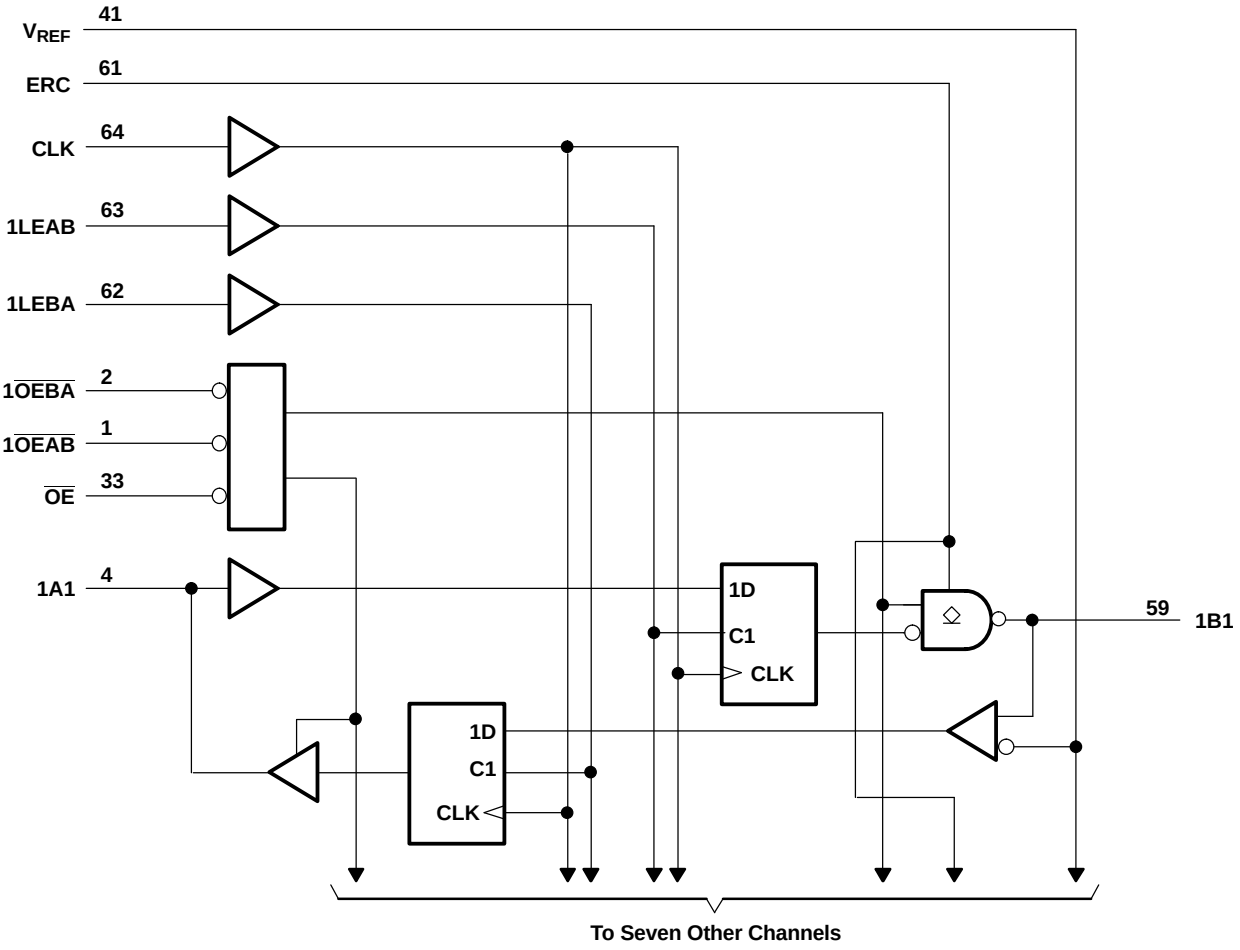
INPUTS			OUTPUTS	
$\overline{\text{OE}}$	$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	A PORT	B PORT
L	L	L	Active	Active(1)
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

(1) This condition is not recommended.

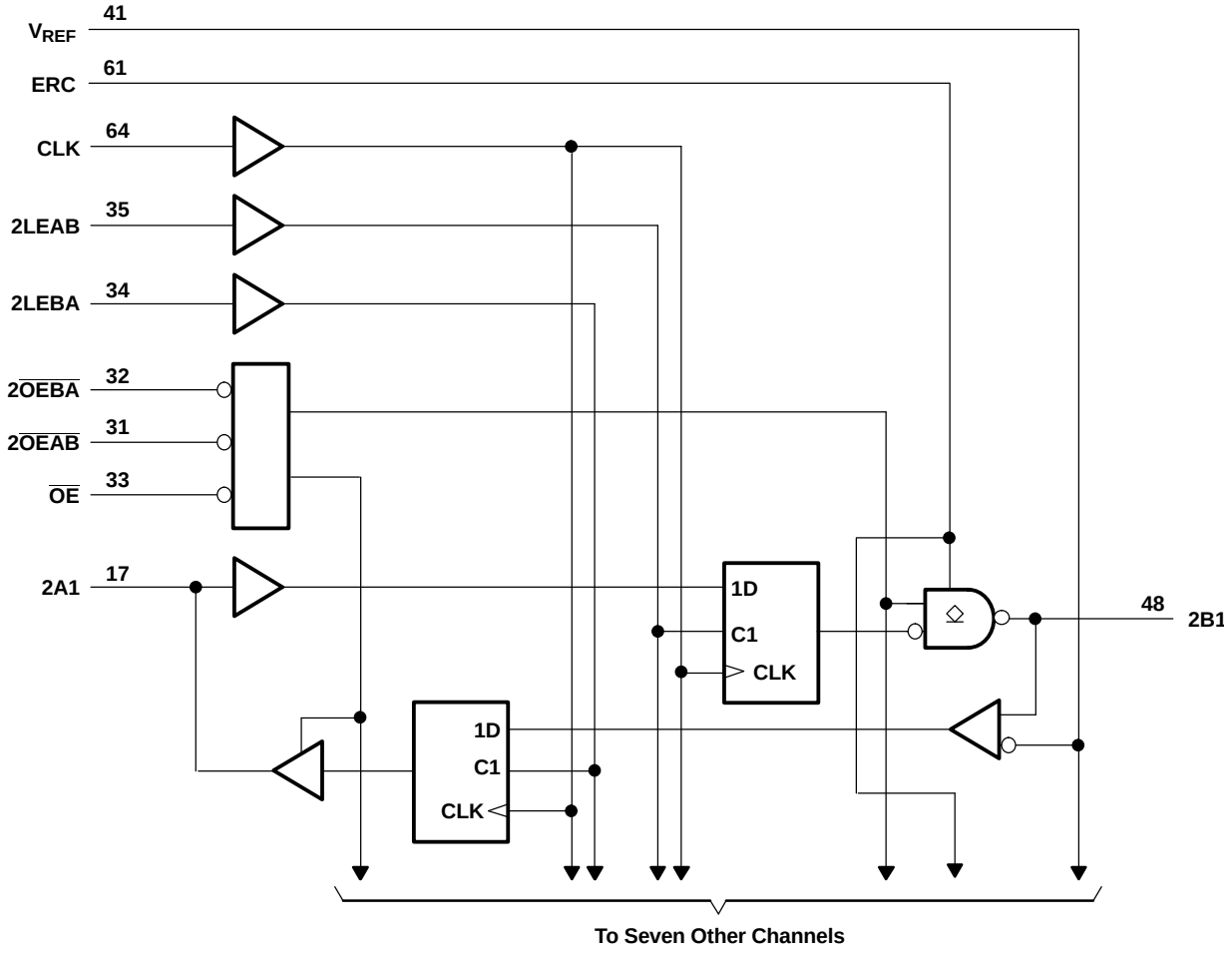
B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC DIAGRAM (POSITIVE LOGIC) (CONTINUED)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	A port, $\overline{ERC}$, and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		200	
I_O	Current into any A-port output in the high state(3)			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[(1)(2)(3)(4)]

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 0.05			V
		ERC	V_{CC} – 0.6	V_{CC}	5.5	
		Except B port and ERC	2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 0.05	V
		ERC		GND	0.6	
		Except B port and ERC			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}(2)	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}(2)	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}(3)	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}(4)	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}(5)	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}(6)	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}(7)		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4.5	6.5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	7.5	pF
	B port	V_O = 1.5 V or 0			8.5	10.5	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

Live-Insertion Specifications for B Port

over operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	μA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		μA

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	3		ns
		CLK high or low	3		
t_{su}	Setup time	A before CLK	3		ns
		B before CLK	3		
		A before LEAB↓, CLK = don't care	2.5		
		B before LEBA↓, CLK = don't care	2.5		
t_h	Hold time	A after CLK	0.5		ns
		B after CLK	0.5		
		A after LEAB↓, CLK = don't care	0.5		
		B after LEBA↓, CLK = don't care	0.5		

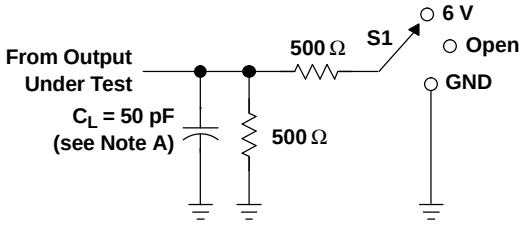
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

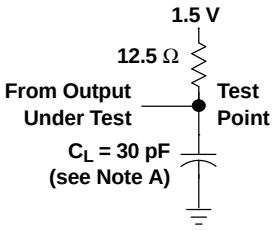
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	MIN	TYP(2)	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	A	B	Slow	3.5		7.7	ns
t_{PHL}				2.4		6.3	
t_{PLH}	A	B	Fast	2		6.3	ns
t_{PHL}				2		5.9	
t_{PLH}	LEAB	B	Slow	3.5		7.8	ns
t_{PHL}				2.7		6.4	
t_{PLH}	LEAB	B	Fast	2		6.4	ns
t_{PHL}				2		6	
t_{PLH}	CLK	B	Slow	4.7		8	ns
t_{PHL}				2.7		6.4	
t_{PLH}	CLK	B	Fast	3.6		6.8	ns
t_{PHL}				2		6.1	
t_{en}	$\overline{OE}$	B	Slow	3.5		7.3	ns
t_{dis}				3.5		7	
t_{en}	$\overline{OE}$	B	Fast	2		6	ns
t_{dis}				2		6.6	
t_{en}	$\overline{OEAB}$	B	Slow	3.5		7.4	ns
t_{dis}				3.5		7	
t_{en}	$\overline{OEAB}$	B	Fast	2		6.1	ns
t_{dis}				2		6.3	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.6		ns
			Fast		1.5		
t_f	Fall time, B outputs (80% to 20%)		Slow		3		ns
			Fast		2.2		
t_{PLH}	B	A		1.5		5.5	ns
t_{PHL}				1.5		5.5	
t_{PLH}	LEBA	A		1.3		5.2	ns
t_{PHL}				1		5	
t_{PLH}	CLK	A		1.2		6.3	ns
t_{PHL}				1		5	
t_{en}	$\overline{OE}$	A		1.5		5.6	ns
t_{dis}				1.5		6.1	
t_{en}	$\overline{OEBA}$	A		1.2		5.4	ns
t_{dis}				2		6.1	

(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

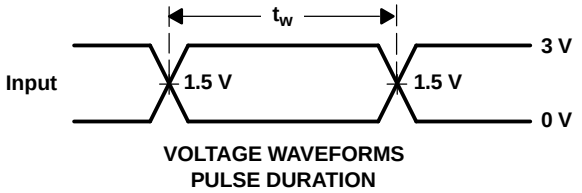


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

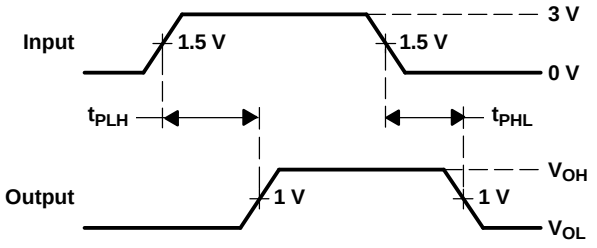


LOAD CIRCUIT FOR A OUTPUTS

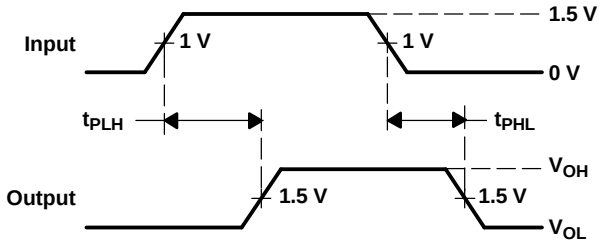
LOAD CIRCUIT FOR B OUTPUTS



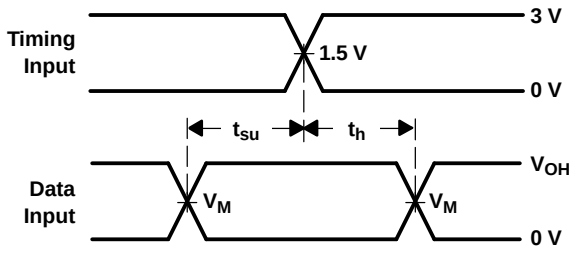
VOLTAGE WAVEFORMS
PULSE DURATION



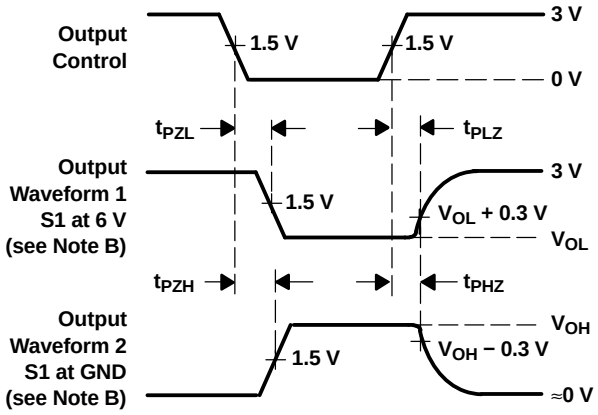
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

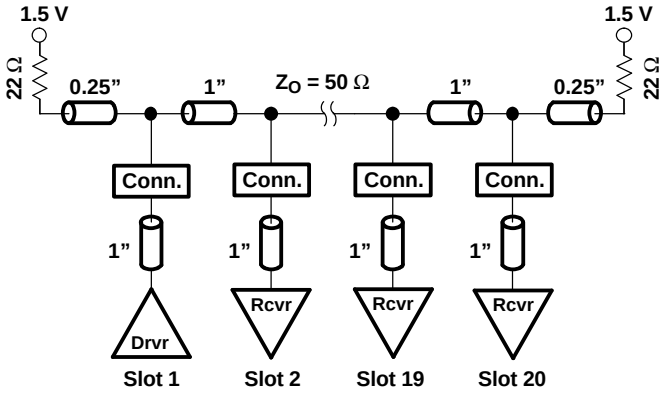


Figure 2. High-Drive Test Backplane

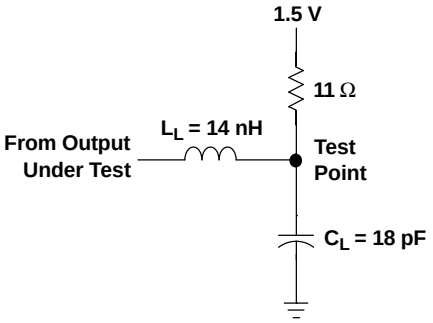


Figure 3. High-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	TYP(2)	UNIT
t_{PLH}	A	B	Slow	5	ns
t_{PHL}				5	
t_{PLH}	A	B	Fast	3.8	ns
t_{PHL}				3.8	
t_{PLH}	LEAB	B	Slow	4.9	ns
t_{PHL}				4.9	
t_{PLH}	LEAB	B	Fast	3.9	ns
t_{PHL}				3.9	
t_{PLH}	CLK	B	Slow	4.8	ns
t_{PHL}				4.8	
t_{PLH}	CLK	B	Fast	3.7	ns
t_{PHL}				3.7	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$	B	Slow	4.9	ns
t_{dis}				4.7	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$	B	Fast	3.5	ns
t_{dis}				4.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTLPH1655DGGR	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH1655
SN74GTLPH1655DGGR.B	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH1655

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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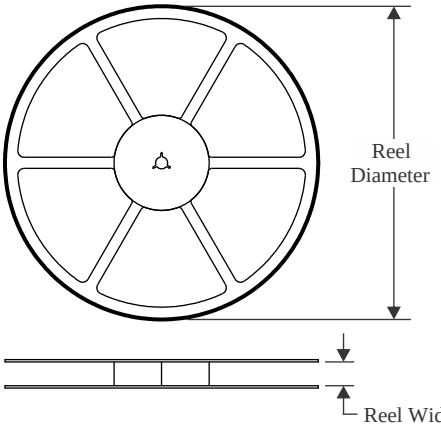
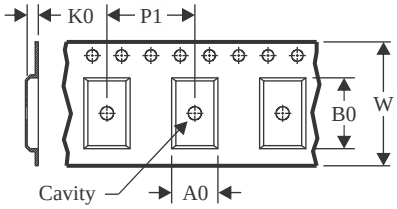
TAPE AND REEL INFORMATION

REEL DIMENSIONS

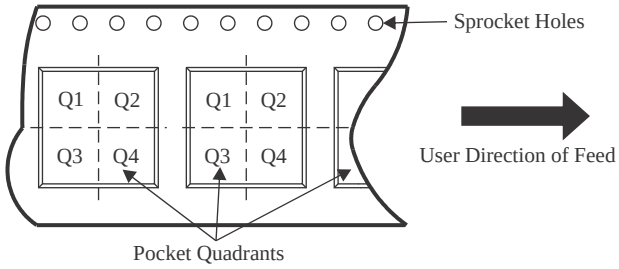


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

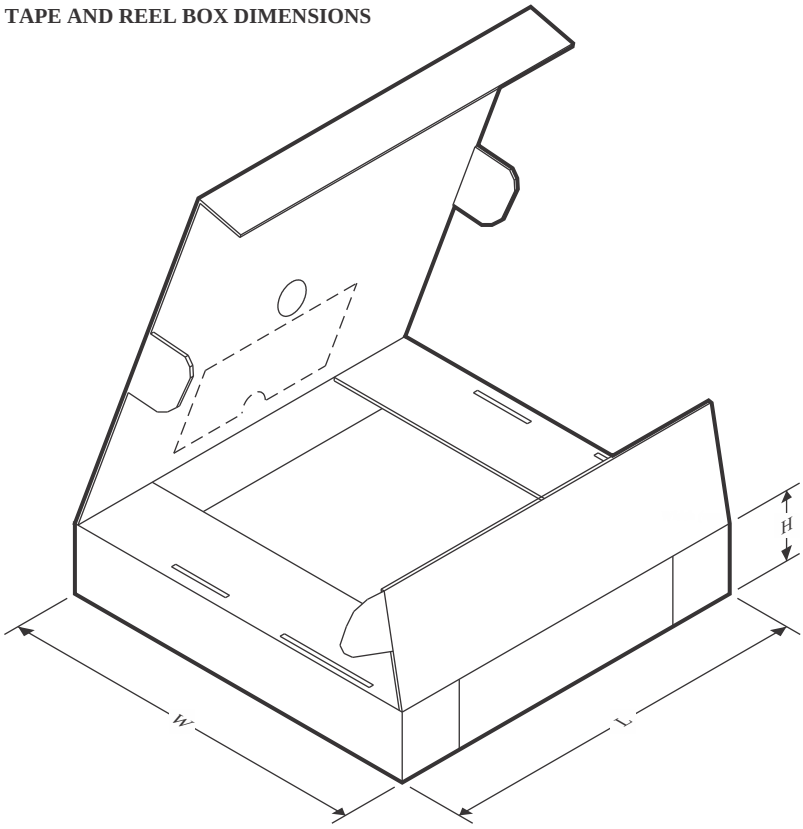
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH1655DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

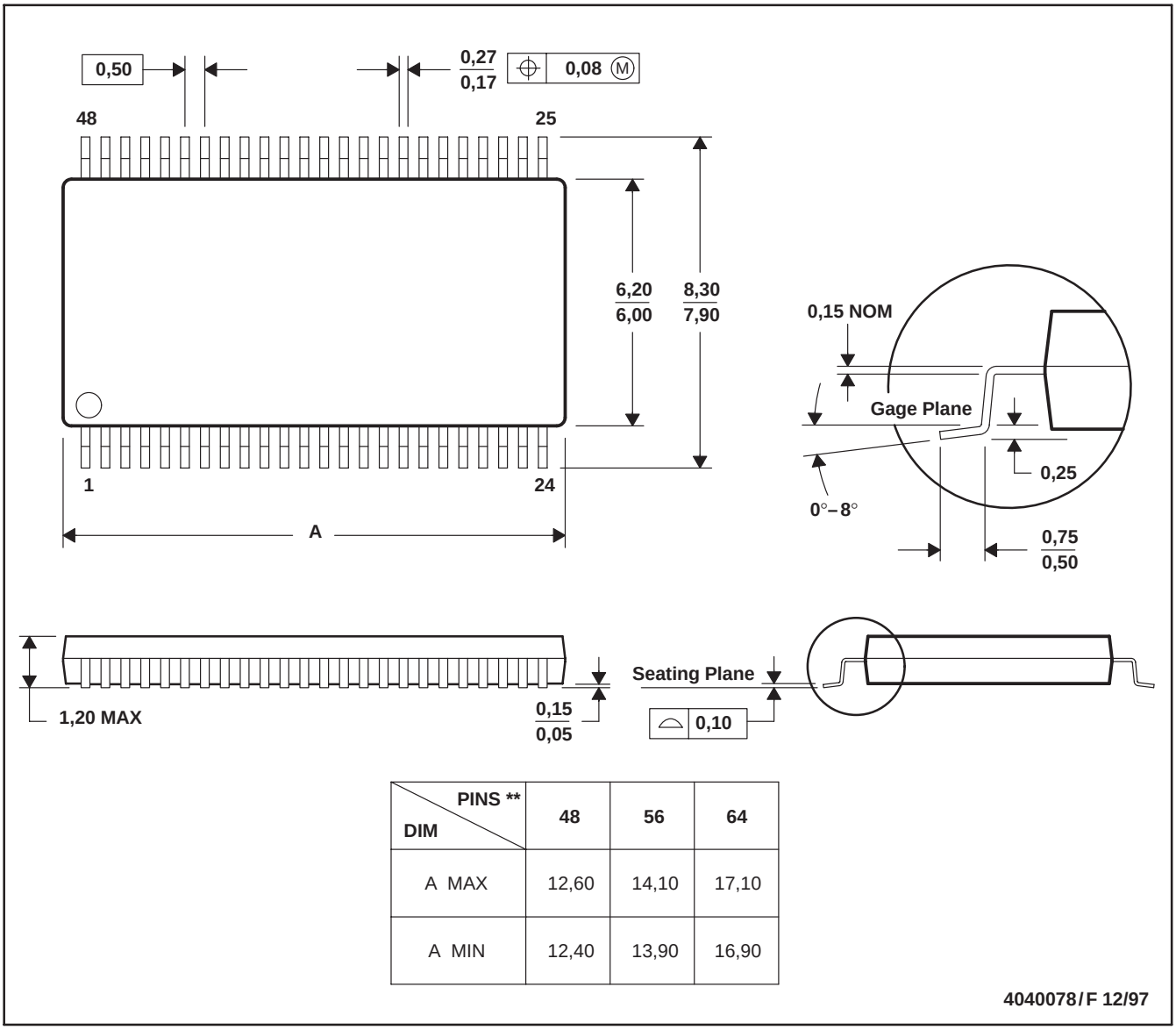


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH1655DGGR	TSSOP	DGG	64	2000	356.0	356.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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