



SN74GTL2014 4 通道 LVTTTL 至 GTL 收发器

1 特性

- 可用作 GTL–/GTL/GTL+ 至 LVTTTL 转换器或 LVTTTL 至 GTL–/GTL/GTL+ 转换器
- LVTTTL 输入最高可承受 5.5V 电压，允许直接访问 TTL 或 5V CMOS
- GTL 输入/输出工作电压高达 3.6V，这使得器件可在高压开漏应用中使用
- VREF 可降至 0.5V，以实现低电压 CPU 使用率
- 支持局部断电
- 锁断保护超过 500mA，符合 JESD78 规范的要求
- 封装选项：TSSOP14
- -40°C 至 +85°C 工作温度范围
- 所有端子上具备静电放电 (ESD) 保护
 - 2000V 人体模型 (HBM)，JESD22-A114
 - 1000V 充电器件模型 (CDM)，IEC61000-4-2

2 应用

- 服务器
- 基站
- 有线通信

3 说明

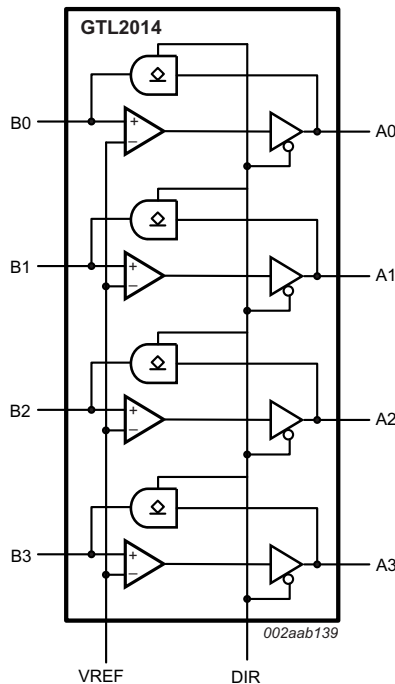
SN74GTL2014 是一款 4 通道转换器，用于连接 3.3V LVTTTL 芯片组 I/O 与 Xeon 处理器 GTL–/GTL/GTL+ I/O。

SN74GTL2014 在所有端子上集成了 ESD 保护单元，并且采用 TSSOP 封装 (5.0mm × 4.4mm)。器件在自然通风环境下的额定工作温度范围为 -40°C 至 85°C。

器件信息⁽¹⁾

部件号	封装	封装尺寸 (标称值)
SN74GTL2014	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



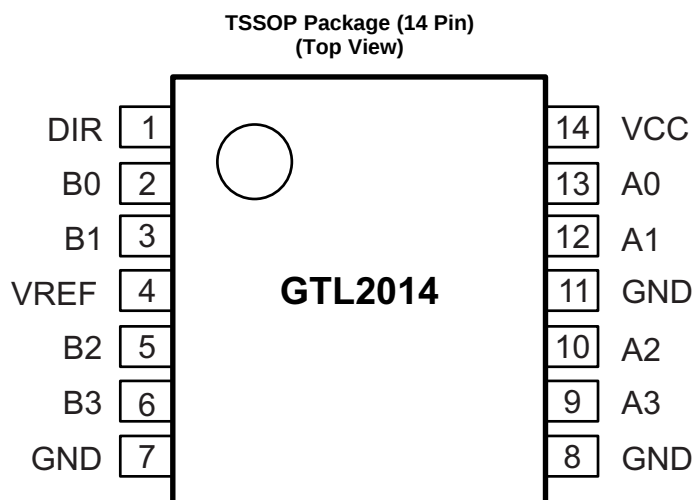
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4 修订历史记录

Changes from Original (February 2014) to Revision A	Page
• 已添加 添加了处理额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。	1
• Updated Specifications section	4
• Updated LVTTTL/TTL to GTL–/GTL/GTL+ application schematic.	9
• Updated LVTTTL/TTL to GTL–/GTL/GTL+ application schematic.	11
• Added <i>Power Supply Recommendations</i>	12

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
A0	13	LVTTTL data input/output
A01	12	
A02	10	
A03	9	
B0	2	GTL data input/output
B01	3	
B02	5	
B03	6	
DIR	1	Direction control input (LVTTTL)
GND	7	Ground
	8	
	11	
VCC	14	Supply voltage
VREF	4	GTL reference voltage

6 Specifications

6.1 Absolute Maximum Ratings

 Specified at $T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	4.6	V
I _{IK}	Input clamping current, V _I < 0 V			−50	mA
V _{SEL}	Input control voltages SEL ⁽²⁾⁽³⁾		−0.5	6	V
V _I	Input voltage	A port	−0.5	7	V
		B port	−0.5	4.6	
I _{OK}	Control input clamp current, V _O < 0 V			−50	mA
V _O	Output voltage	A port	−0.5	7	V
		B port	−0.5	4.6	
I _{OL}	Current into any output in the low state	A port		40	mA
		B port		80	
I _{OH}	Current into any output in the high state			−40	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-55	150	$^{\circ}\text{C}$
$V_{ESD}^{(1)}$	Human Body Model (HBM), JEDEC: JESD22-A114 ⁽²⁾	All pins	0	2	kV
	IEC61000-4-2 contact discharge ⁽³⁾	All pins	0	1	

- (1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. *Pins listed as 250 V may actually have higher performance.*
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. *Pins listed as 250 V may actually have higher performance.*

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3	3.3	3.6	V
V _{TT}	Termination voltage	GTL−	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	
		GTL+	1.35	1.5	1.65	
V _{REF}	Reference voltage	Overall	0.5	2 / 3 V _{TT}	V _{CC} / 2	V
		GTL−	0.5	0.6	0.63	
		GTL	0.76	0.8	0.84	
		GTL+	0.87	1	1.1	
V _I	Input voltage	A port	0	3.3	5.5 ⁽²⁾	V
		B port	0	V _{TT}	3.6	
V _{IH}	High-level input voltage	A port and DIR	2			V
		B port	V _{REF} + 50 mV			

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) The $V_{I(max)}$ of LVTTTL port is 3.6 V if configured as output (DIR=L).

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{IL}	Low-level input voltage	A port and DIR			0.8	V
		B port		V _{REF} – 50 mV		
I _{OH}	High-level input current	A port			–20	mA
I _{OL}	Low-level output current	A port			20	mA
		B port			50	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74GTL2014	UNIT
		PW	
		14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	136.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	63.0	
R _{θJB}	Junction-to-board thermal resistance	78.6	
Ψ _{JT}	Junction-to-top characterization parameter	11.9	
Ψ _{JB}	Junction-to-board characterization parameter	77.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Specified at T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	–40°C TO 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	A port	V _{CC} = 3 to 3.6 V, I _{OH} = –100 μA	V _{CC} – 0.2			V
		V _{CC} = 3 V, I _{OH} = –16 mA	2			
V _{OL}	A port	V _{CC} = 3 V, I _{OL} = 8 mA	0.28 0.4			V
	A port	V _{CC} = 3 V, I _{OL} = 16 mA	0.55 0.8			
	B port	V _{CC} = 3 V, I _{OL} = 40 mA	0.23 0.4			
I _I	A port	V _{CC} = 3.6 V, V _I = V _{CC}	±1			μA
		V _{CC} = 3.6, V _I = 0 V	±1			
		V _{CC} = 3.6, V _I = 5.5 V	5			
	B port	V _{CC} = 3.6 V, V _I = V _{TT} or GND	±1			μA
	Control pin	V _{CC} = 3.6 V, V _I = V _{CC} or 0 V	±1			μA
I _{off}	OFF-state output current on A port	V _{CC} = 0 V, V _{IO} = 0 to 3.6 V	±10			μA
	OFF-state output current on A port	V _{CC} = 0 V, V _{IO} 3.6 to 5.5V	±100			
	OFF-state output current on B port	V _{CC} = 0 V, V _{IO} = 0 to 3.6 V	±10			
I _{CC}	A port	V _{CC} = 3.6 V, V _I = V _{CC} or GND, I _O = 0	3 10			mA
	B port	V _{CC} = 3.6 V, V _I = V _{TT} or GND, I _O = 0	3 10			mA
ΔI _{CC}	A port or control input	V _{CC} = 3.6 V, V _I = V _{CC} – 0.6 V	500			μA
C _I	Input capacitance of control pin	V _I = 3.0 V or 0 V	2 2.5			pF
C _{IO}	A port	V _O = 3 V or 0	4 6			pF
	B port	V _O = V _{TT} or 0	5.46 5.55			

6.6 Dynamic Electrical Characteristics

over operating range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 1.65$ to 4.6 V, $GND = 0$ V for GTL (see [Functional Block Diagram](#))

PARAMETER		GTL–			GTL			GTL+			UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{REF} = 0.6\text{ V}$ $V_{TT} = 0.9\text{ V}$			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{REF} = 0.8\text{ V}$ $V_{TT} = 1.2\text{ V}$			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{REF} = 1\text{ V}$ $V_{TT} = 1.5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} (low to high propagation delay)	An to Bn		2.8	5		2.8	5		2.8	5	ns
t _{PHL} (high to low propagation delay)			3.3	7		3.4	7		3.4	7	
t _{PLH} (low to high propagation delay)	Bn to An		5.3	8		5.2	8		5.1	8	ns
t _{PHL} (high to low propagation delay)			5.2	8		4.9	7.16		4.7	7.16	

6.7 Typical Characteristics

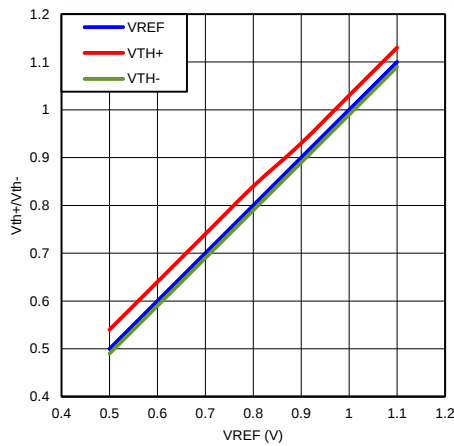


Figure 1. GTL Vth+ and Vth– vs VREF (25°C)

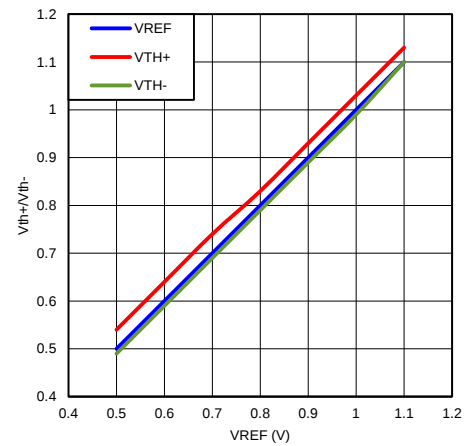


Figure 2. GTL Vth+ and Vth– vs VREF (–40°C)

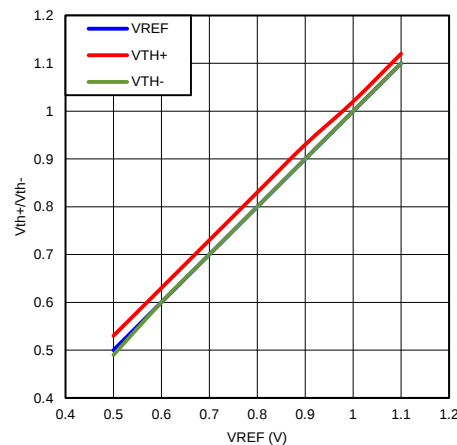
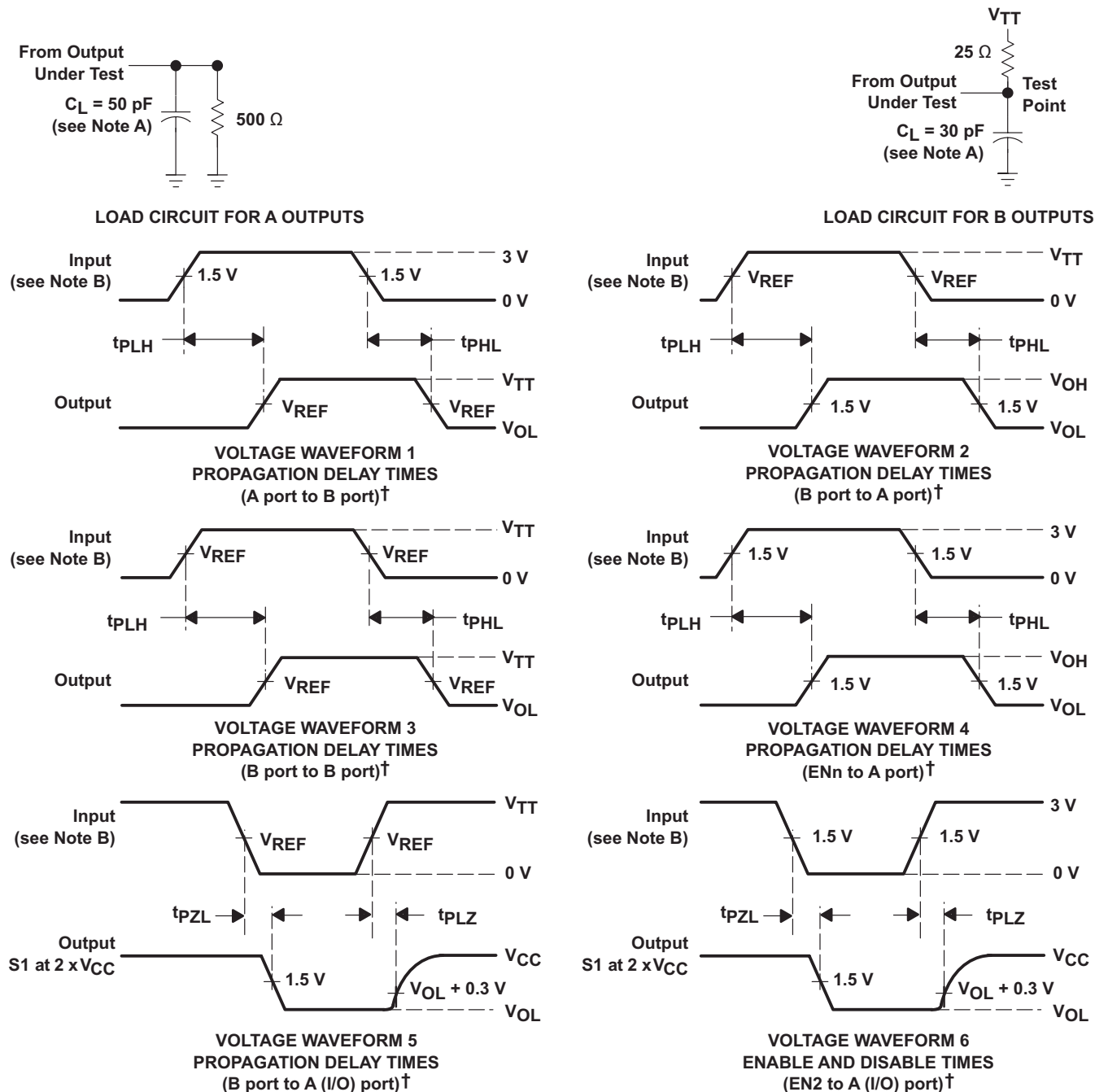


Figure 3. GTL Vth+ and Vth– vs VREF (125°C)

7 Parameter Measurement Information

$V_{TT} = 1.2\text{ V}$, $V_{REF} = 0.8\text{ V}$ for GTL and $V_{TT} = 1.5\text{ V}$, $V_{REF} = 1\text{ V}$ FOR GTL+



[†] All control inputs are LVTTTL levels.

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 4. Load Circuits and Voltage Waveforms

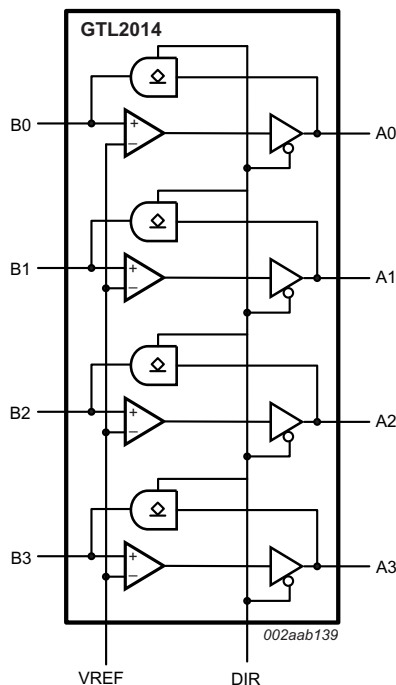
8 Detailed Description

8.1 Overview

The GTL2014 is a 4-channel translating transceiver designed for 3.3-V LVTTTL system interface with a GTL–/GTL/GTL+ bus, where GTL–/GTL/GTL+ refers to the reference voltage of the GTL bus and the input/output voltage thresholds associated with it.

The direction pin allows the part to function as either a GTL-to-LVTTTL sampling receiver or as a LVTTTL-to-GTL interface.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 5 V tolerance on LVTTTL input

The GTL2014 LVTTTL inputs (only) are tolerant up to 5.5 V and allows direct access to TTL or 5 V CMOS inputs. The LVTTTL outputs are not 5.5 V tolerant.

8.3.2 3.6 V tolerance on GTL Input/Output

The GTL2014 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

8.3.3 Ultra-Low VREF and High Bandwidth

GTL2014's VREF tracks down to 0.5 V for low voltage CPUs with excellent propagation delay performance. This feature allows the GTL2014 to support high data rates with the GTL– bus.

8.4 Device Functional Modes

The GTL2014 performs translation in two directions. One direction is GTL–/GTL/GTL+ to LVTTTL when DIR is tied to GND. With appropriate VREF set up, the GTL input can be compliant with GTL–/GTL/GTL+. Another direction is LVTTTL to GTL–/GTL/GTL+ when DIR is tied to VCC. 3.6 V tolerance on the GTL output allows the GTL outputs to pull up to any voltage level under 3.6 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

GTL2014 is the voltage translator for GTL–/GTL/GTL+ to LVTTTL or LVTTTL to GTL–/GTL/GTL+. Please find the reference schematic and recommend value for passive component in the [Typical Application](#).

9.2 Typical Application

9.2.1 GTL–/GTL/GTL+ to LVTTTL

Select appropriate VTT/VREF based upon GTL–/GTL/GTL+. The parameters in [Recommended Operating Conditions](#) are compliant to the GTL specification.

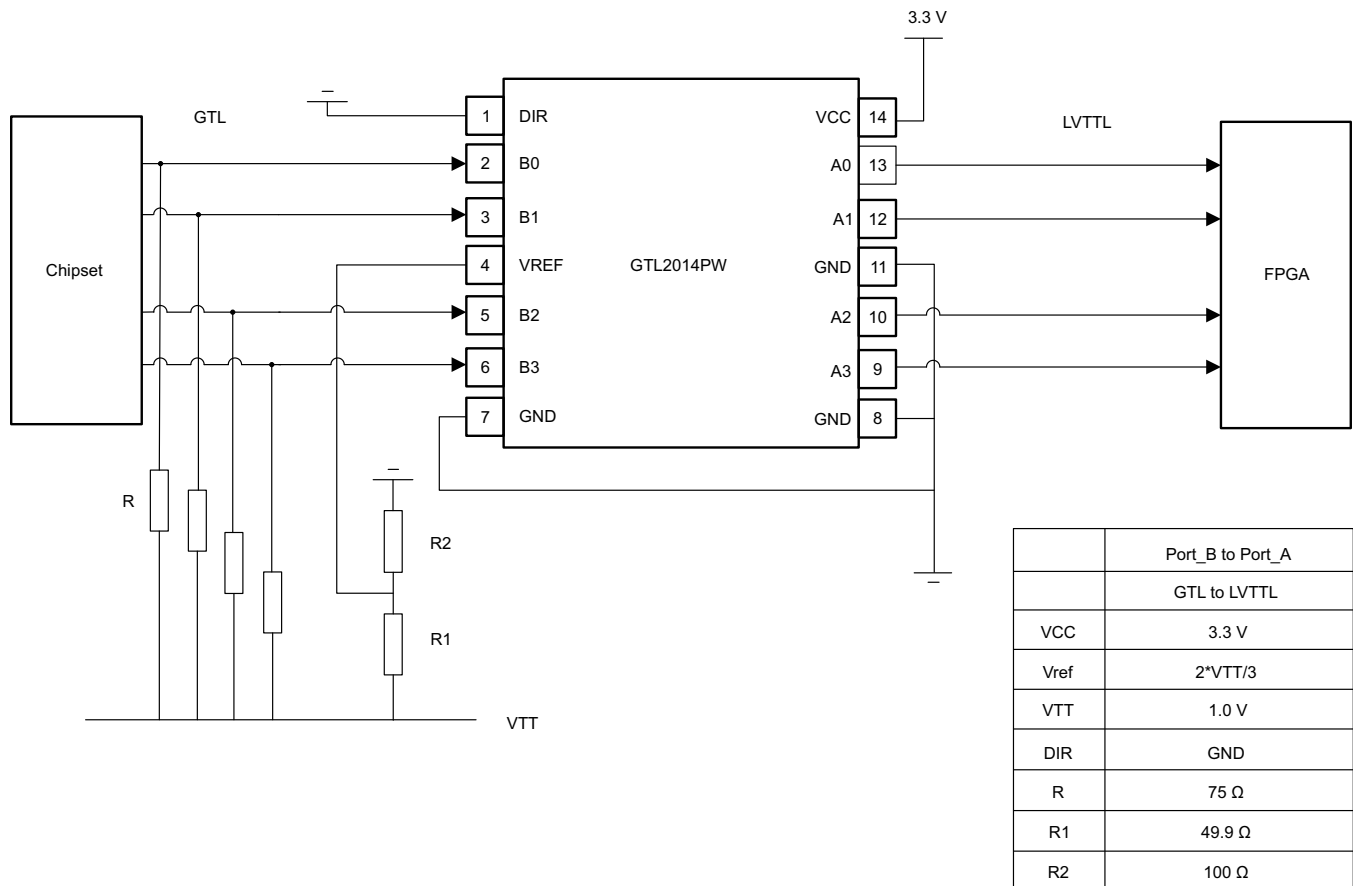


Figure 5. Application Diagram for GTL to LVTTTL

Typical Application (continued)

9.2.1.1 Design Requirements

The GTL2014 requires industrial standard LVTTTL and GTL inputs. The design example in [Application Information](#) show standard voltage level and typical resistor values.

NOTE

Only LVTTTL terminals (A1/A2/A3/A4) are tolerant to 5 V.

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Select direction base upon application (GTL–/GTL/GTL+ to LVTTTL or LVTTTL to GTL–/GTL/GTL+).
2. Set up appropriate DIR pin and VREF/VTTL.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LVTTTL to GTL–/GTL/GTL+).

9.2.1.3 Application Curve

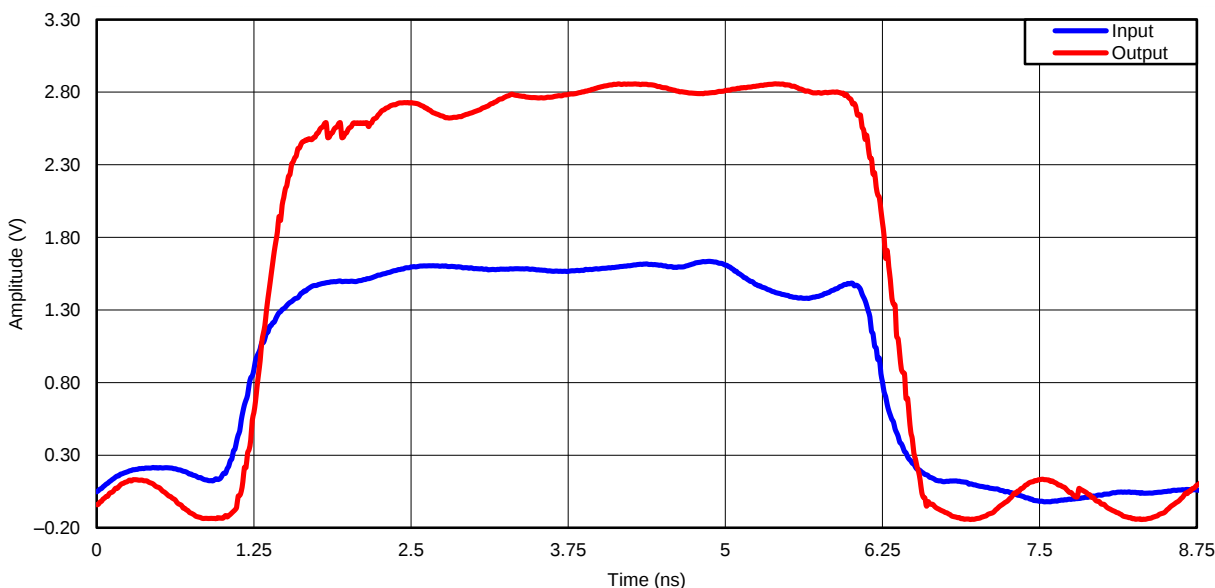


Figure 6. GTL-to-LVTTTL, VREF = 1 V, VIN = 1.5 V, 100 MHz

Typical Application (continued)

9.2.2 LVTTL/TTL to GTL–/GTL/GTL+

Because GTL is an open-drain interface, the selection of pullup resistor depends on the application requirement (for example, data rate) and PCB trace capacitance.

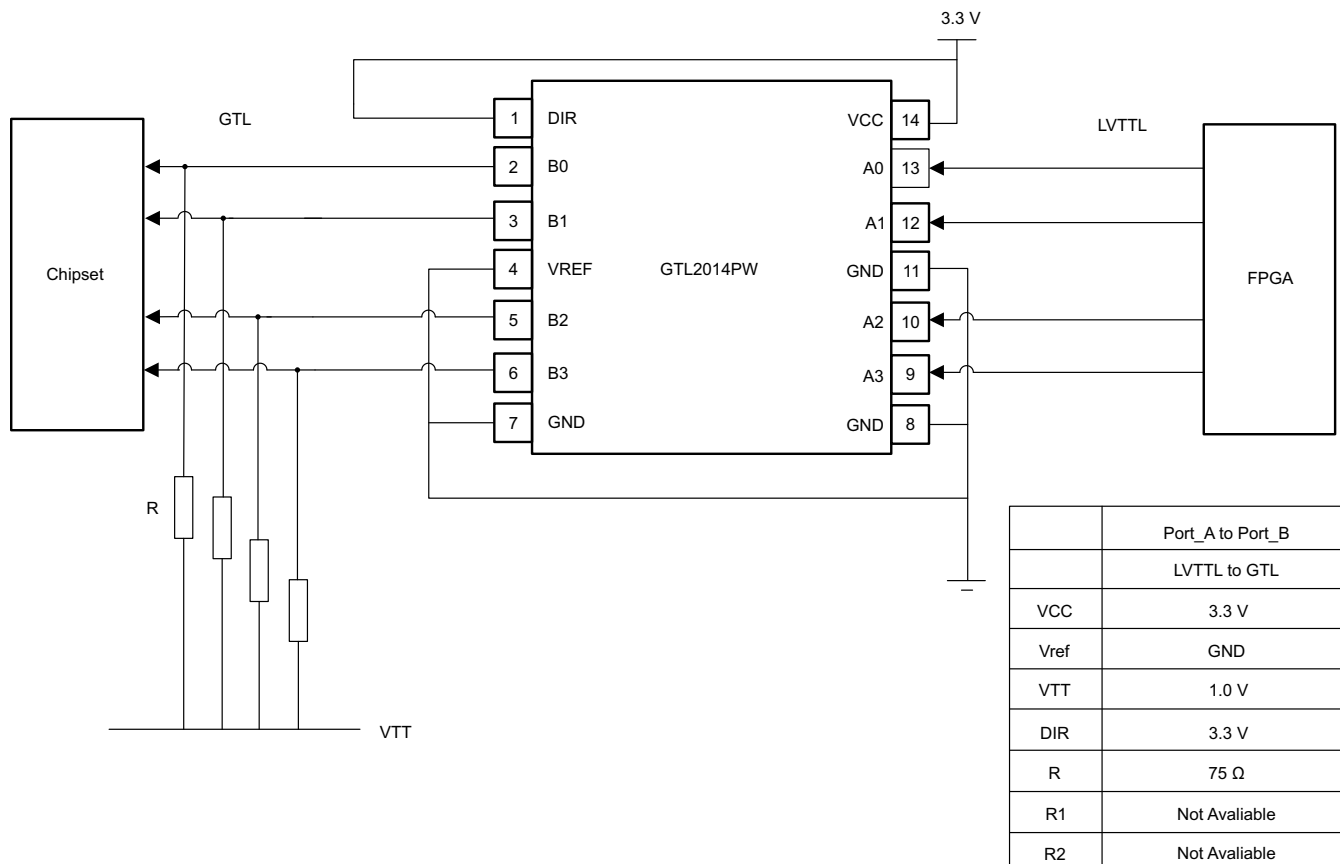


Figure 7. Application Diagram for LVTTL to GTL

9.2.2.1 Design Requirements

The GTL2014 requires industrial standard LVTTL and GTL inputs. The design example in the [Application Information](#) section show standard voltage level and typical resistor values.

NOTE

Only LVTTL terminals (A1/A2/A3/A4) are tolerant to 5 V.

9.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Select direction based upon application (GTL–/GTL/GTL+ to LVTTL or LVTTL to GTL–/GTL/GTL+).
2. Set up appropriate DIR pin and VREF/VTT.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LVTTL to GTL–/GTL/GTL+).

Typical Application (continued)

9.2.2.3 Application Curve

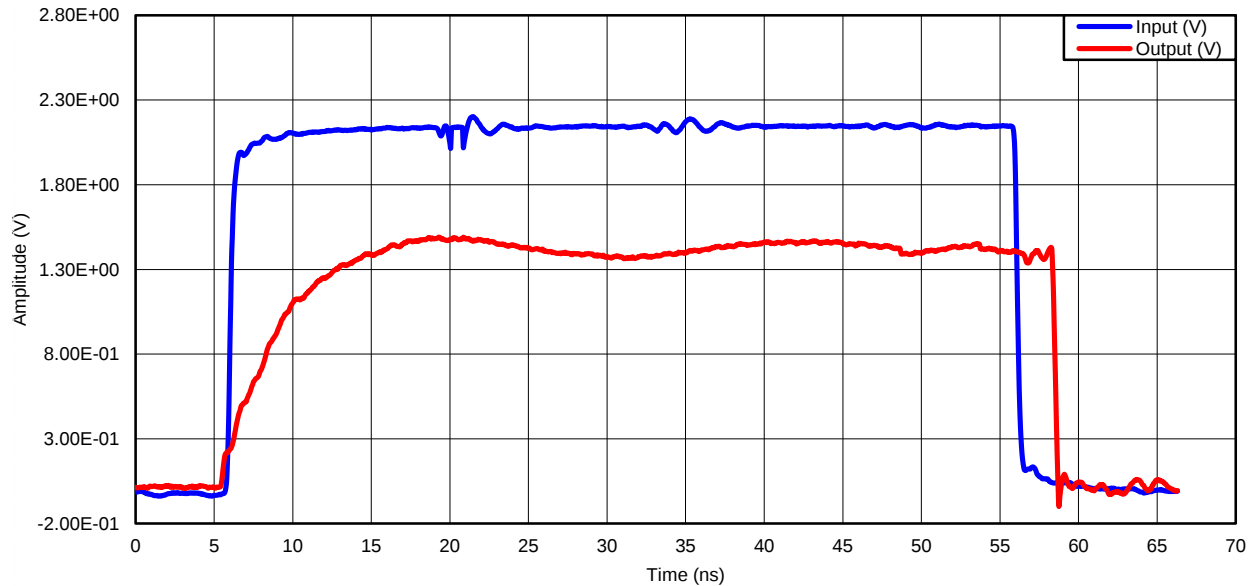


Figure 8. LVTTL-to-GTL, VREF = 1 V, VTT = 1.5 V, 10 MHz

10 Power Supply Recommendations

Because GTL is a low voltage interface, TI recommends a 0.1-μF decoupling capacitor for VREF.

11 Layout

11.1 Layout Guidelines

Typically, GTL/LVTTL is running at a low data rate; however, the GTL2014 is optimized for excellent propagation delay, slew rate, bandwidth, and is able support 100-MHz frequencies.

11.2 Layout Example

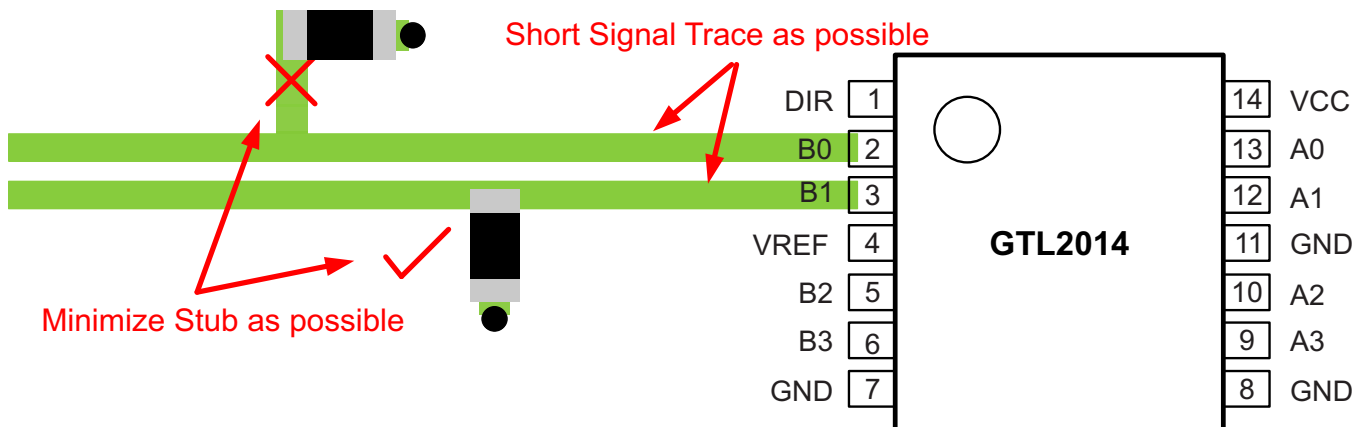


Figure 9. Layout Example for GTL Trace

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.3 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTL2014PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	GT14
SN74GTL2014PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GT14
SN74GTL2014PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GT14
SN74GTL2014PWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GT14

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

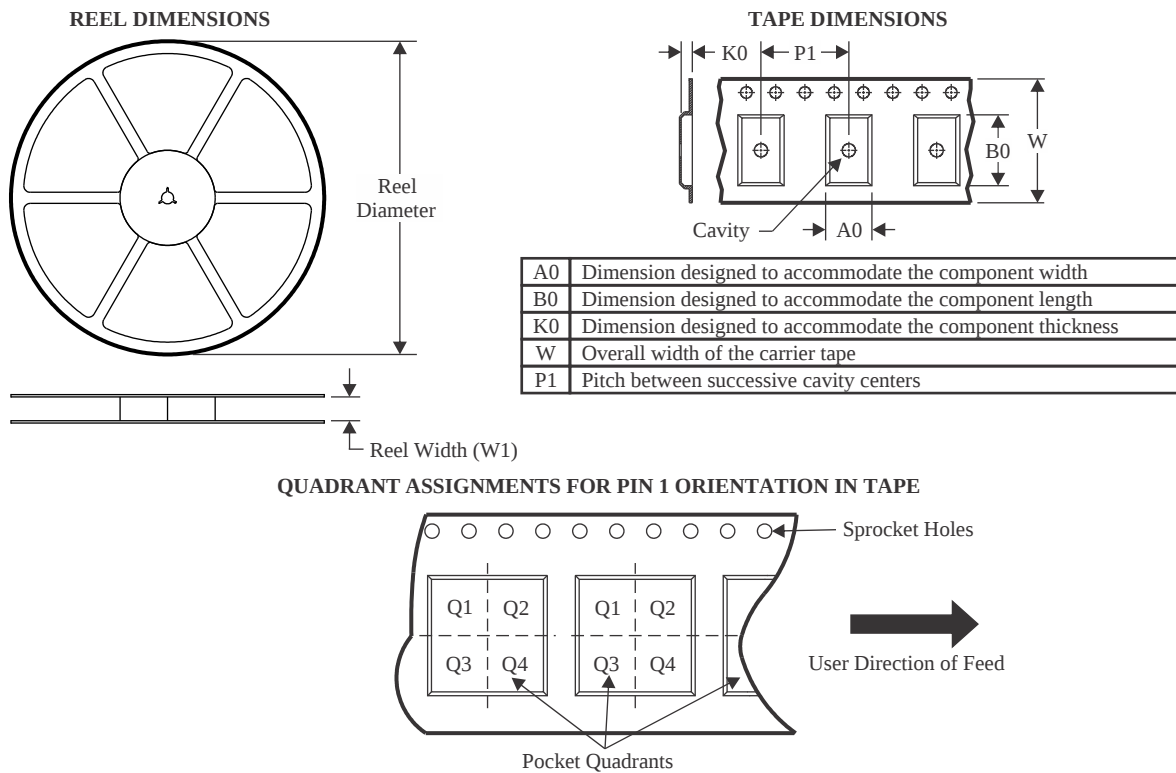
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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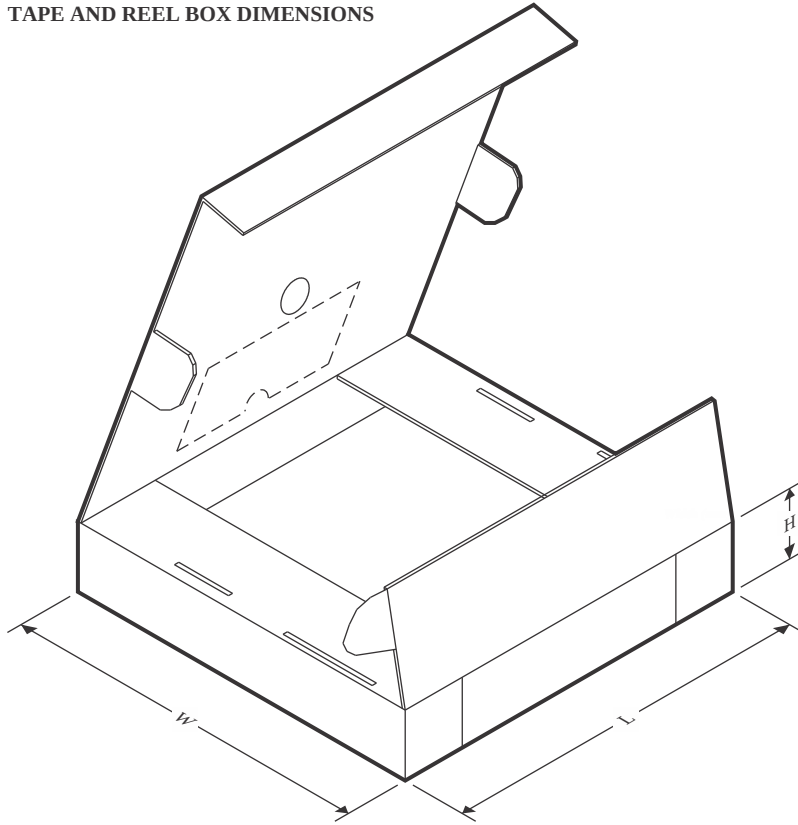
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2014PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74GTL2014PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

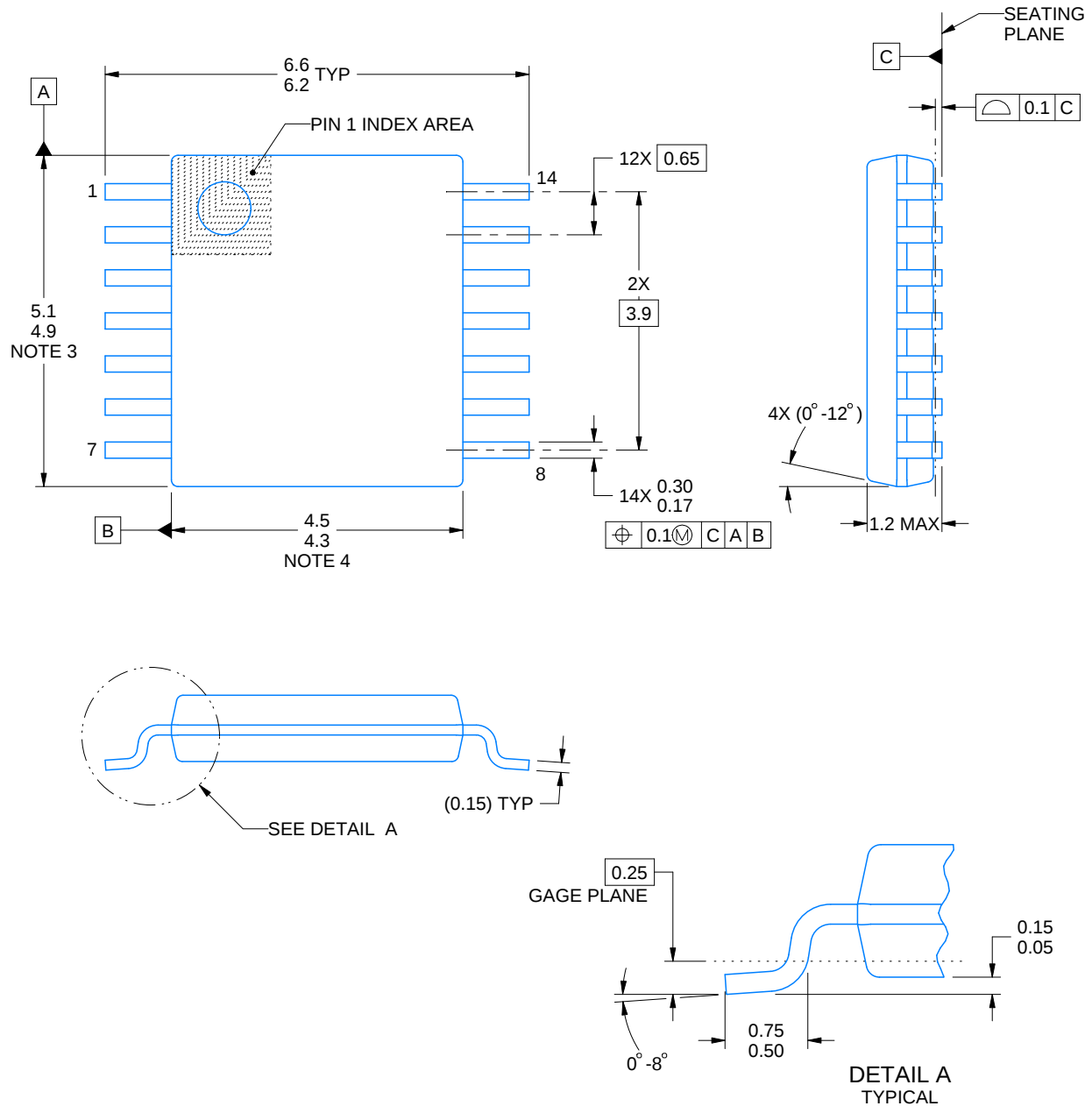
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2014PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74GTL2014PW RG4	TSSOP	PW	14	2000	353.0	353.0	32.0

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

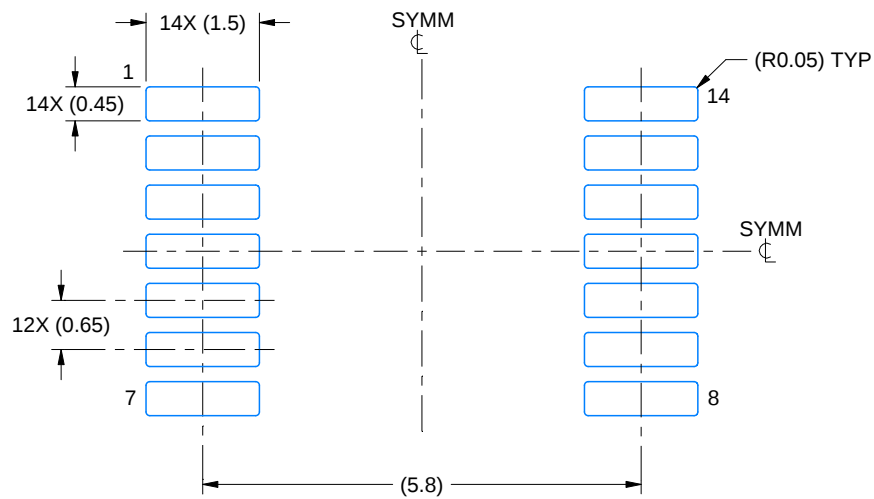
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

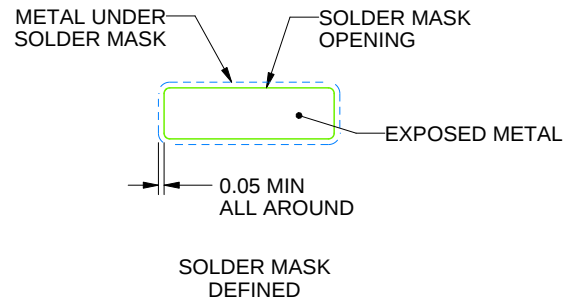
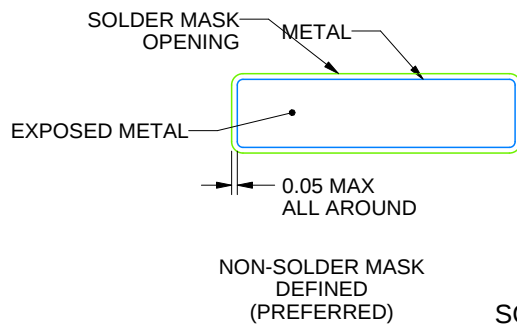
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

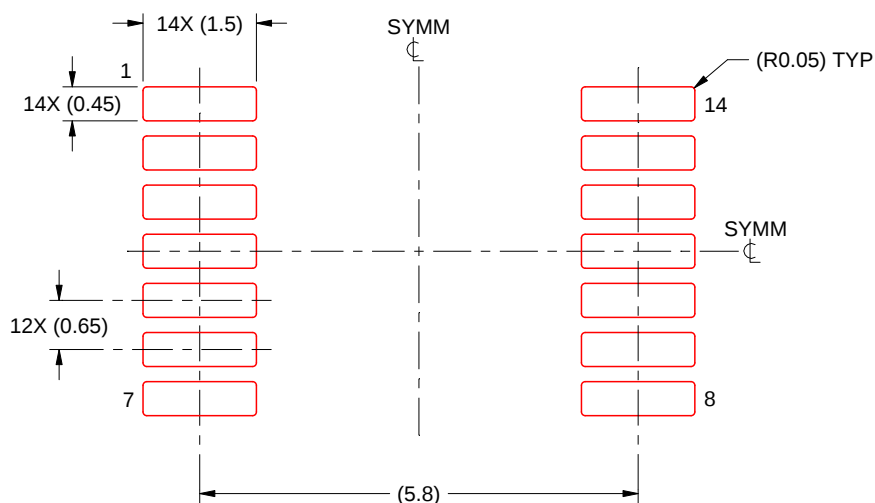
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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