

SN74F1016

16-BIT SCHOTTKY BARRIER DIODE R-C BUS-TERMINATION ARRAY

SDFS093 – NOVEMBER 1992 – REVISED DECEMBER 1993

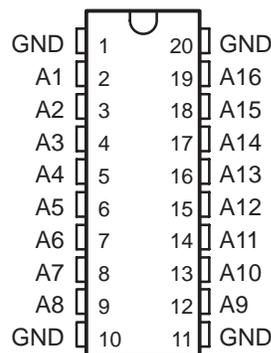
- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 300 mA
- 16-Bit Array Structure Suited for Bus-Oriented Systems

description

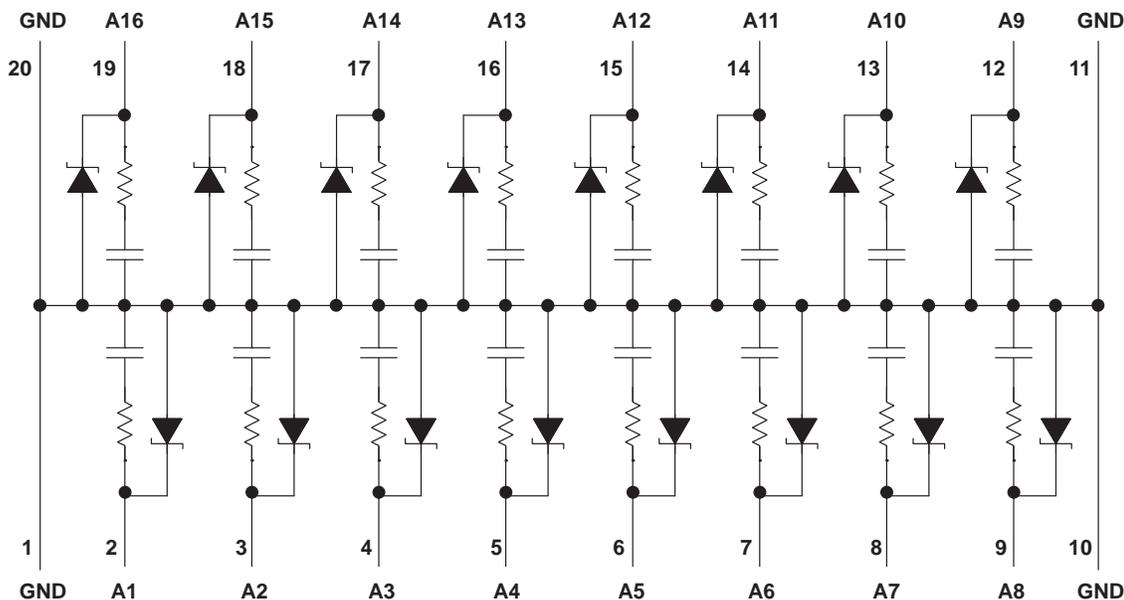
This bus-termination array is designed to reduce reflection noise and minimize ringing on high-performance bus lines. The SN74F1016 features a 16-bit R-C network and Schottky barrier diode array. These Schottky diodes provide clamp-to-ground functionality and serve to minimize overshoot and undershoot of high-speed switching buses.

The SN74F1016 is characterized for operation from 0°C to 70°C.

DW PACKAGE
(TOP VIEW)



schematic diagram



- Resistor = 50 Ω ± 10%
 Capacitor = 47 pF ± 10%, V_R = 2.5 V, f = 1 MHz
 Diode = Schottky

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R	7 V
Continuous forward current, I_F : Any D terminal from GND	50 mA
Total through all GND terminals	170 mA
Repetitive peak forward current, I_{FRM}^\ddagger : Any D terminal from GND	300 mA
Total through all GND terminals	1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_W \leq 100 \mu\text{s}$, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_R Static reverse current	$V_R = 7 \text{ V}$			2	μA
V_{FM} Peak forward voltage	$I_F = 200 \text{ mA}$		1.25		V
C_t Total capacitance	$V_R = 0$			80	pF
	$V_R = 2 \text{ V}$			60	
	$V_R = 3 \text{ V}$			55	

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_x Internal crosstalk current	Total GND current = 1.2 A, See Note 2		10	50	μA

NOTE 2: I_x is measured under the following conditions with one diode static, all others switching:

Switching diodes: $t_W = 100 \mu\text{s}$, duty cycle = 20%;

Static diode: $V_R = 5 \text{ V}$; the static diode input current is the internal crosstalk current I_x .

switching characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{rr} Reverse recovery time	$I_F = 10 \text{ mA}$, $I_{RM(REC)} = 10 \text{ mA}$, $I_{R(REC)} = 1 \text{ mA}$, $R_L = 100 \Omega$		8	10	ns

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{US} Undershoot voltage	$t_f = 2 \text{ ns}$, $t_W = 50 \text{ ns}$, $V_{IH} = 5 \text{ V}$, $V_{IL} = 0$, $Z_S = 25 \Omega$, $Z_O = 50 \Omega$, $L = 36\text{-inch coaxial cable}$		0.7	0.8	V



APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1016 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in Figure 1. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current voltage for the SN74F1016 is shown in Figure 1.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

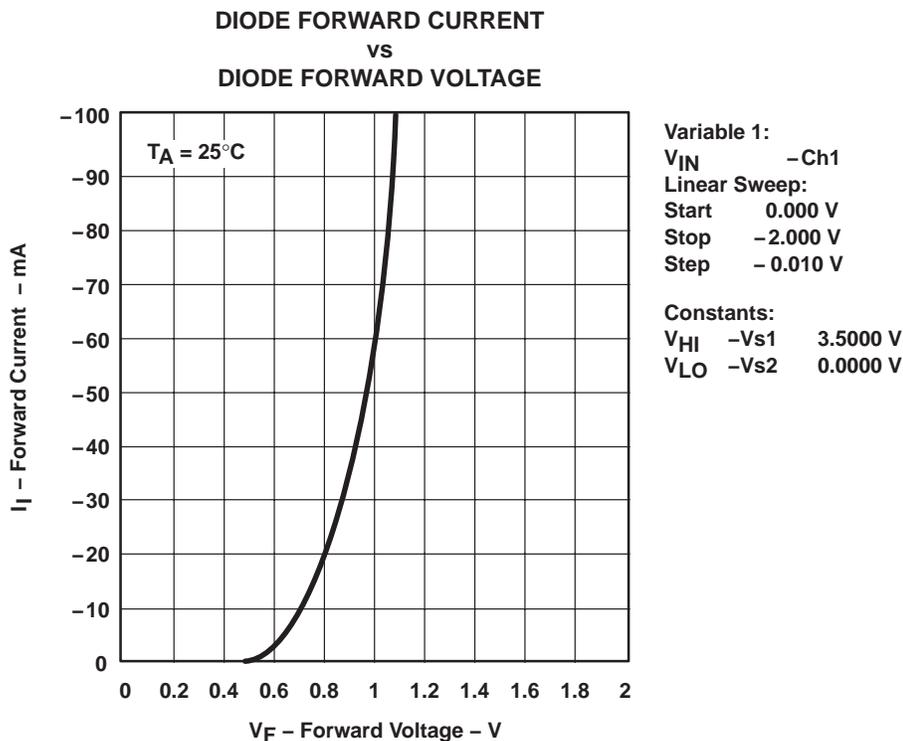
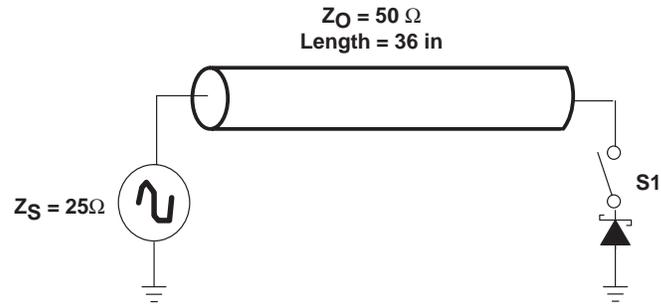


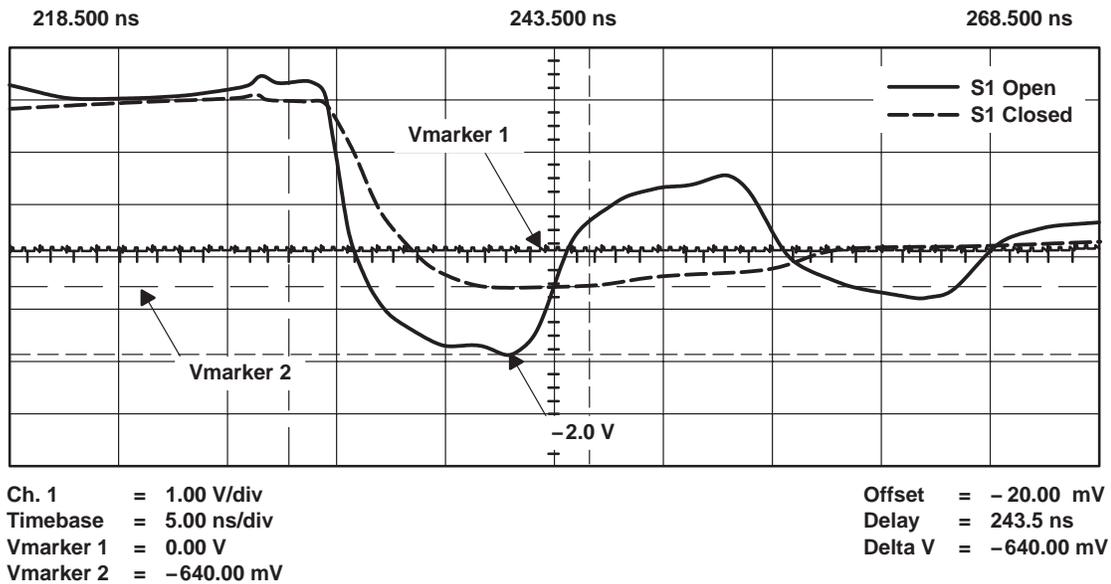
Figure 1

SN74F1016
16-BIT SCHOTTKY BARRIER DIODE
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(a) UNDERSHOOT TEST SETUP



(b) SCOPE DISPLAY

Figure 2. Undershoot Test Setup and Scope Display

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F1016DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	F1016
SN74F1016DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F1016
SN74F1016DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F1016

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

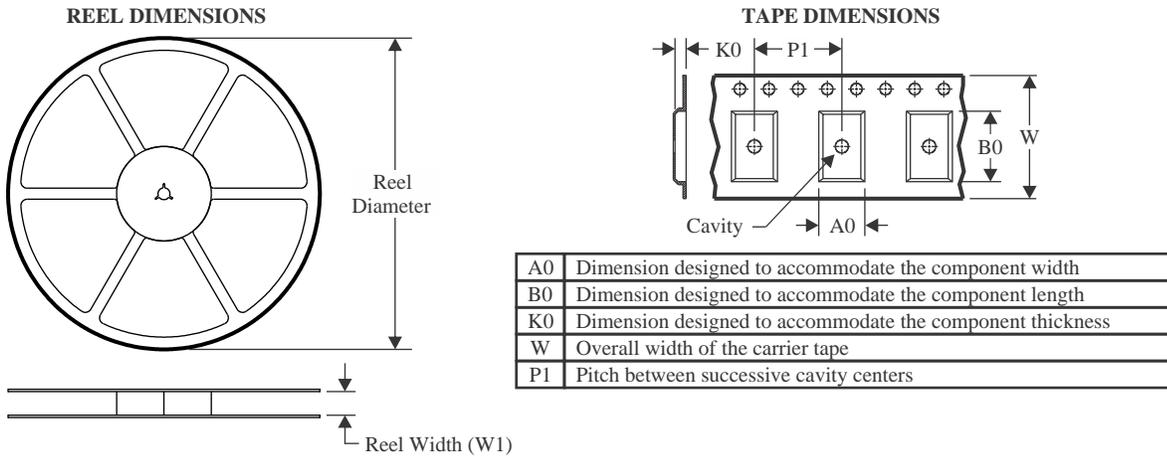
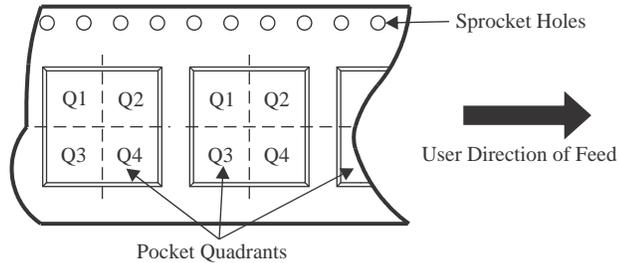
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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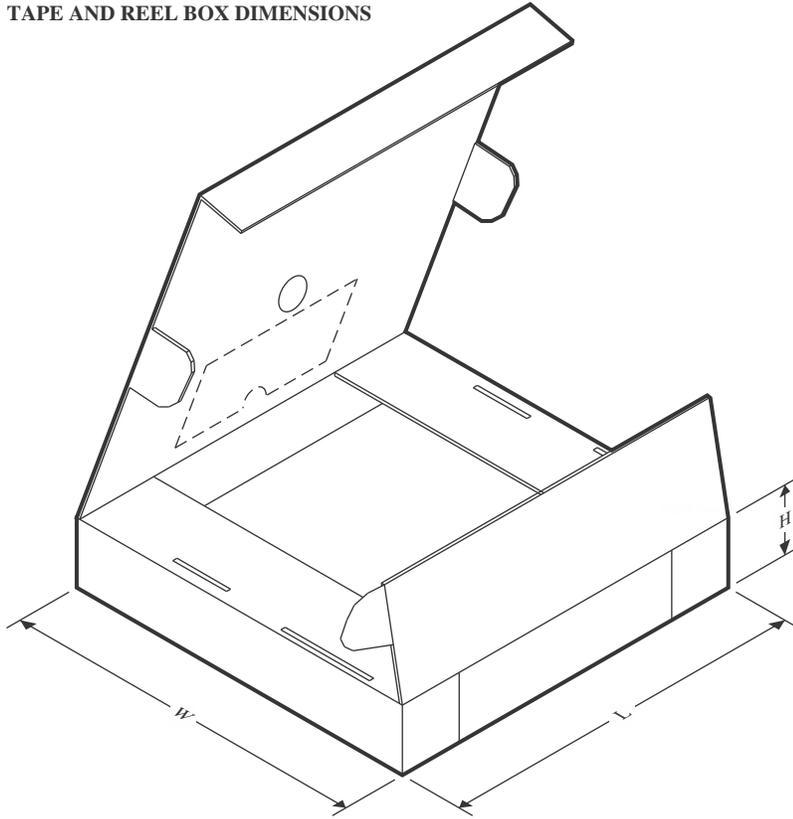
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F1016DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F1016DWR	SOIC	DW	20	2000	350.0	350.0	43.0

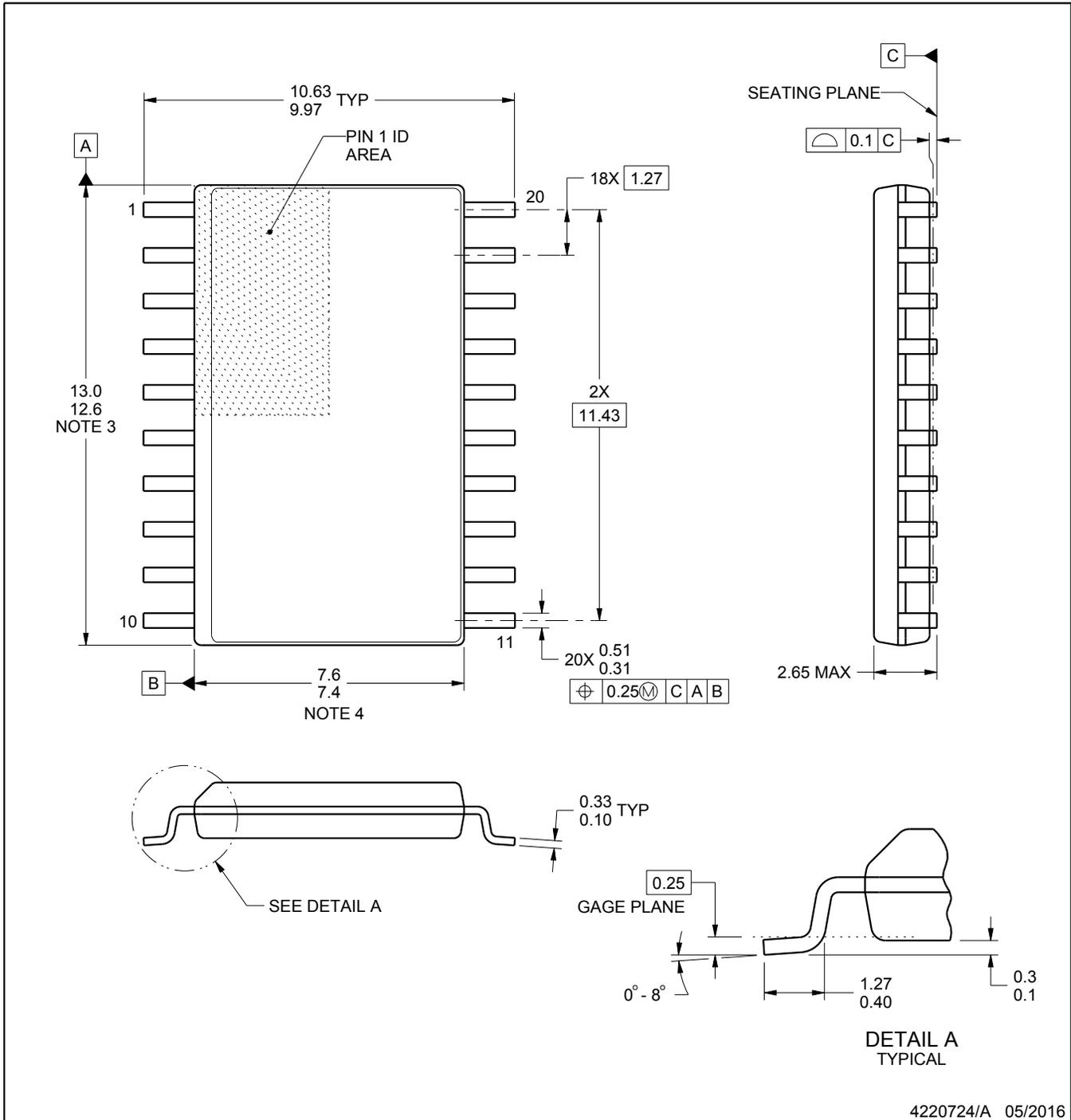
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

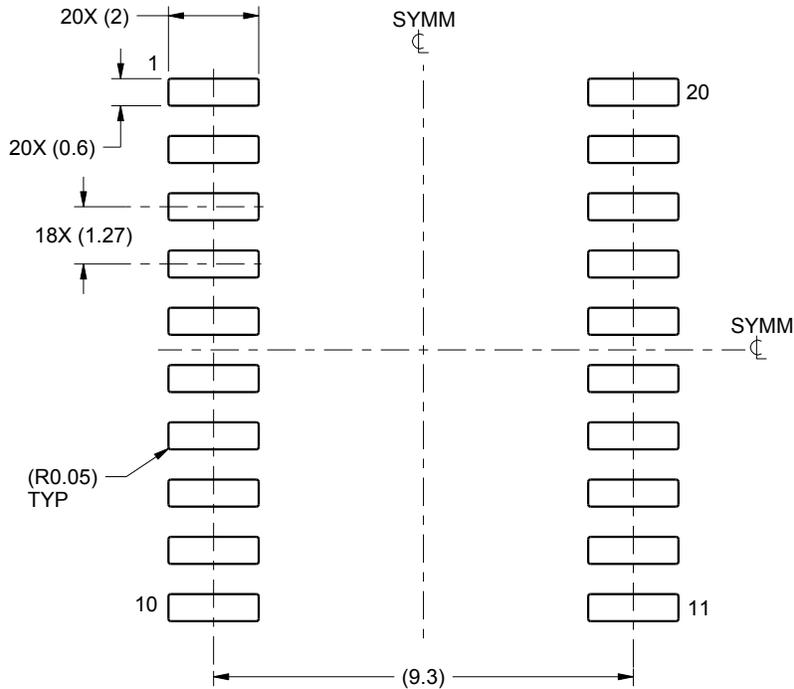
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

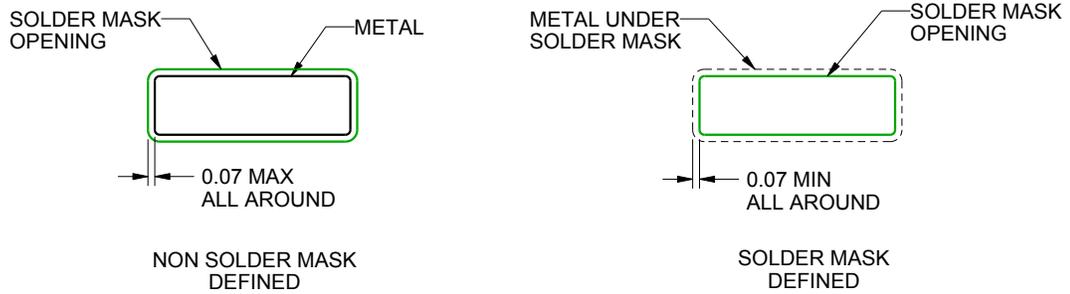
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

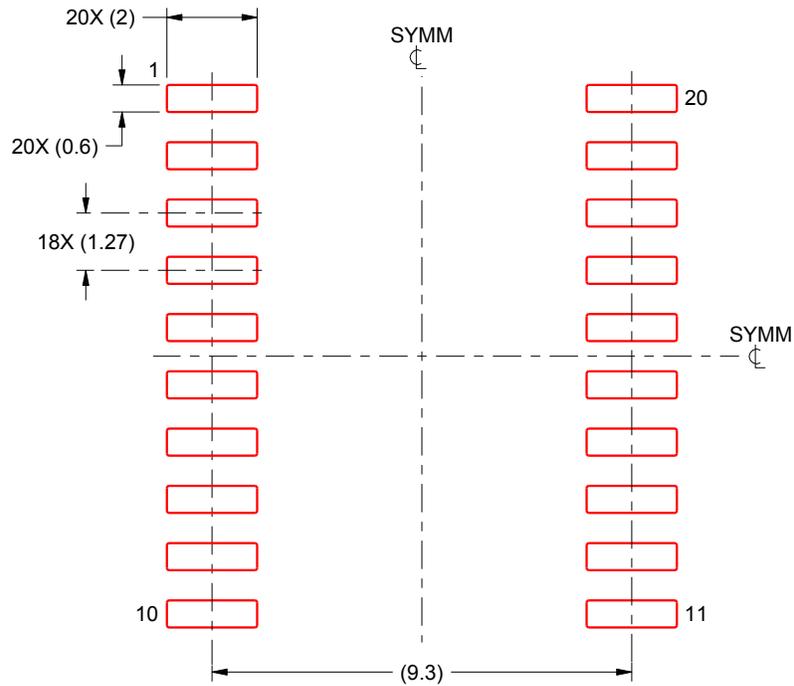
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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