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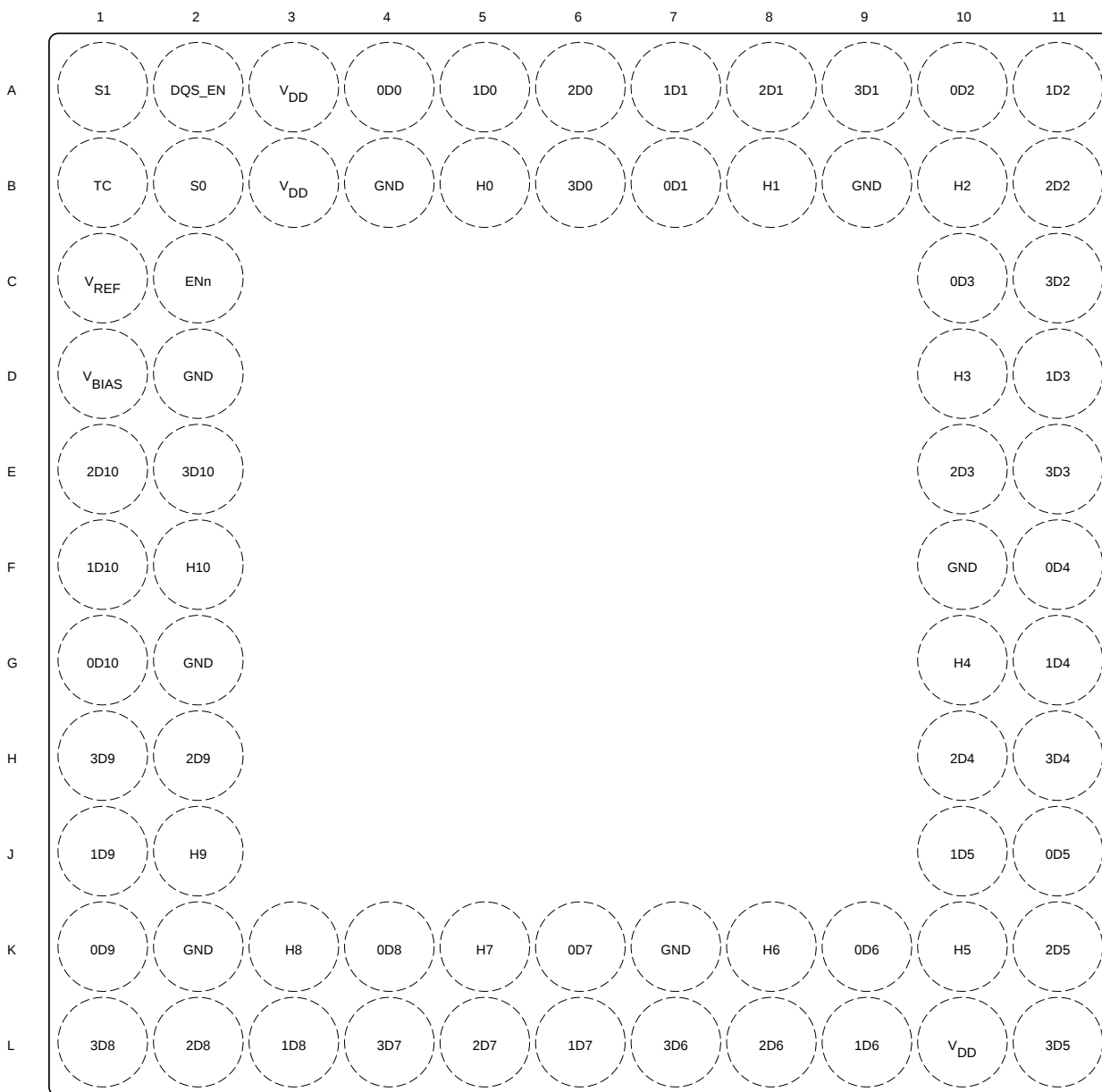
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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2018) to Revision C (September 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了数据表，以包含丰富的术语.....	1
Changes from Revision A (February 2016) to Revision B (April 2018)	Page
• Changed the $V_{BIAS\ MAX}$ value From: $0.33 \times V_{DD}$ To: V_{DD} in the <i>Recommended Operating Conditions</i> table....	6
Changes from Revision * (April 2005) to Revision A (February 2016)	Page
• 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Removed <i>Pin Assignments</i> table due to updated <i>Pin Out Drawing</i>	3

5 Pin Configuration and Functions



**图 5-1. ZST Package
72-Pin NFBGA
Top View**

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
0D0	A4	I/O	D0 port0
0D1	B7	I/O	D1 port0
0D2	A10	I/O	D2 port0
0D3	C10	I/O	D3 port0
0D4	F11	I/O	D4 port0

表 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
0D5	J11	I/O	D5 port0
0D6	K9	I/O	D6 port0
0D7	K6	I/O	D7 port0
0D8	K4	I/O	D8 port0
0D9	K1	I/O	D9 port0
0D10	G1	I/O	D10 port0
1D0	A5	I/O	D0 port1
1D1	A7	I/O	D1 port1
1D2	A11	I/O	D2 port1
1D3	D11	I/O	D3 port1
1D4	G11	I/O	D4 port1
1D5	J10	I/O	D5 port1
1D6	L9	I/O	D6 port1
1D7	L6	I/O	D7 port1
1D8	L3	I/O	D8 port1
1D9	J1	I/O	D9 port1
1D10	F1	I/O	D10 port1
2D0	A6	I/O	D0 port2
2D1	A8	I/O	D1 port2
2D2	B11	I/O	D2 port2
2D3	E10	I/O	D3 port2
2D4	H10	I/O	D4 port2
2D5	K11	I/O	D5 port2
2D6	L8	I/O	D6 port2
2D7	L5	I/O	D7 port2
2D8	L2	I/O	D8 port2
2D9	H2	I/O	D9 port2
2D10	E1	I/O	D10 port2
3D0	B6	I/O	D0 port3
3D1	A9	I/O	D1 port3
3D2	C11	I/O	D2 port3
3D3	E11	I/O	D3 port3
3D4	H11	I/O	D4 port3
3D5	L11	I/O	D5 port3
3D6	L7	I/O	D6 port3
3D7	L4	I/O	D7 port3
3D8	L1	I/O	D8 port3
3D9	H1	I/O	D9 port3
3D10	E2	I/O	D10 port3
DQS_EN	A2	I	D10 port output voltage control
ENn	C2	I	Active low enable input
GND	B4, B9, F10, K7, K2, G2, D2	P	Ground
H0	B5	I/O	H port0
H1	B8	I/O	H port1

表 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
H2	B10	I/O	H port2
H3	D10	I/O	H port3
H4	G10	I/O	H port4
H5	K10	I/O	H port5
H6	K8	I/O	H port6
H7	K5	I/O	H port7
H8	K3	I/O	H port8
H9	J2	I/O	H port9
H10	F2	I/O	H port10
S0	B2	I	Select input control
S1	A1	I	Select input control
TC	B1	I	Termination control input
V _{BIAS}	D1	P	Bias voltage
V _{DD}	A3, B3, L10	P	Power supply
V _{REF}	C1	P	Reference voltage

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{DD}	Supply voltage		- 0.5	2.5	V
V _{IN}	Control input voltage ^{(2) (3)}		- 0.5	2.5	V
V _{I/O}	Switch I/O voltage ^{(2) (3) (4)}		- 0.5	2.5	V
I _{IK}	Control input clamp current	V _{IN} < 0 or V _{IN} > 0		±50	mA
I _{I/O}	I/O port clamp current	V _{I/O} < 0 or V _{I/O} > 0		±50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±100	mA
	Continuous current through V _{DD} or GND pins			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [§ 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage		1.7	1.8	1.9	V
V _{REF}	Reference supply voltage		0.49 × V _{DD}	0.5 × V _{DD}	0.51 × V _{DD}	V
V _{BIAS}	BIAS supply voltage		0	0.3 × V _{DD}	V _{DD}	V
V _{IH}	High-level control input voltage	S	V _{REF} + 250 mV			V
		EN, TX, DQS_EN	0.65 × V _{DD}			
V _{IL}	Low-level control input voltage	S	V _{REF} - 250 mV			V
		EN, TX, DQS_EN	0.35 × V _{DD}			
V _{I/O}	Data input/output voltage		0		V _{DD}	V
T _A	Operating free-air temperature		0		85	°C

- (1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74CBTU4411	UNIT
		ZST (NFBGA)	
		72 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Minimum and maximum limits apply for $T_A = 0^\circ\text{C}$ to 85°C (unless otherwise noted). Typical limits apply for $V_{DD} = 1.8\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted).⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK} ⁽²⁾	Control inputs ⁽³⁾	$V_{DD} = 1.7\text{ V}$, $I_{IN} = -18\text{ mA}$			-1.8	V
V_{BIAS_DQS}	D10	$V_{DD} = 1.7\text{ V}$, $DQS_EN = V_{DD}$	1.1		1.275	V
V_{OH}	D10	$V_{DD} = 1.7\text{ V}$, $DQS_EN = V_{DD}$, $\overline{EN} = V_{DD}$, $I_O = 100\text{ }\mu\text{A}$		1.6	1.8	V
I_{IN}	Control inputs ⁽³⁾	$V_{DD} = 1.9\text{ V}$, $V_{IN} = V_{DD}$ or GND			± 1	μA
I_{OZ} ⁽⁴⁾		$V_{DD} = 1.9\text{ V}$, $V_O = 0$ to 1.9 V , $V_I = 0$, Switch OFF, V_{BIAS} open			± 10	μA
I_{CC}		$V_{DD} = 1.9\text{ V}$, TC = GND, $\overline{EN} = \text{GND}$, $I_{I/O} = 0$, S0 or S1 input switching at 50% duty cycles, Data I/O are open		0.7	2.5	mA
		$\overline{EN} = V_{DD}$			500	μA
I_{CCD}		$V_{DD} = 1.9\text{ V}$, TC = GND, $\overline{EN} = \text{GND}$, $I_{I/O} = 0$, S0 or S1 input switching at 50% duty cycle, Data I/O are open			0.5	mA/MHz ⁽⁵⁾
C_{in}	S port	$V_{DD} = 1.9\text{ V}$, TC = GND, $\overline{EN} = \text{GND}$, $V_{IN} = V_{REF} \pm 250\text{ mV}$	2.5		3.5	pF
	$\overline{EN}$, TC, DQS_EN inputs	$V_{DD} = 1.9\text{ V}$, $V_{IN} = 0$ or 1.9 V		2.5		
$C_{io(OFF)}$	H port	$V_{I/O} = 0.5 \times V_{DD} \pm 0.4\text{ V}$, Switch OFF, V_{BIAS} open			2.5	pF
$C_{io(ON)}$		$V_{I/O} = 0.5 \times V_{DD} \pm 0.4\text{ V}$, Switch ON, $V_{BIAS} = \text{GND}$			4.6	pF
r_{on} ⁽⁶⁾		$V_{DD} = 1.7\text{ V}$, $V_I = 0.5 \times V_{DD} \pm 0.5\text{ V}$, $I_O = 10\text{ mA}$	6	10	17	Ω
$\Delta r_{on(Flat)}$ ⁽⁷⁾		$V_{DD} = 1.7\text{ V}$, $DQS_EN = V_{DD}$, $I_O = 10\text{ mA}$		1.5	3	Ω
		$V_I = 0.5 V_{DD} \pm 0.25\text{ V}$ $V_I = 0.5 V_{DD} \pm 0.5\text{ V}$		2.5	5	
r_{term}	S port	$V_{DD} = 1.7\text{ V}$	110	160	210	Ω
$r_{pulldown}$	D0 - D10	$V_{DD} = 1.7\text{ V}$	280	400	520	Ω
	D10	$DQS_EN = V_{DD}$, $\overline{EN} = \text{GND}$	1600	2300	3000	
r_{pullup}	D10	$V_{DD} = 1.7\text{ V}$, $DQS_EN = V_{DD}$, $\overline{EN} = \text{GND}$	700	1000	1300	Ω

- (1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.
- (2) V_{IK} refers to the clamp voltage due to the internal diode, which is connected from each control input to GND.
- (3) For the leakage current test on S0 and S1, $\overline{EN}$ and TC inputs are set to low.
- (4) For I/O ports, the parameter I_{OZ} includes the input leakage current. I_{OZ} applies only to the H port.
- (5) This frequency of S0 and S1 inputs, for example, for a data I/O rate of 533 Mbit/s, with a burst of 4, the required frequency is for S0 or S1 input is $\approx 66\text{ MHz}$ ($533/8$). The total I_{CC} due to switching S0, S1 will be approximately 27 mA ($66\text{ MHz} \times 0.4\text{ mA/MHz}$).
- (6) Measured by the voltage drop between the D and H pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or H) pins.
- (7) $\Delta r_{on(Flat)}$ is the difference of maximum r_{on} and minimum r_{on} for a specific channel in a specific device.

6.6 Switching Characteristics

$T_A = 0^\circ\text{C}$ to 85°C (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$	D or H port		400			MHz
	S port ⁽¹⁾		84			
t_{pd}		From D or H (input) to D or H (output)		297		ps
$t_{en}(t_{pZL}, t_{pZH})^{(2)}$		From S (input) to D (output)	750		2100	ps
$t_{dis}(t_{pLZ}, t_{pHZ})^{(2)}$		From S (input) to D (output)	750		2100	ps
t_{osk}					85	ps
t_{esk}					40	ps
$t_{start}^{(3)}$				20		μs

(1) $\overline{\text{EN}} = \text{GND}$, $\text{TC} = \text{GND}$

(2) $V_{\text{BIAS}} = \text{open}$

(3) t_{start} is the time required for the charge-pump circuit output voltage to reach a steady state value after V_{DD} is applied.

6.7 Typical Characteristic

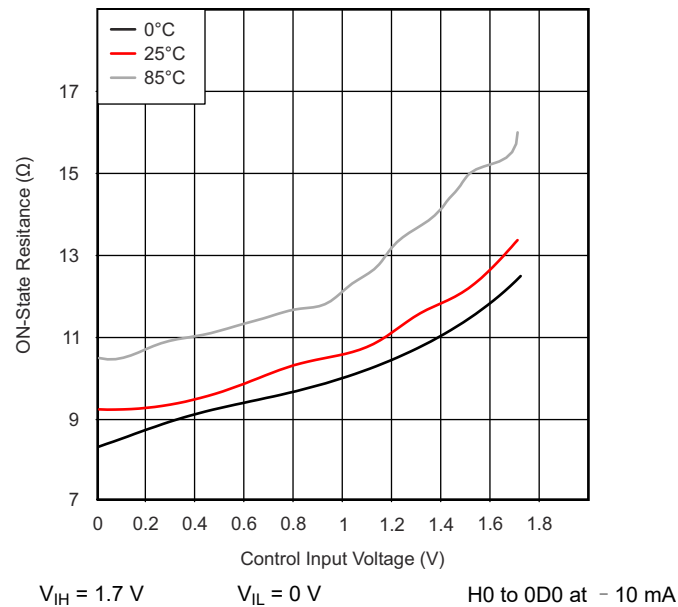
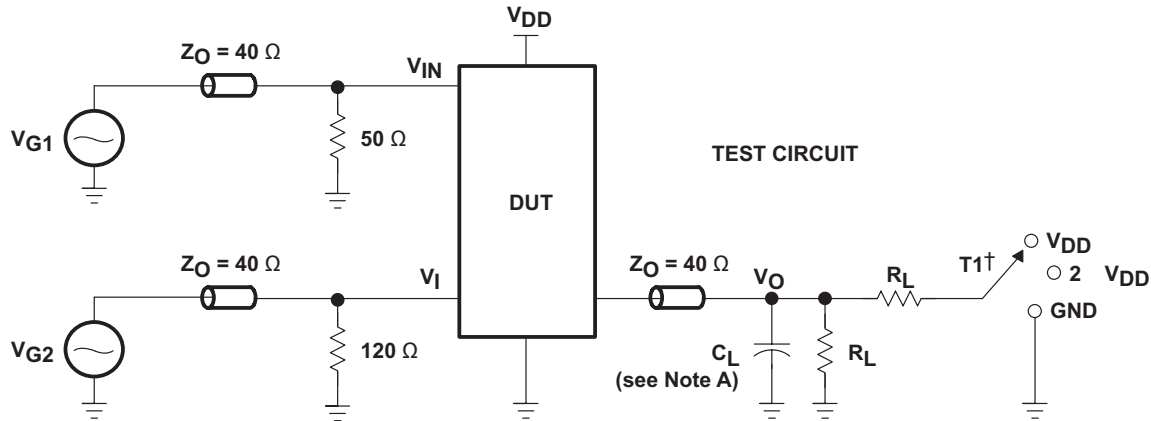


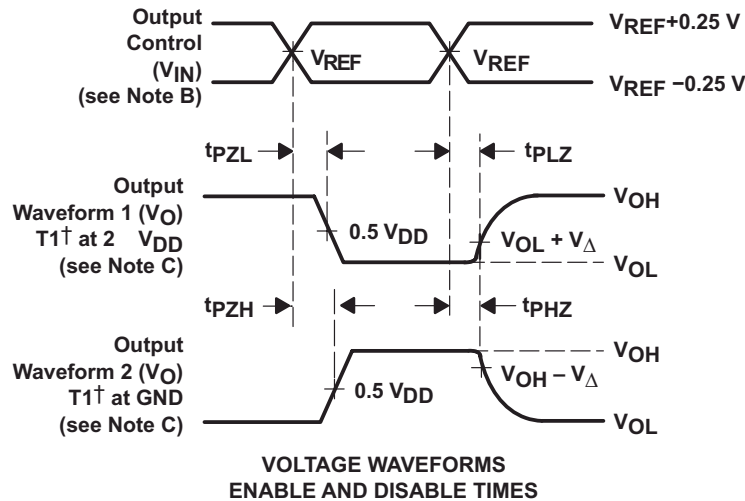
图 6-1. ON-State Resistance Across Temperature

7 Parameter Measurement Information

7.1 Enable and Disable Times



TEST	V _{DD}	T1†	R _L	V _I	C _L	V _Δ
t _{PLZ} /t _{PZL}	1.8 V ± 0.1 V	2 × V _{DD}	1 kΩ	GND	6 pF	0.125 V
t _{PHZ} /t _{PZH}	1.8 V ± 0.1 V	GND	1 kΩ	V _{DD}	6 pF	0.125 V

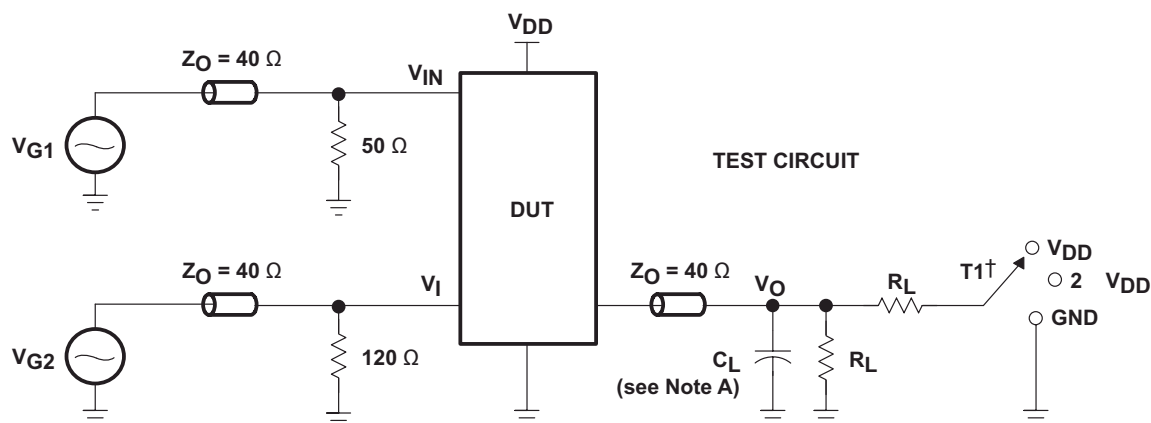


† T1 is an external terminal.

- A. C_L includes probe and jig capacitance.
- B. Output control applies to select (S0, S1) inputs.
- C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.
- E. The outputs are measured one at a time, with one transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- G. t_{PZL} and t_{PZH} are the same as t_{en}.

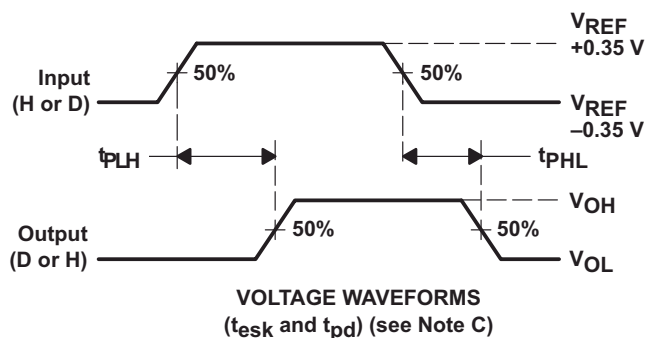
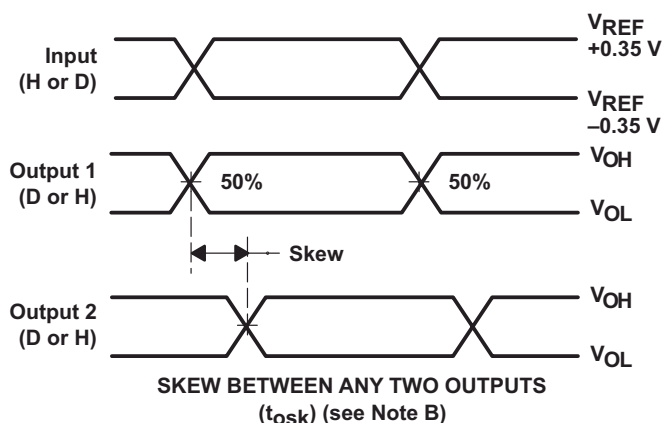
图 7-1. Test Circuit and Voltage Waveforms

7.2 Skew and Propagation Delay Times



TEST	V _{DD}	T1†	R _L	V _I	C _L
t _{pd}	1.8 V ± 0.1 V	V _{DD}	150 Ω	See waveform	6 pF
t _{osk}	1.8 V ± 0.1 V	V _{DD}	150 Ω	See waveform	6 pF
t _{esk}	1.8 V ± 0.1 V	V _{DD}	150 Ω	See waveform	6 pF

† T1 is an external terminal.



- C_L includes probe and jig capacitance.
- t_{osk} is the difference in output voltage from channel to channel in a specific device.
- t_{PLH} and t_{PHL} are the same as t_{pd} and t_{esk} = |t_{PLH} - t_{PHL}|
- All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.
- The outputs are measured one at a time, with one transition per measurement.

图 7-2. Test Circuit and Voltage Waveforms

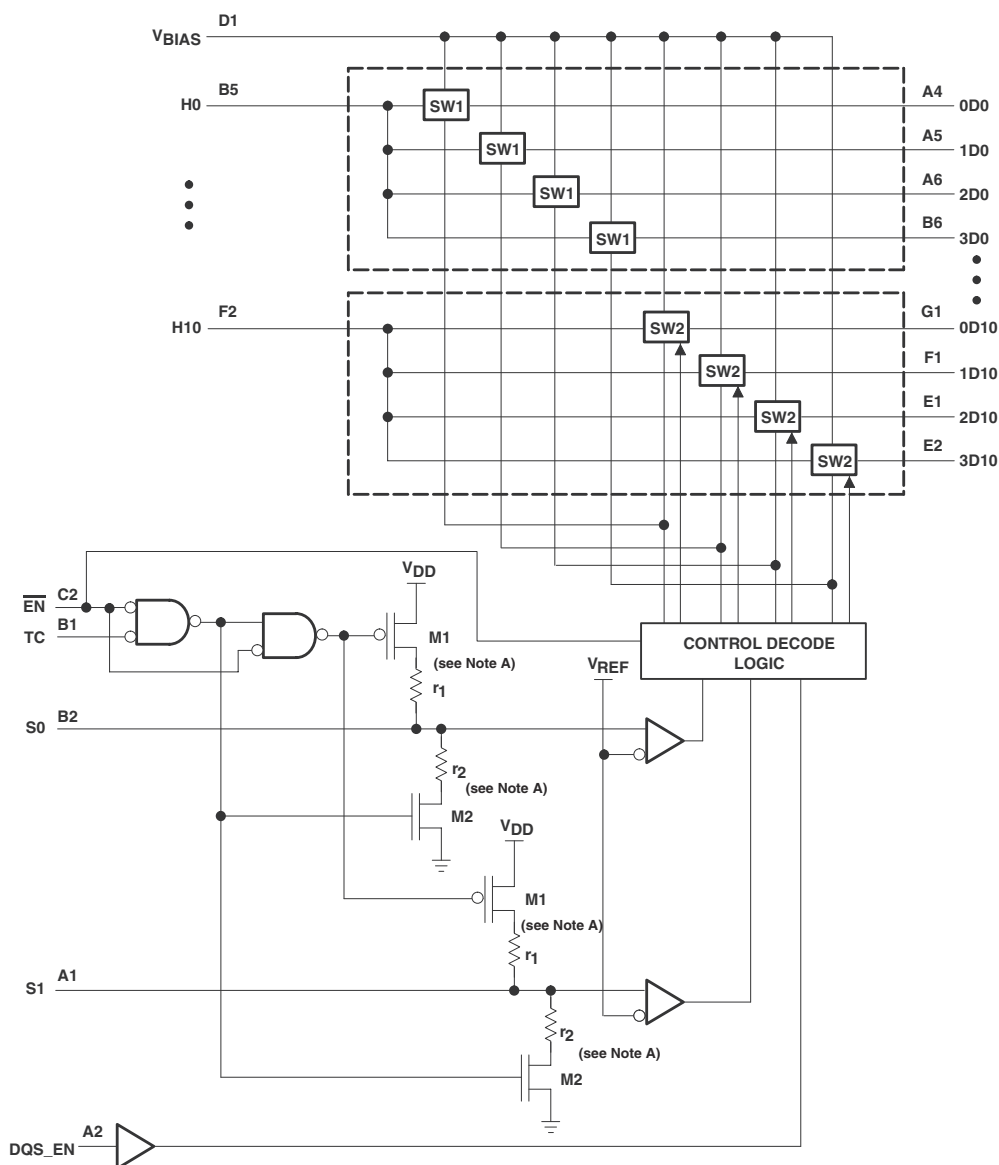
8 Detailed Description

8.1 Overview

The SN74CBTU4411 device is organized as an 11-bit 1-of-4 multiplexer or demultiplexer with a single switch-enable ($\overline{\text{EN}}$) input. When $\overline{\text{EN}}$ is low, the switch is enabled and the H port is connected to one of the D ports. Ports D0 to D9 for the disabled channels are connected to V_{BIAS} through a 400- Ω resistor. DQS_EN determines the output voltage for the disabled D10 ports. When DQS_EN is low, this voltage is V_{BIAS} . When DQS_EN is high, the disabled D10 ports are connected to an internal voltage ($V_{\text{BIAS_DQS}}$) source, which is approximately equal to 0.7 V_{DD} .

When $\overline{\text{EN}}$ is high, all the channels are disabled. Ports D0 to D9 are connected to V_{BIAS} . For the D10 port, the disabled output voltage is determined by the DQS_EN input. When DQS_EN is low, this voltage is V_{BIAS} . When DQS_EN is high, this voltage is V_{DD} .

8.2 Functional Block Diagram



A. $r_1 + r_{\text{on}}(\text{M1}), r_2 + r_{\text{on}}(\text{M2}) = 160 \, \Omega$ typical

图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. The $\overline{\text{EN}}$ and TC inputs determine the internal termination for S0 and S1 inputs. When $\overline{\text{EN}}$ is low, the termination is determined by the TC input. When both $\overline{\text{EN}}$ and TC are low, termination resistors are disconnected from the S inputs. When $\overline{\text{EN}}$ is low and TC is high, both pullup and pulldown resistors are connected to the S inputs. When $\overline{\text{EN}}$ is high, only the pulldown termination resistors are connected to the S inputs, regardless of the voltage level at the TC input.

8.4 Device Functional Modes

表 8-1 和 表 8-2 list the functional modes of the SN74CBTU4411.

表 8-1. Function Table

INPUTS				INPUT/OUTPUT Hn	FUNCTION
$\overline{\text{EN}}$	DQS_EN	S1	S0		
L	L	L	L	0Dn	Hn = 0Dn 1Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	L	H	1Dn	Hn = 1Dn 0Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	H	L	2Dn	Hn = 2Dn 0Dn, 1Dn, 3Dn connected to V_{BIAS}
L	L	H	H	3Dn	Hn = 3Dn 0Dn, 1Dn, 2Dn connected to V_{BIAS}
L	H	L	L	0Dn	H0 - H9 = 0D0 - 0D9 1D0 - 1D9, 2D0 - 2D9, 3D0 - 3D9 connected to V_{BIAS} H10 = 0D10 1D10, 2D10, 3D10 connected to $V_{\text{BIAS_DQS}}$ ⁽¹⁾
L	H	L	H	1Dn	H0 - H9 = 1D0 - 1D9 0D0 - 0D9, 2D0 - 2D9, 3D0 - 3D9 connected to V_{BIAS} H10 = 1D10 0D10, 2D10, 3D10 connected to $V_{\text{BIAS_DQS}}$ ⁽¹⁾
L	H	H	L	2Dn	H0 - H9 = 2D0 - 2D9 0D0 - 0D9, 1D0 - 1D9, 3D0 - 3D9 connected to V_{BIAS} H10 = 2D10 0D10, 1D10, 3D10 connected to $V_{\text{BIAS_DQS}}$ ⁽¹⁾
L	H	H	H	3Dn	H0 - H9 = 3D0 - 3D9 0D0 - 0D9, 1D0 - 1D9, 2D0 - 2D9 connected to V_{BIAS} H10 = 3D10 0D10, 1D10, 2D10 connected to $V_{\text{BIAS_DQS}}$ ⁽¹⁾
H	L	X	X	Z	0Dn, 1Dn, 2Dn, 3Dn connected to V_{BIAS}
H	H	X	X	Z	0D0 - 0D9, 1D0 - 1D9, 2D0 - 2D9, 3D0 - 3D9 connected to V_{BIAS} 0D10, 1D10, 2D10, 3D10 connected to V_{DD}

(1) $V_{\text{BIAS_DQS}}$ is an internal voltage condition.

表 8-2. Function Table Continued

INPUTS		FUNCTION
$\overline{\text{EN}}$	TC	
L	L	Termination resistors disconnected from S inputs
L	H	Termination resistors connected with S inputs
H	X	Pulldown termination resistor connected and pullup termination resistor disconnected from the S inputs

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74CBTU4411 is suitable for DDR-II applications where high-bandwidth is required. This device has low and flat ON resistance and has internal termination control inputs. The D-ports are precharged by Bias voltage (V_{BIAS}).

9.2 Typical Application

SN74CBTU4411 is an 11 bit, 1:4 Mux and suitable for high-bandwidth applications.

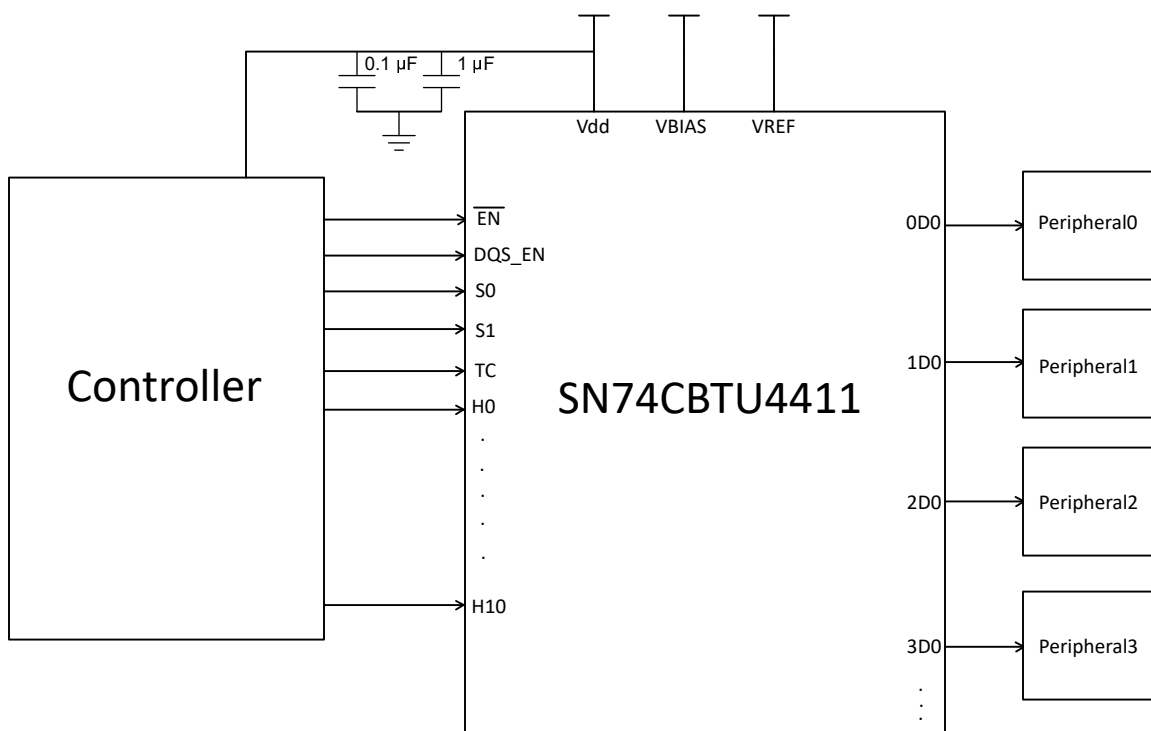


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

SN74CBTU4411 supports 400-MHz bandwidth on the D or H ports and 84 MHz on the S port. The Enable control from the controller must be activated and depending on the select pins, the data is transferred into one of the peripherals 0 to 3. The Enable control at high will tristate the input or output as per the functional table. See [节 6.3](#) and [节 6.1](#) for other voltage, current and handling parameters.

9.2.2 Detailed Design Procedure

The H port signal from the controller can go to one of the 4 peripheral ports depending on the select inputs S0 and S1. The V_{BIAS} and V_{REF} can be determined from 节 6.3.

1. Recommended Input Conditions

- For specified high and low levels for all the input control pins, see V_{IH} and V_{IL} in 节 6.3.
- Inputs are not overvoltage tolerant and should be below the valid V_{DD} .

2. Recommend Input/Output Conditions

- The absolute maximum continuous on state switch current for any I/O should not exceed ± 100 mA.
- The I/O voltage range should not be above V_{DD} and below ground.

9.2.3 Application Curve

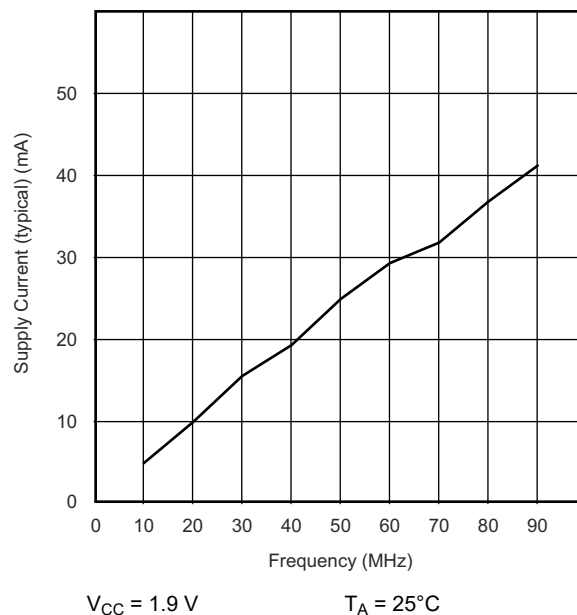


图 9-2. Supply Current (Typical) vs Frequency Data

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in 节 6.3.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a $0.1\text{-}\mu\text{F}$ capacitor. If there are multiple V_{CC} pins, TI recommends a $0.01\text{-}\mu\text{F}$ or $0.022\text{-}\mu\text{F}$ capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A $0.1\text{-}\mu\text{F}$ and $1\text{-}\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

图 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os, so they also cannot float when disabled.

11.2 Layout Example

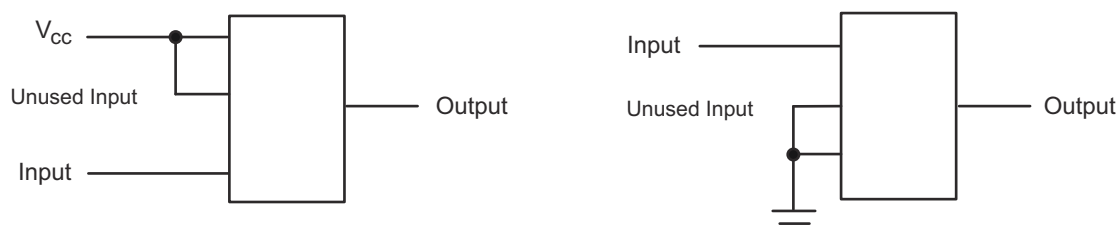


图 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)

12.2 接收文档更新通知

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12.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.4 Trademarks

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13 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBTU4411ZSTR	Active	Production	NFBGA (ZST) 72	2000 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	CTU4411
SN74CBTU4411ZSTR.A	Active	Production	NFBGA (ZST) 72	2000 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	CTU4411

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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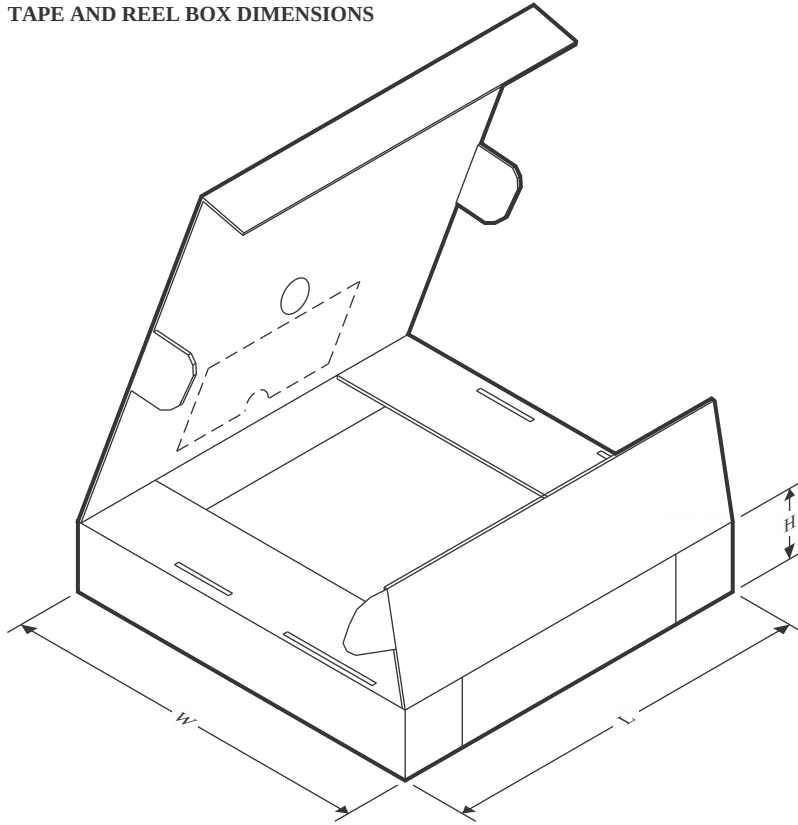
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

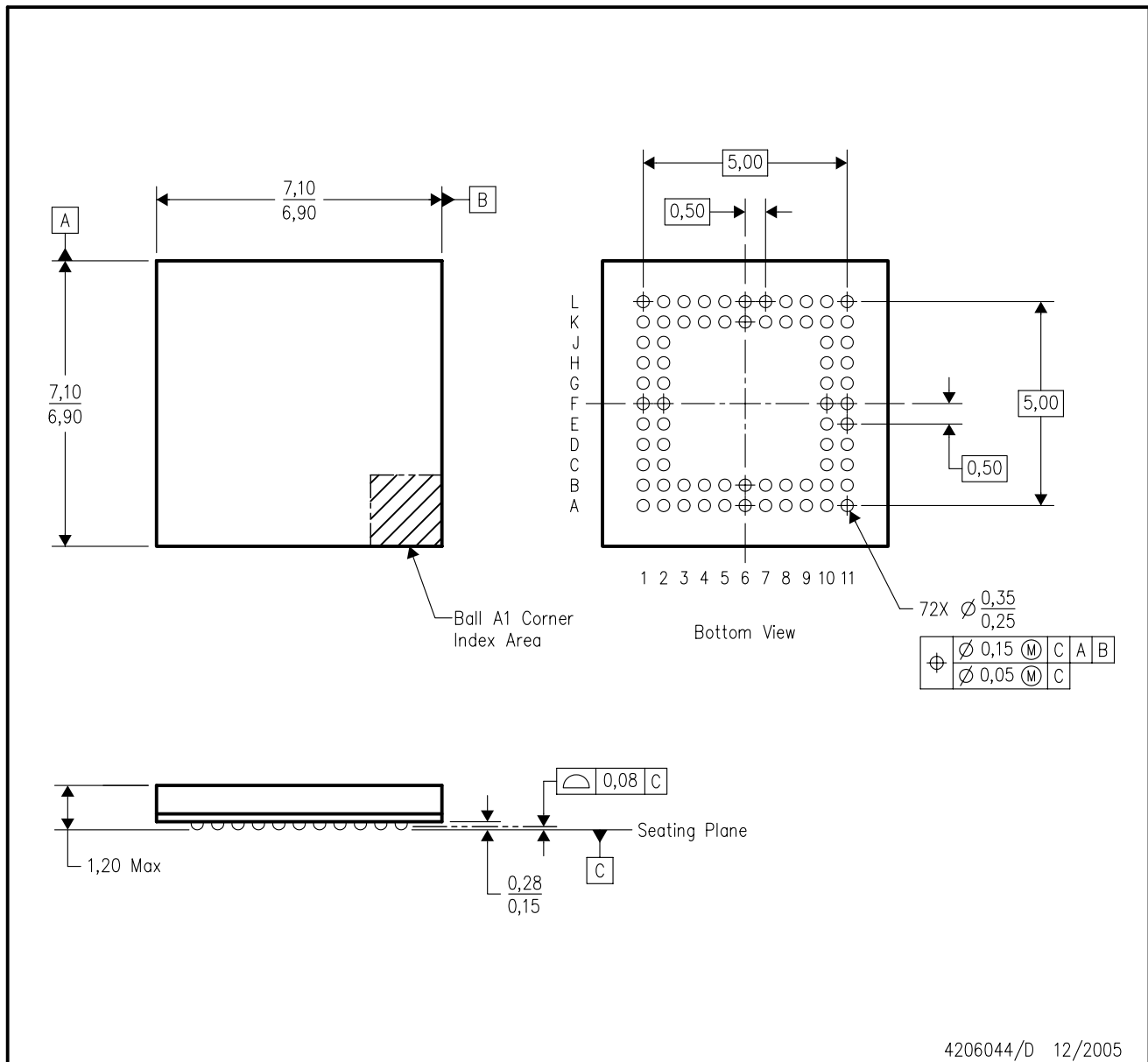


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	336.6	336.6	31.8

ZST (S-PBGA-N72)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Complies to JEDEC MO-195 variation AD (depopulated).
 - D. This package is lead-free. Refer to the 72 GST package (drawing 4206043) for tin-lead (SnPb).

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