

SN74CBTLV3384

LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS059G – MARCH 1998 – REVISED JUNE 2004

- 5- Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

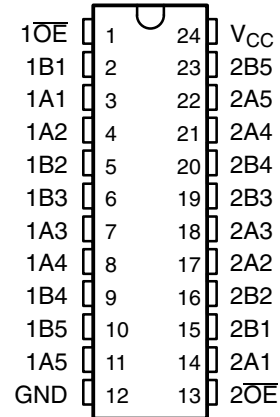
The SN74CBTLV3384 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 5-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 5-bit bus switches or one 10-bit bus switch. When \overline{OE} is low, the associated 5-bit bus switch is on, and A port is connected to B port. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3384DBQR	CBTLV3384
	SOIC – DW	Tube	SN74CBTLV3384DW	CBTLV3384
		Tape and reel	SN74CBTLV3384DWR	
	TSSOP – PW	Tape and reel	SN74CBTLV3384PWR	CL384
	TVSOP – DGV	Tape and reel	SN74CBTLV3384DGVR	CL384

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
1 \overline{OE}	2 \overline{OE}	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

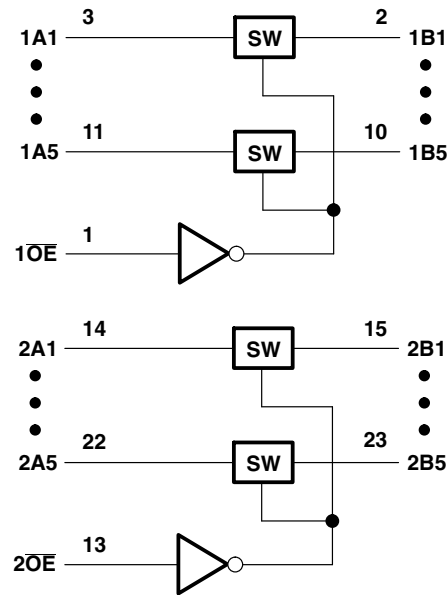
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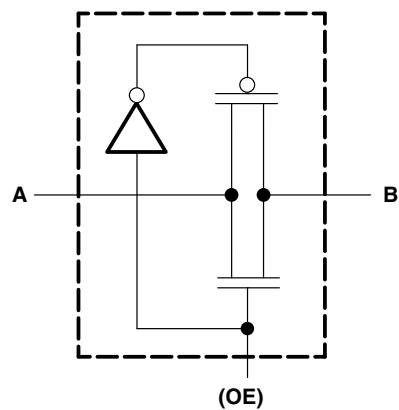
SN74CBTLV3384 LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS059G – MARCH 1998 – REVISED JUNE 2004

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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LOW-VOLTAGE 10-BIT FET BUS SWITCH

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	0.7	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	0.8	
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V
I_I		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND				±1	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V				10	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND				10	μA
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V, Other inputs at V_{CC} or GND				300	μA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0				4.5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V}$ or 0, $\overline{OE} = V_{CC}$				10	pF
r_{on}^\S	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			5	Ω
			$I_I = 24\text{ mA}$			5	
		$V_I = 1.7\text{ V}$	$I_I = 15\text{ mA}$			27	
						40	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			5	
			$I_I = 24\text{ mA}$			5	
		$V_I = 2.4\text{ V}$	$I_I = 15\text{ mA}$			10	
						15	

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^{\parallel}	A or B	B or A		0.15		0.25	ns
t_{en}	\overline{OE}	A or B	1	5	1	4.3	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1	5.5	ns

^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

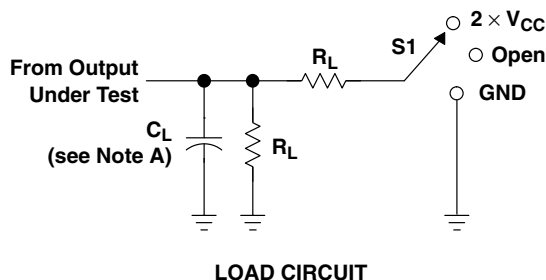


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LOW-VOLTAGE 10-BIT FET BUS SWITCH

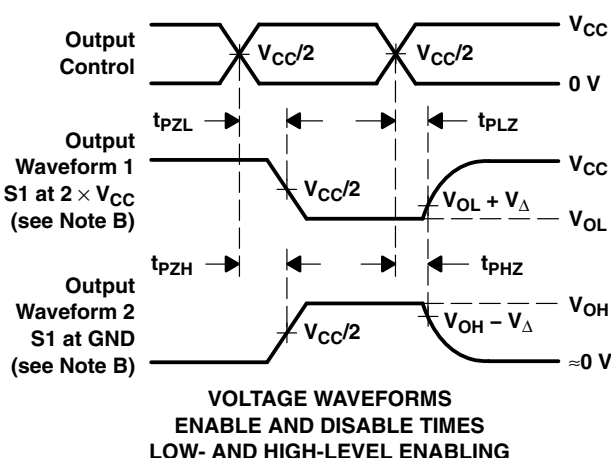
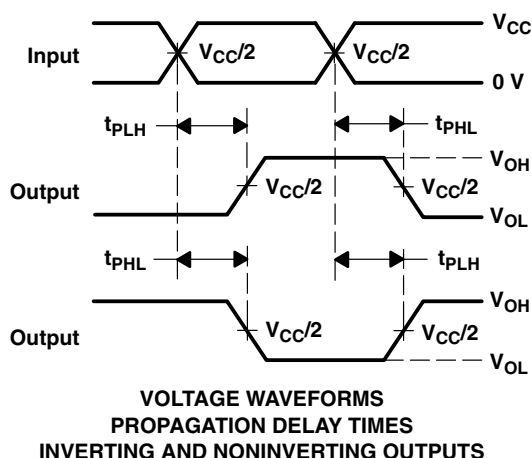
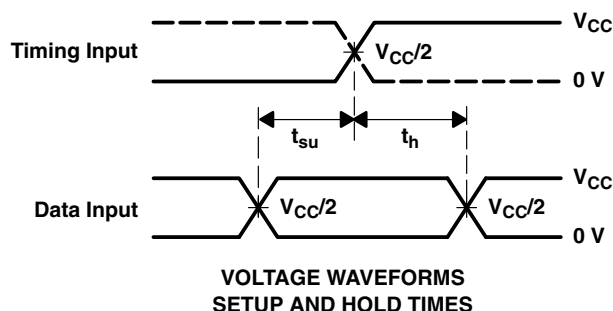
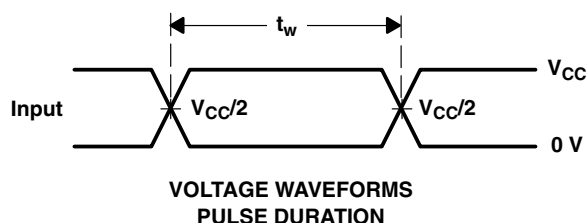
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBTLV3384DBQRG4	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3384
74CBTLV3384DBQRG4.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3384
SN74CBTLV3384DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3384
SN74CBTLV3384DBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3384
SN74CBTLV3384DGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384DGVR.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3384
SN74CBTLV3384DW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3384
SN74CBTLV3384DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3384
SN74CBTLV3384DWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3384
SN74CBTLV3384PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384PWRG4	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384
SN74CBTLV3384PWRG4.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL384

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3384DBQRG4	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3384DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3384DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3384DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3384DBQRG4	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CBTLV3384DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CBTLV3384DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74CBTLV3384DWR	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE

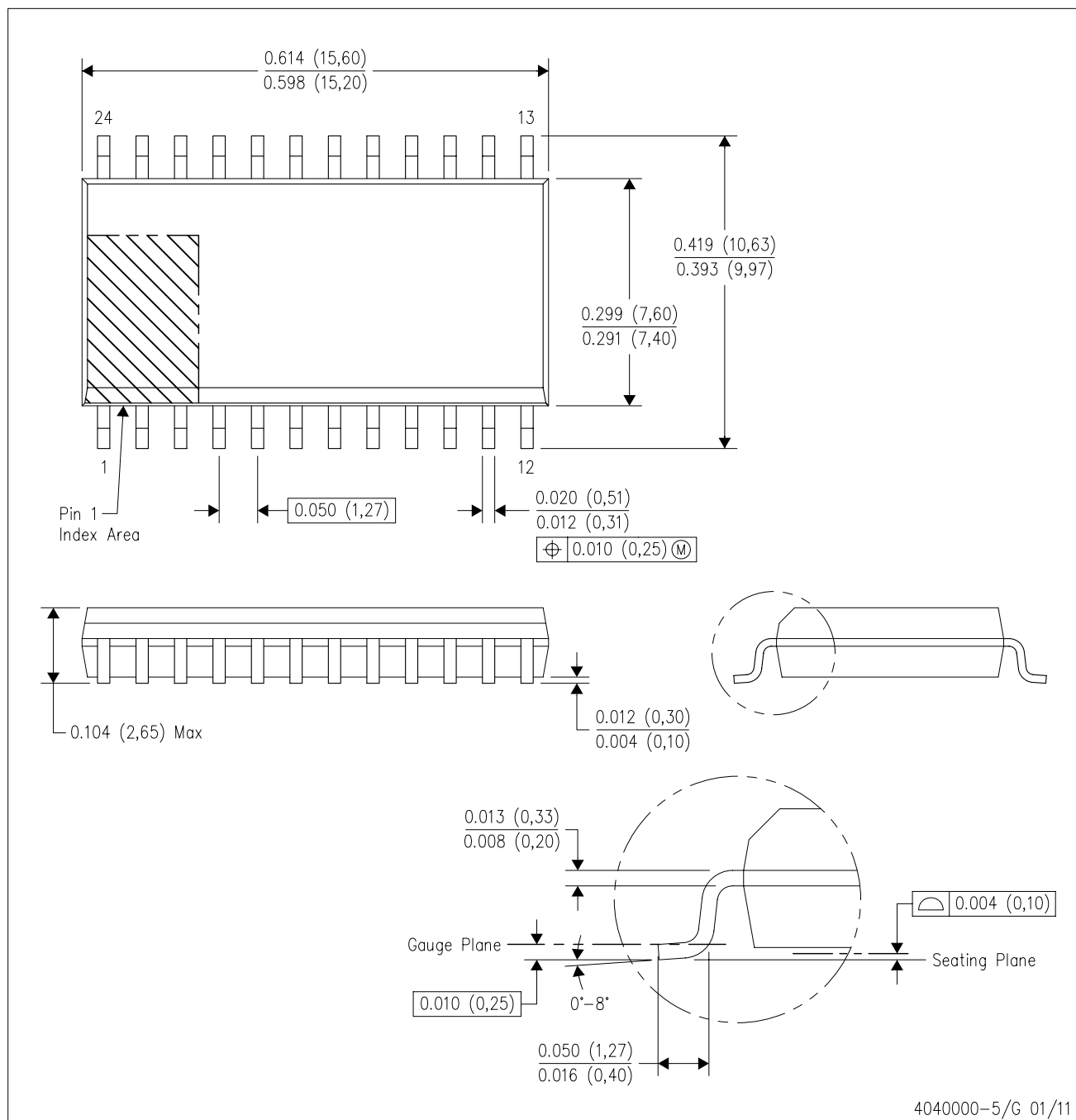


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBTLV3384DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTLV3384DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTLV3384PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBTLV3384PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.



TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



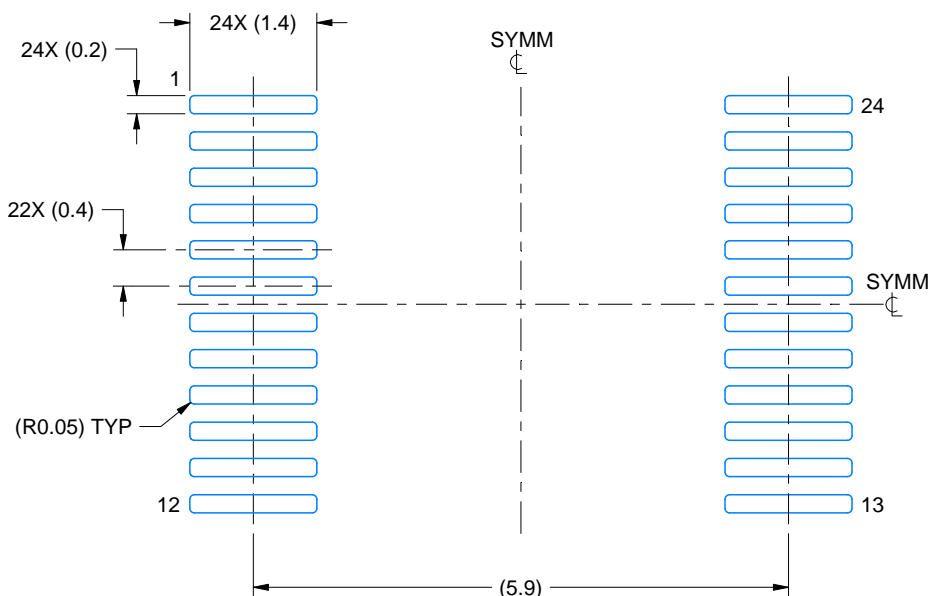
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

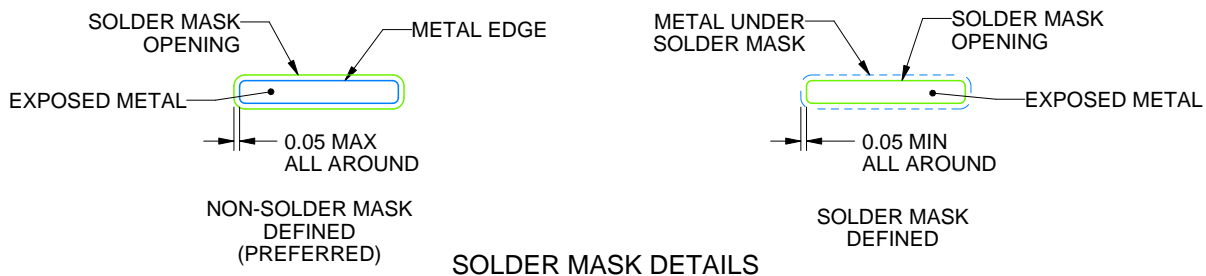
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

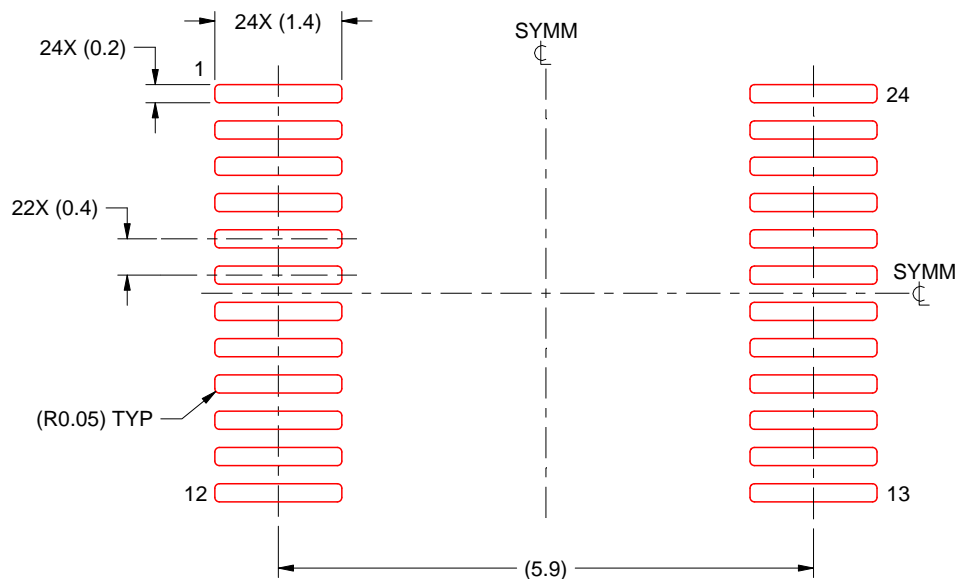
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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