

## SN74CBTLV3126 低电压四通道 FET 总线开关

### 1 特性

- 标准 126 型引脚
- 两个端口间使用  $5\Omega$  开关连接
- 支持在数据 I/O 端口进行轨到轨开关
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

### 2 应用

- 数据中心和企业计算
- 宽带固定线路接入
- 楼宇自动化
- 有线网络
- 电机驱动器

### 3 说明

SN74CBTLV3126 四通道 FET 总线开关具有独立的线路开关。当每个开关的相关输出使能 (OE) 输入为低电平时，开关被禁用。

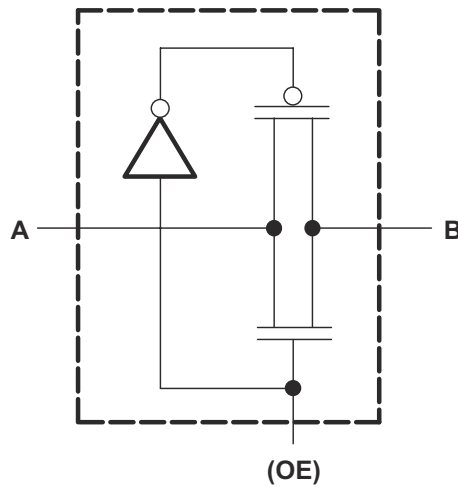
该器件专用于使用  $I_{off}$  的局部断电应用。 $I_{off}$  特性确保在关断时防止损坏电流通过器件回流。SN74CBTLV3126 器件可在电源关断时提供隔离。

为确保在上电或掉电期间均处于高阻抗状态，应将 OE 通过下拉电阻器接地；该电阻器的最小值取决于驱动器的灌电流能力。

#### 封装信息<sup>(1)</sup>

| 器件型号          | 封装                 | 封装尺寸 (标称值)      |
|---------------|--------------------|-----------------|
| SN74CBTLV3126 | SOIC ( D , 14 )    | 8.65mm × 3.91mm |
|               | TVSOP ( DGV , 14 ) | 3.60mm × 4.40mm |
|               | TSSOP ( PW , 14 )  | 5.00mm × 4.40mm |
|               | VQFN ( RGY , 14 )  | 4.00mm × 3.50mm |
|               | SSOP ( DBQ , 16 )  | 4.90mm × 3.90mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



每个 FET 开关的简化版原理图



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

|                                                                                                                                                   |             |
|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision K (June 2021) to Revision L (August 2022)</b> .....                                                                      | <b>Page</b> |
| • Updated the <i>Overview</i> section.....                                                                                                        | <b>8</b>    |
| <b>Changes from Revision J (January 2019) to Revision K (June 2021)</b> .....                                                                     | <b>Page</b> |
| • 更新了整个文档中的表格、图和交叉引用的编号格式.....                                                                                                                    | <b>1</b>    |
| • Changed <i>active low</i> to <i>active high</i> in the <i>Pin Configurations and Functions</i> section to reflect logic description change..... | <b>3</b>    |
| <b>Changes from Revision I (October 2003) to Revision J (January 2019)</b> .....                                                                  | <b>Page</b> |
| • 添加了器件信息表、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。.....                                                             | <b>1</b>    |
| • Added $V_{IH}$ MAX values in the <i>Recommended Operating Conditions</i> table.....                                                             | <b>5</b>    |

## 5 Pin Configuration and Functions

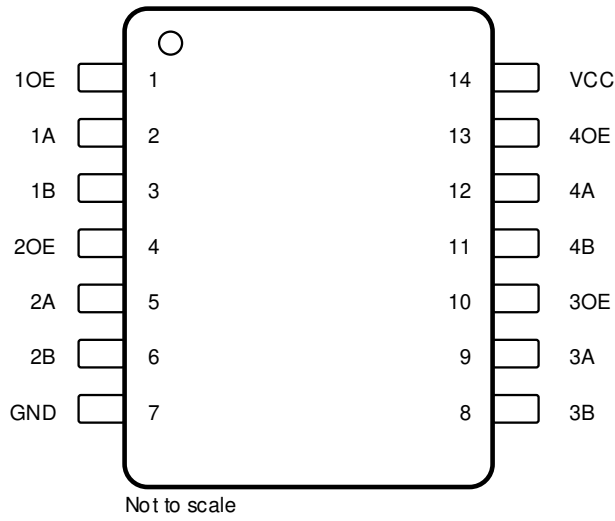


图 5-1. D, DGV, and PW Package, 14 Pin SOIC, TVSOP, and TSSOP (Top View)

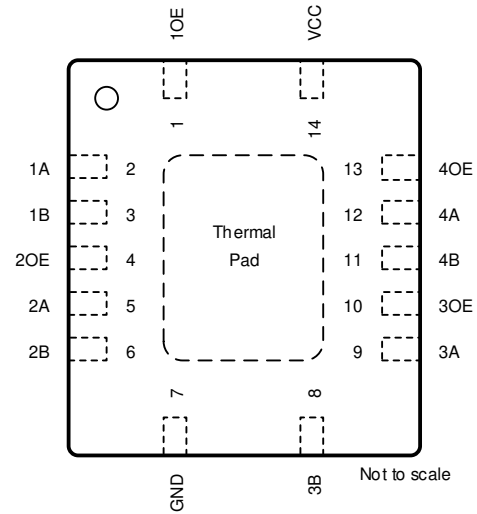


图 5-2. RGY Package, 14 Pin VQFN (Top View)

表 5-1. Pin Functions, D, DGV, PW, RGY

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                               |
|-----------------|-----|---------------------|---------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |                     |                                                                                                                           |
| 1A              | 2   | I/O                 | Channel 1 input or output                                                                                                 |
| 1B              | 3   | I/O                 | Channel 1 input or output                                                                                                 |
| 10E             | 1   | I                   | Output enable, active high                                                                                                |
| 2A              | 5   | I/O                 | Channel 2 input or output                                                                                                 |
| 2B              | 6   | I/O                 | Channel 2 input or output                                                                                                 |
| 2OE             | 4   | I                   | Output enable, active high                                                                                                |
| 3A              | 9   | I/O                 | Channel 3 input or output                                                                                                 |
| 3B              | 8   | I/O                 | Channel 3 input or output                                                                                                 |
| 3OE             | 10  | I                   | Output enable, active high                                                                                                |
| 4A              | 12  | I/O                 | Channel 4 input or output                                                                                                 |
| 4B              | 11  | I/O                 | Channel 4 input or output                                                                                                 |
| 4OE             | 13  | I                   | Output enable, active high                                                                                                |
| GND             | 7   | —                   | Ground                                                                                                                    |
| V <sub>CC</sub> | 14  | P                   | Power supply                                                                                                              |
| Thermal Pad     |     | —                   | Exposed thermal pad. There is no requirement to solder this pad; if connected, it should be left floating or tied to GND. |

(1) I = input, O = output, I/O = input and output, P = power

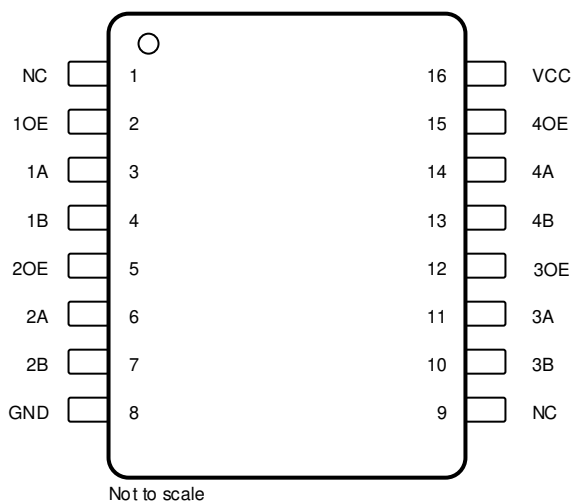


图 5-3. DBQ Package, 16 Pin SSOP (Top View)

表 5-2. Pin Functions, DBQ

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                |
|-----------------|-----|---------------------|----------------------------|
| NAME            | NO. |                     |                            |
| 1A              | 3   | I/O                 | Channel 1 input or output  |
| 1B              | 4   | I/O                 | Channel 1 input or output  |
| 1OE             | 2   | I                   | Output enable, active high |
| 2A              | 6   | I/O                 | Channel 2 input or output  |
| 2B              | 7   | I/O                 | Channel 2 input or output  |
| 2OE             | 5   | I                   | Output enable, active high |
| 3A              | 11  | I/O                 | Channel 3 input or output  |
| 3B              | 10  | I/O                 | Channel 3 input or output  |
| 3OE             | 12  | I                   | Output enable, active high |
| 4A              | 14  | I/O                 | Channel 4 input or output  |
| 4B              | 13  | I/O                 | Channel 4 input or output  |
| 4OE             | 15  | I                   | Output enable, active high |
| GND             | 8   | —                   | Ground                     |
| NC              | 9   | —                   | No internal connection     |
| V <sub>CC</sub> | 16  | P                   | Power supply               |

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                    |                      | MIN   | MAX  | UNIT |
|------------------|------------------------------------|----------------------|-------|------|------|
| V <sub>CC</sub>  | Supply voltage range               |                      | – 0.5 | 4.6  | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup> |                      | – 0.5 | 4.6  | V    |
| I <sub>I/O</sub> | Continuous channel current         |                      |       | 128  | mA   |
| I <sub>IK</sub>  | Input clamp current                | V <sub>I/O</sub> < 0 |       | – 50 | mA   |
| T <sub>stg</sub> | Storage temperature range          |                      | – 65  | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

<sup>(1)</sup>

|                 |                                  | MIN                              | MAX | UNIT            |
|-----------------|----------------------------------|----------------------------------|-----|-----------------|
| V <sub>CC</sub> | Supply voltage                   | 2.3                              | 3.6 | V               |
| V <sub>IH</sub> | High-level control input voltage | V <sub>CC</sub> = 2.3 V to 2.7 V | 1.7 | V <sub>CC</sub> |
|                 |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 2   | V <sub>CC</sub> |
| V <sub>IL</sub> | Low-level control input voltage  | V <sub>CC</sub> = 2.3 V to 2.7 V | 0.7 | V               |
|                 |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 0.8 | V               |
| T <sub>A</sub>  | Operating free-air temperature   | – 40                             | 85  | °C              |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74CBTLV3126 |             |            |            |            | UNIT |
|-------------------------------|----------------------------------------------|---------------|-------------|------------|------------|------------|------|
|                               |                                              | D (SOIC)      | DGV (TVSOP) | PW (TSSOP) | RGY (VQFN) | DBQ (SSOP) |      |
|                               |                                              | 14 PINS       | 14 PINS     | 14 PINS    | 14 PINS    | 16 Pins    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 100.6         | 154.8       | 123.3      | 59.6       | 118.7      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 55.5          | 64.5        | 53.0       | 71.3       | 66.4       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 56.8          | 88.4        | 66.3       | 35.6       | 62.2       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 17.0          | 11.1        | 9.3        | 4.2        | 20.9       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 56.4          | 87.4        | 65.7       | 35.7       | 61.7       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A           | N/A         | N/A        | 16.1       | N/A        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS                                             |                                                                | MIN                  | TYP <sup>(1)</sup> | MAX     | UNIT          |
|-----------------------------------------------|-------------------------------------------------------------|----------------------------------------------------------------|----------------------|--------------------|---------|---------------|
| $V_{IK}$                                      | $V_{CC} = 3\text{ V}$ ,                                     | $I_I = -18\text{ mA}$                                          |                      |                    | -1.2    | V             |
| $I_I$                                         | $V_{CC} = 3.6\text{ V}$ ,                                   | $V_I = V_{CC}$ or GND                                          |                      |                    | $\pm 1$ | $\mu\text{A}$ |
| $I_{off}$                                     | $V_{CC} = 0$ ,                                              | $V_I$ or $V_O = 0$ to $3.6\text{ V}$                           |                      |                    | 10      | $\mu\text{A}$ |
| $I_{CC}$                                      | $V_{CC} = 3.6\text{ V}$ ,                                   | $I_O = 0$ ,<br>$V_I = V_{CC}$ or GND                           |                      |                    | 10      | $\mu\text{A}$ |
| $\Delta I_{CC}$ <sup>(2)</sup> Control inputs | $V_{CC} = 3.6\text{ V}$ ,                                   | One input at $3\text{ V}$ ,<br>Other inputs at $V_{CC}$ or GND |                      |                    | 300     | $\mu\text{A}$ |
| $C_i$ Control inputs                          | $V_I = 3\text{ V}$ or $0$                                   |                                                                |                      | 2.5                |         | pF            |
| $C_{io(OFF)}$                                 | $V_O = 3\text{ V}$ or $0$ ,<br>OE = GND                     |                                                                |                      | 7                  |         | pF            |
| $r_{on}$ <sup>(3)</sup>                       | $V_{CC} = 2.5\text{ V}$ ,<br>TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$                                                      | $I_I = 64\text{ mA}$ | 5                  | 8       | $\Omega$      |
|                                               |                                                             |                                                                | $I_I = 24\text{ mA}$ | 5                  | 8       |               |
|                                               |                                                             | $V_I = 1.7\text{ V}$ ,                                         | $I_I = 15\text{ mA}$ | 27                 | 40      |               |
|                                               | $V_{CC} = 3\text{ V}$                                       | $V_I = 0$                                                      | $I_I = 64\text{ mA}$ | 5                  | 7       |               |
|                                               |                                                             |                                                                | $I_I = 24\text{ mA}$ | 5                  | 7       |               |
|                                               |                                                             | $V_I = 2.4\text{ V}$ ,                                         | $I_I = 15\text{ mA}$ | 10                 | 15      |               |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

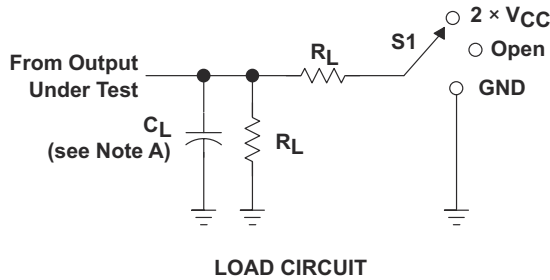
## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER               | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}$ |      | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |      | UNIT |
|-------------------------|-----------------|----------------|-----------------------------------------------|------|-----------------------------------------------|------|------|
|                         |                 |                | MIN                                           | MAX  | MIN                                           | MAX  |      |
| $t_{pd}$ <sup>(1)</sup> | A or B          | B or A         |                                               | 0.15 |                                               | 0.25 | ns   |
| $t_{en}$                | OE              | A or B         | 1.6                                           | 4.5  | 1.9                                           | 4.2  | ns   |
| $t_{dis}$               | OE              | A or B         | 1.3                                           | 4.7  | 1                                             | 4.8  | ns   |

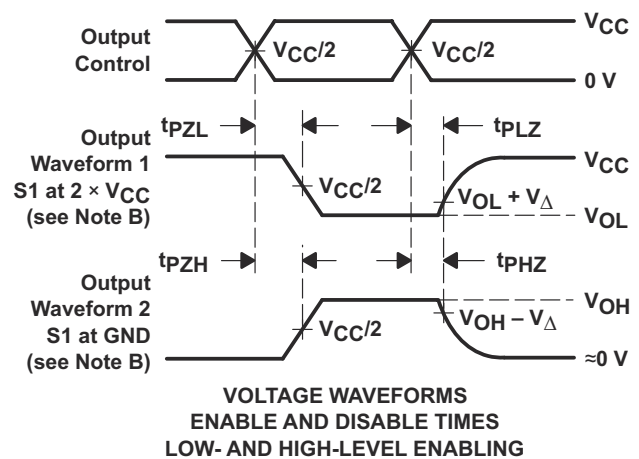
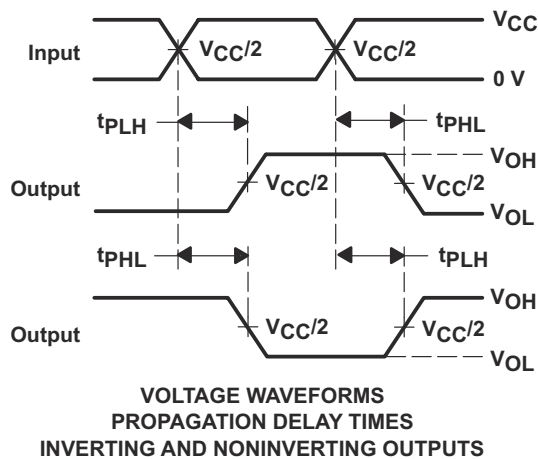
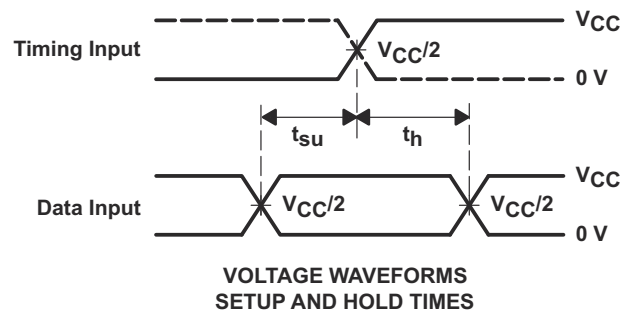
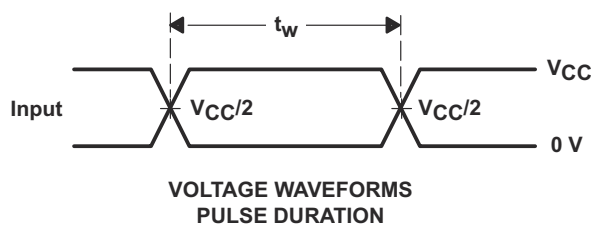
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 7 Parameter Measurement Information



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$                          | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-----------------------------------|-------|--------------|--------------|
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

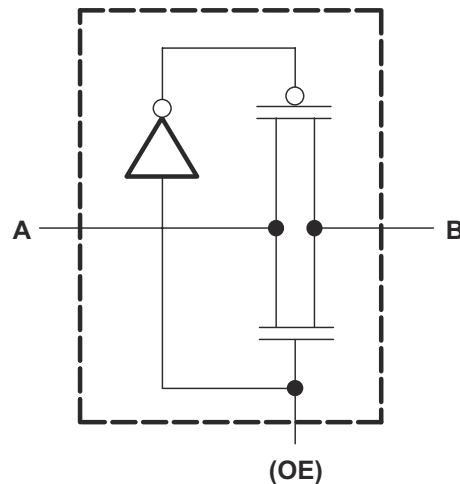
**图 7-1. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low. This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SN74CBTLV3126 features 5- $\Omega$  switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I<sub>off</sub> supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

### 8.4 Device Functional Modes

#### 8.4.1 Function Table (Each Bus Switch)

表 8-1 provides the truth table for the SN74CBTLV3126.

表 8-1. Truth Table

| INPUT<br>OE | FUNCTION        |
|-------------|-----------------|
| L           | Disconnect      |
| H           | A port = B port |



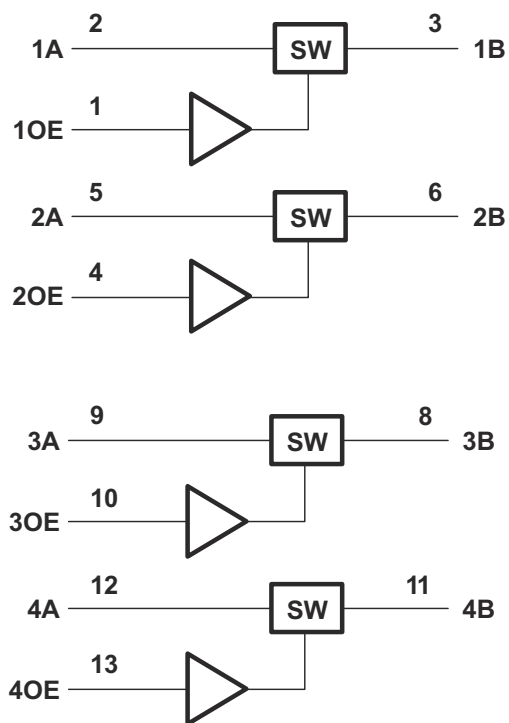


图 8-1. Logic Diagram (Positive Logic)

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

One useful application to take advantage of the SN74CBTLV3126 features is isolating various protocols from a processor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides excellent isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

### 9.2 Typical Application

#### 9.2.1 Protocol and Signal Isolation

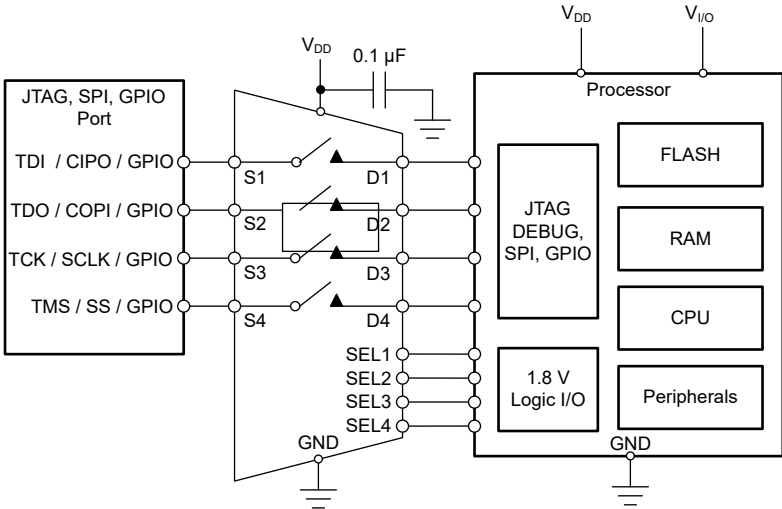


图 9-1. Typical Application

#### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

| PARAMETERS                   | VALUES           |
|------------------------------|------------------|
| Supply ( $V_{DD}$ )          | 3.3 V            |
| Input or output signal range | 0 V to 3.3 V     |
| Control logic thresholds     | 1.8 V compatible |

### 9.2.1.2 Detailed Design Procedure

The SN74CBTLV3126 can operate without any external components except for the supply decoupling capacitors. TI recommends that the digital control pins (OE) be pulled up to  $V_{CC}$  or down to GND to avoid an undesired switch state that could result from the floating pin. All input signals passing through the switch must fall within the *Recommend Operating Conditions* of the SN74CBTLV3126 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature, and the inputs can range from 0 V to 3.3 V when  $V_{DD} = 0$  V.

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

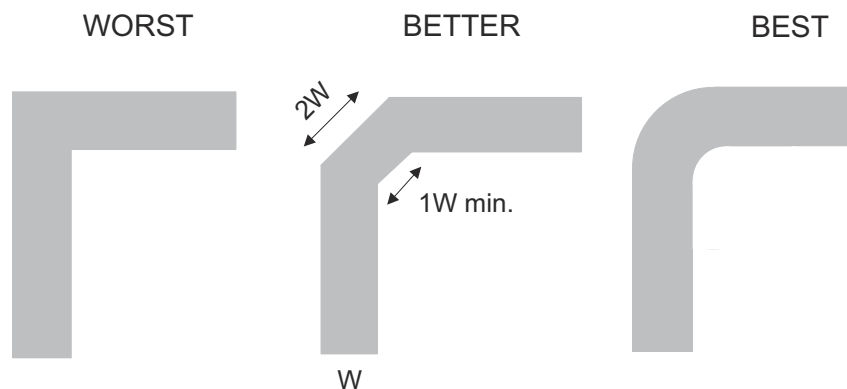


图 11-1. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

- Avoid stubs on the high-speed signals traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.

- When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 11-2.

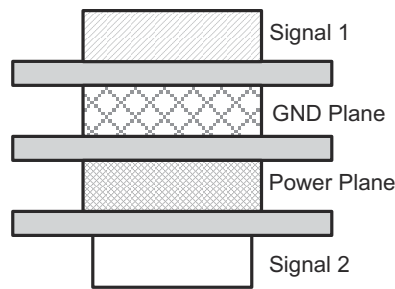


图 11-2. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

图 11-3 shows an example of a PCB layout with the SN74CBTLV3126. Some key considerations are:

Decouple the  $V_{DD}$  pin with a 0.1- $\mu$ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the  $V_{DD}$  supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 11.2 Layout Example

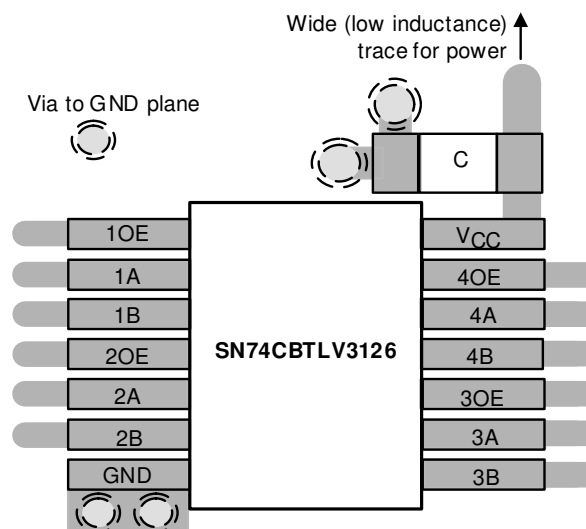


图 11-3. Example Layout

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

**TI 术语表**      本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74CBTLV3126DBQRG4                 | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| 74CBTLV3126DBQRG4.A               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| 74CBTLV3126DBQRG4.B               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| 74CBTLV3126DGVRG4                 | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| 74CBTLV3126DGVRG4.B               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| <a href="#">SN74CBTLV3126D</a>    | Obsolete      | Production           | SOIC (D)   14    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | CBTLV3126           |
| <a href="#">SN74CBTLV3126DBQR</a> | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| SN74CBTLV3126DBQR.A               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| SN74CBTLV3126DBQR.B               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| <a href="#">SN74CBTLV3126DGVR</a> | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126DGVR.B               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| <a href="#">SN74CBTLV3126DR</a>   | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTLV3126           |
| SN74CBTLV3126DR.A                 | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTLV3126           |
| SN74CBTLV3126DR.B                 | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTLV3126           |
| <a href="#">SN74CBTLV3126PW</a>   | Obsolete      | Production           | TSSOP (PW)   14  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | CL126               |
| <a href="#">SN74CBTLV3126PWR</a>  | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126PWR.A                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126PWR.B                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126PWRG4                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126PWRG4.A              | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| SN74CBTLV3126PWRG4.B              | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CL126               |
| <a href="#">SN74CBTLV3126RGYR</a> | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| SN74CBTLV3126RGYR.A               | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |
| SN74CBTLV3126RGYR.B               | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CL126               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

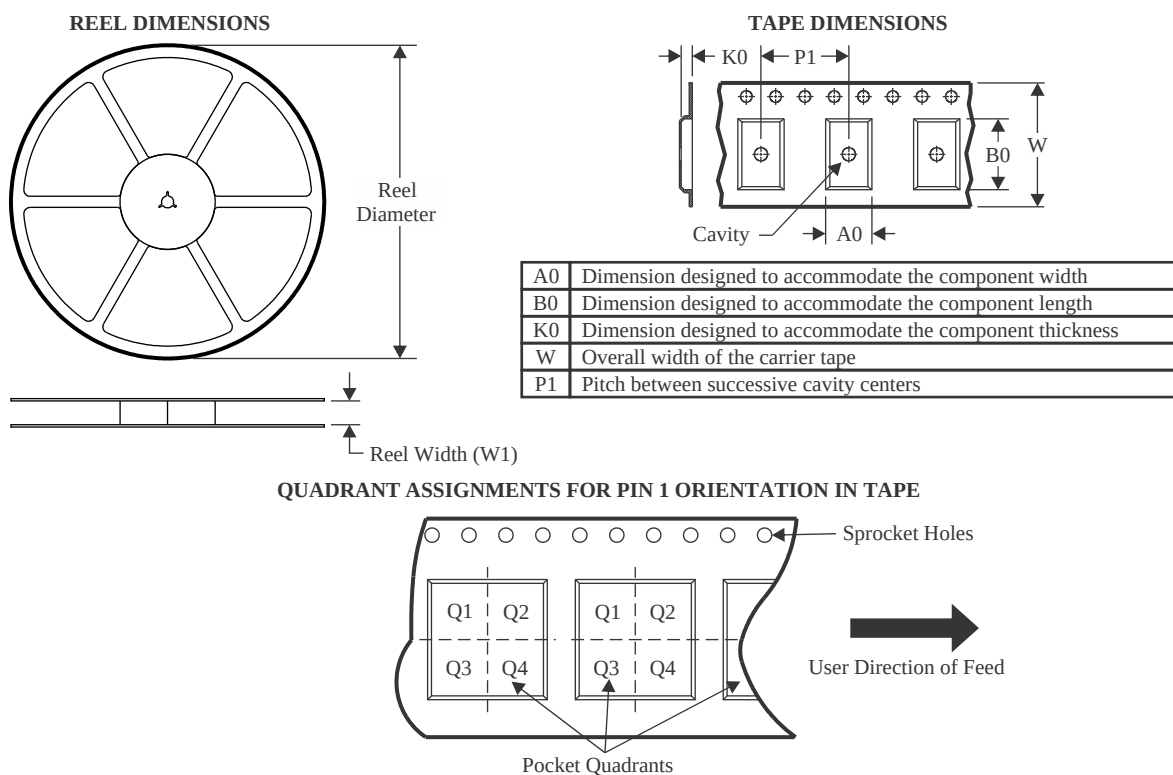
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

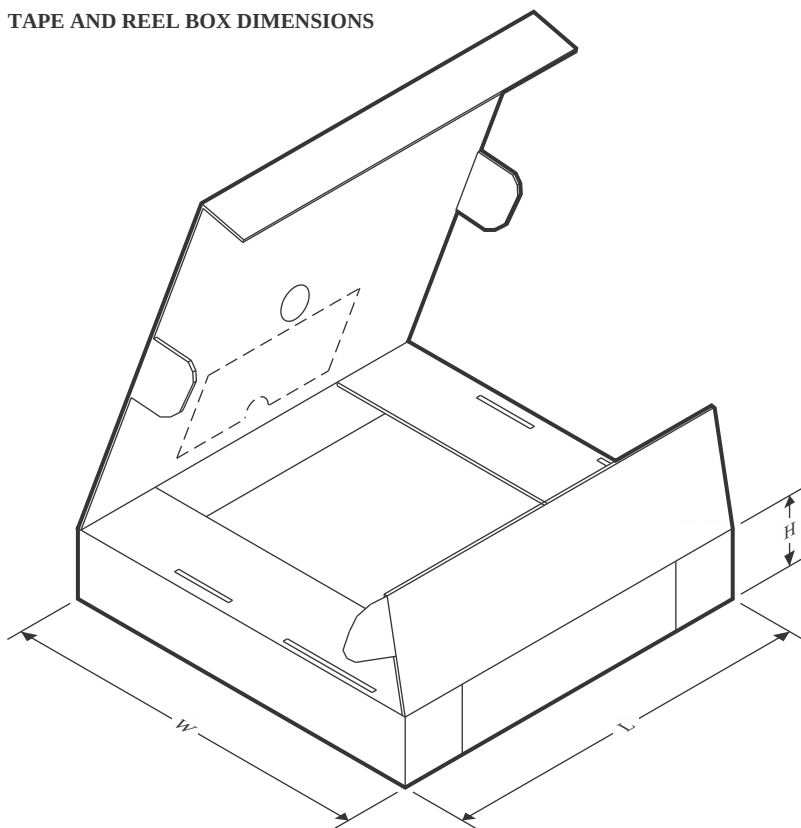


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74CBTLV3126DBQRG4  | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.5               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| 74CBTLV3126DGVRG4  | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126DBQR  | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.5               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126DGVR  | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126DR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3126PWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126PWRG4 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126RGYR  | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

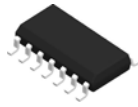


## TAPE AND REEL BOX DIMENSIONS

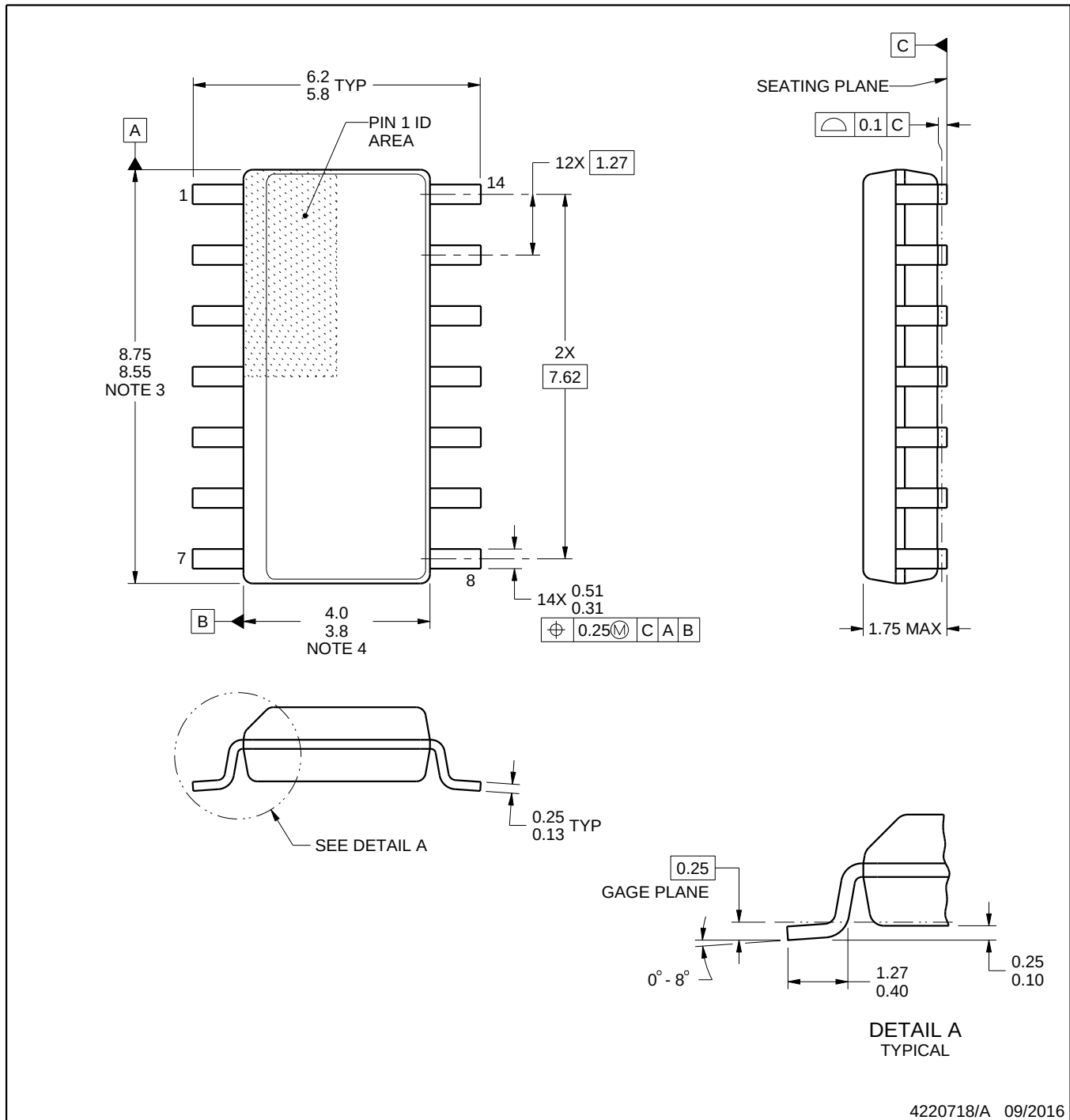


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74CBTLV3126DBQRG4  | SSOP         | DBQ             | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| 74CBTLV3126DGVRG4  | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBTLV3126DBQR  | SSOP         | DBQ             | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CBTLV3126DGVR  | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBTLV3126DR    | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CBTLV3126PWR   | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3126PWRG4 | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBTLV3126RGYR  | VQFN         | RGY             | 14   | 3000 | 353.0       | 353.0      | 32.0        |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

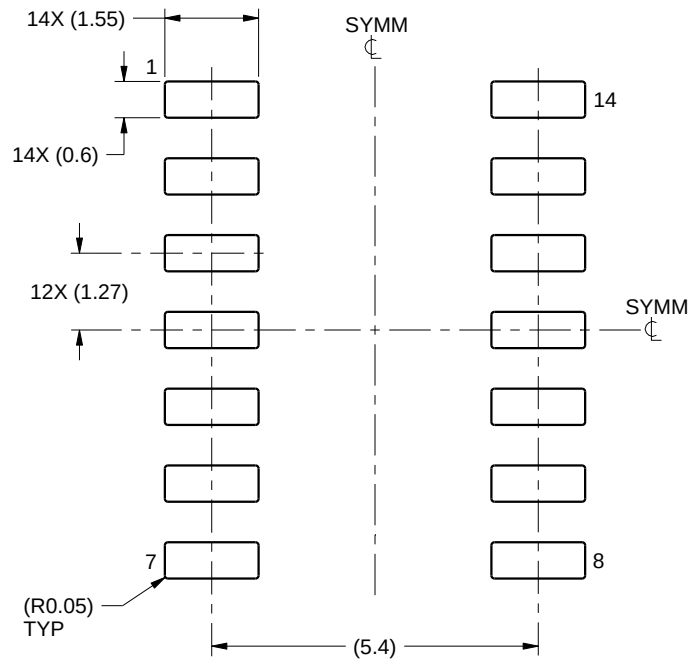


# EXAMPLE BOARD LAYOUT

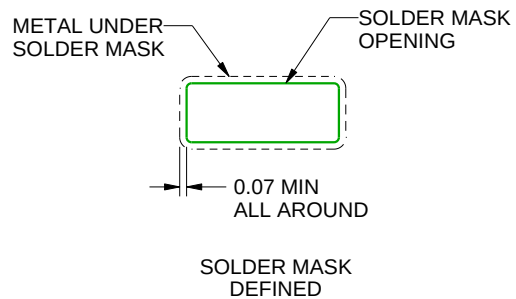
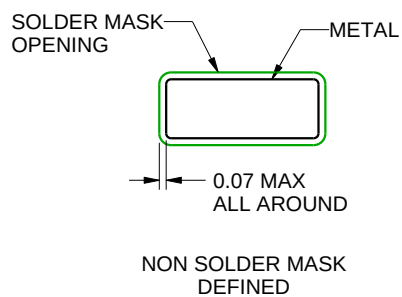
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

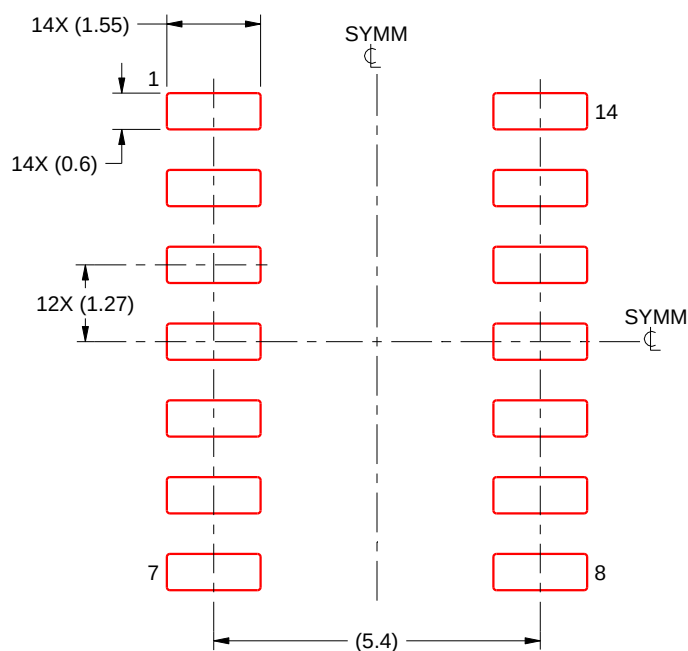
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

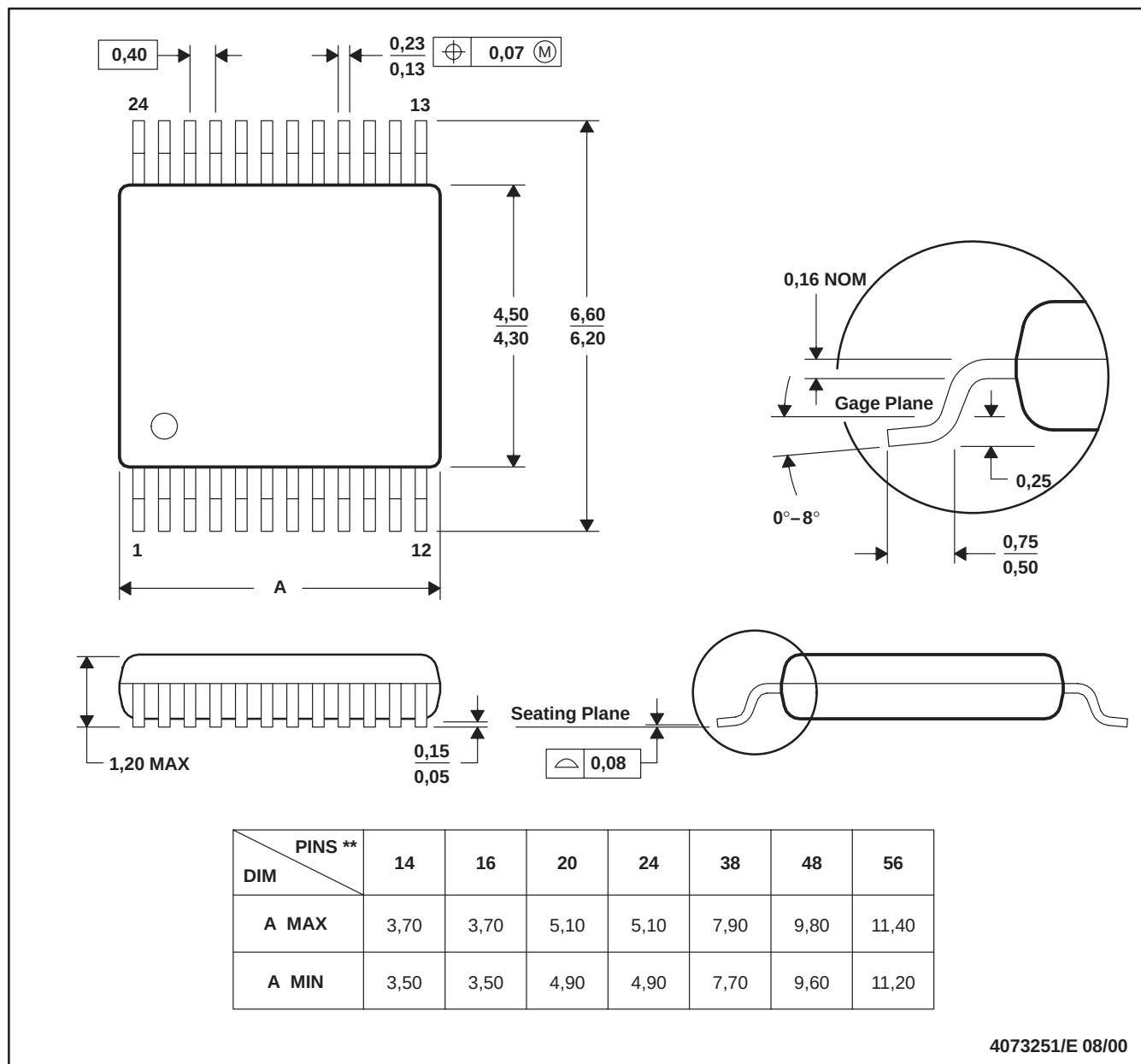
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

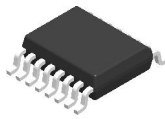
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

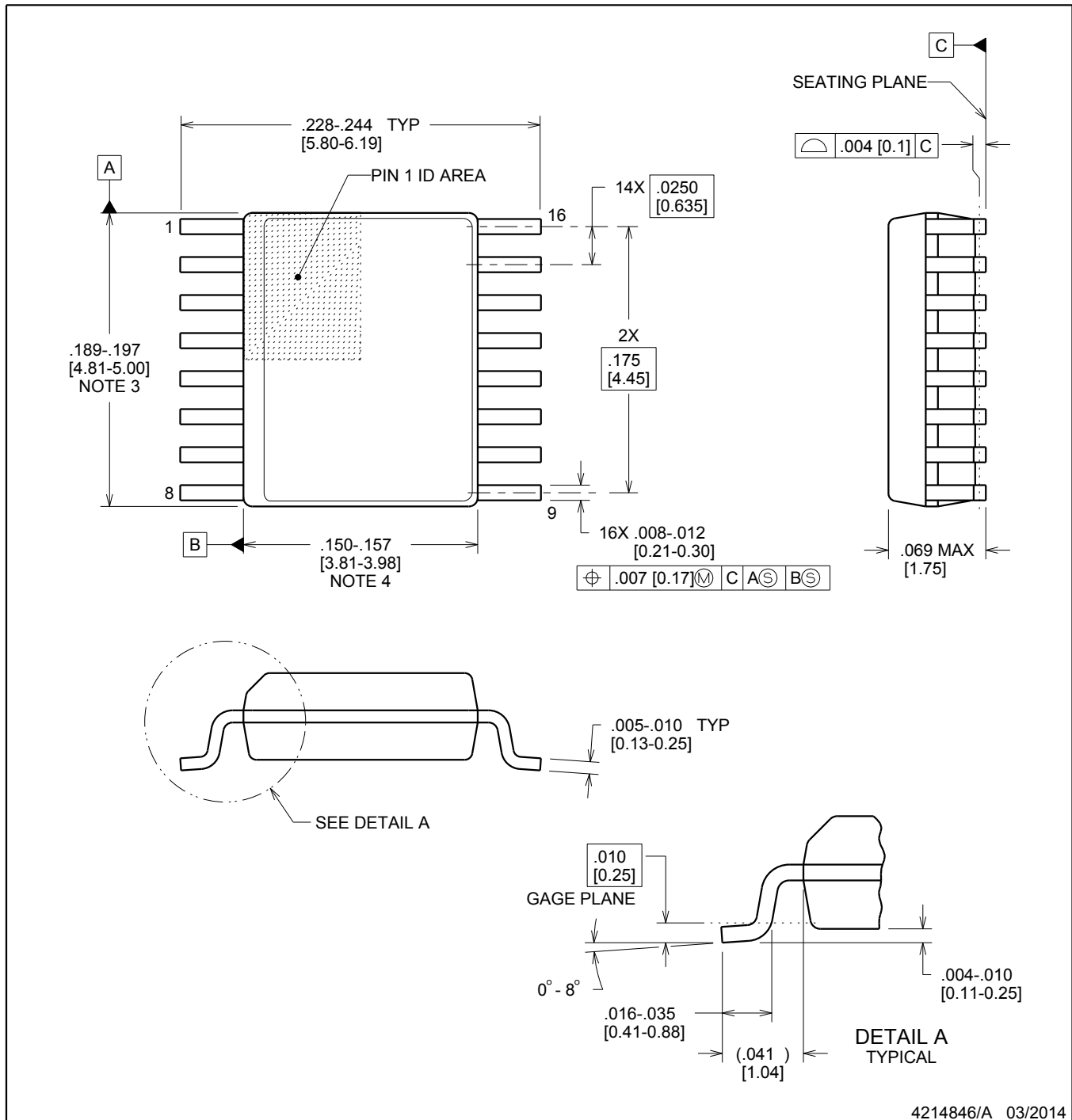


**DBQ0016A**

# PACKAGE OUTLINE

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



## NOTES:

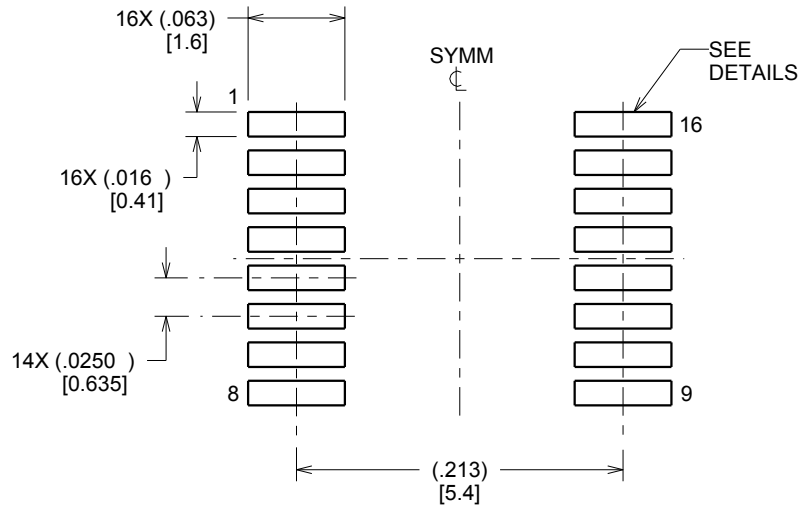
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

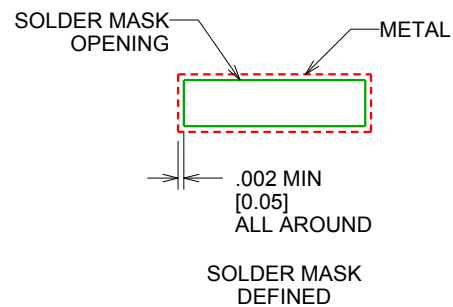
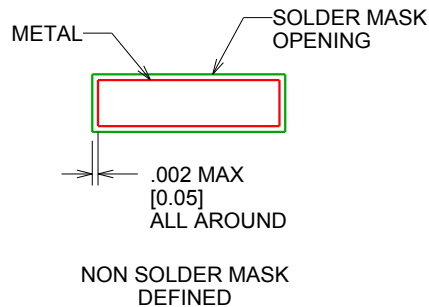
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

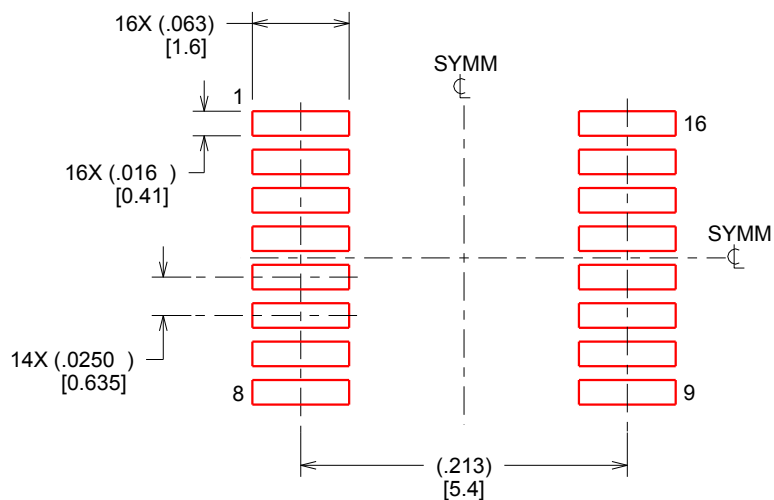
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

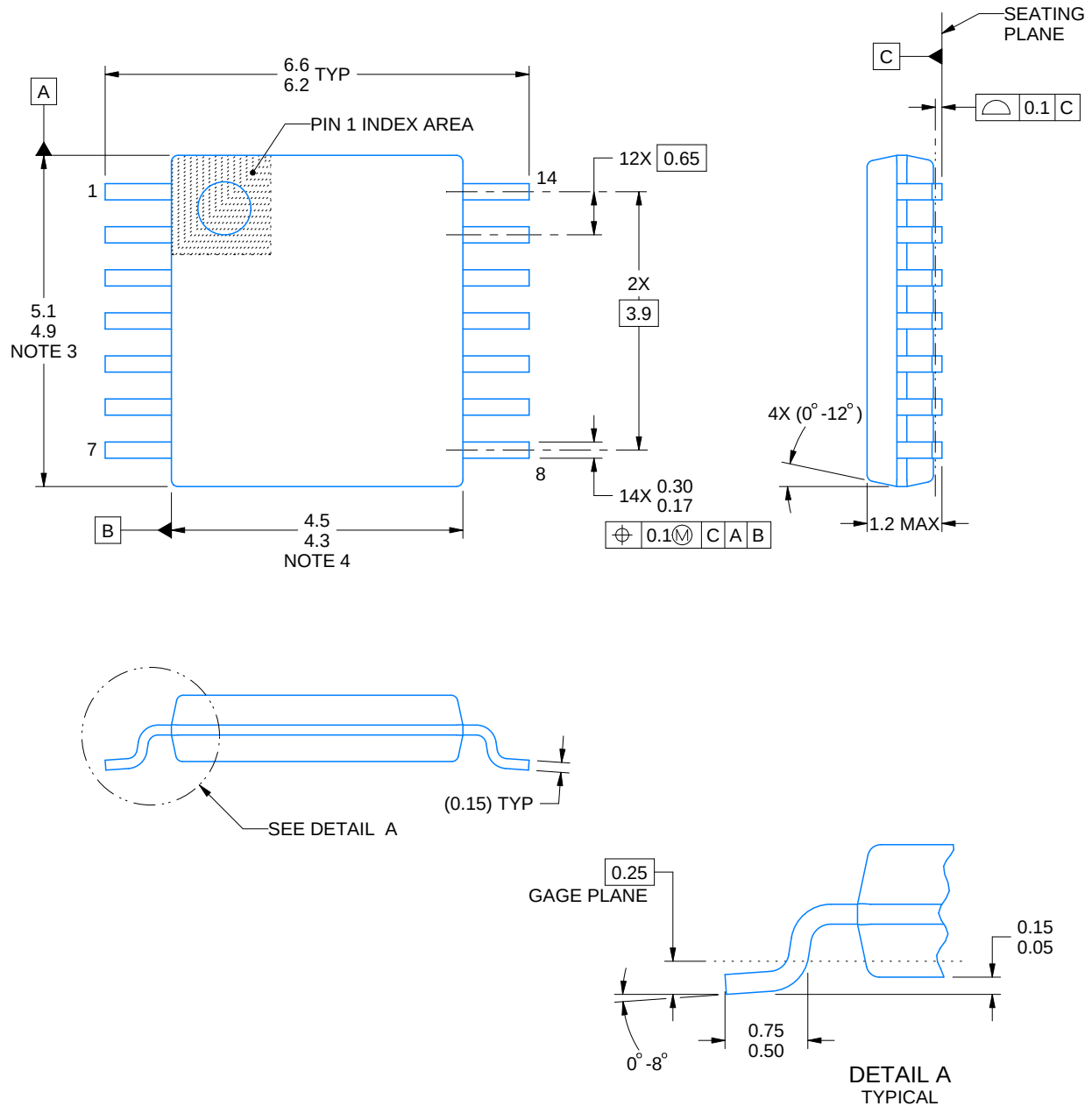


**PW0014A**

## PACKAGE OUTLINE

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

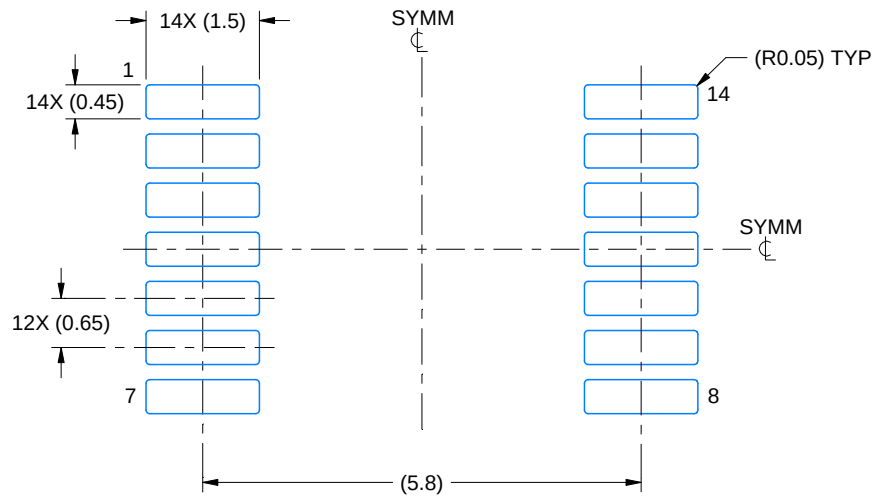
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

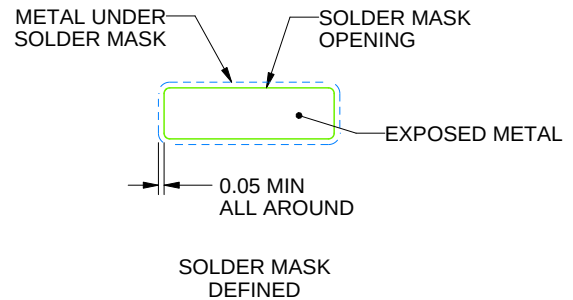
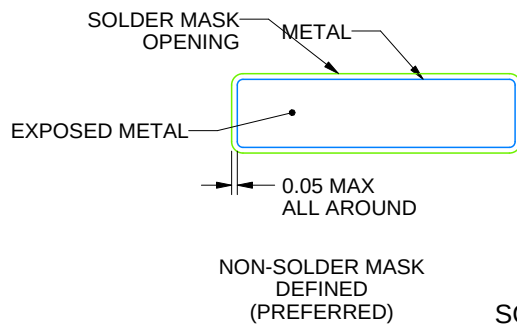
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

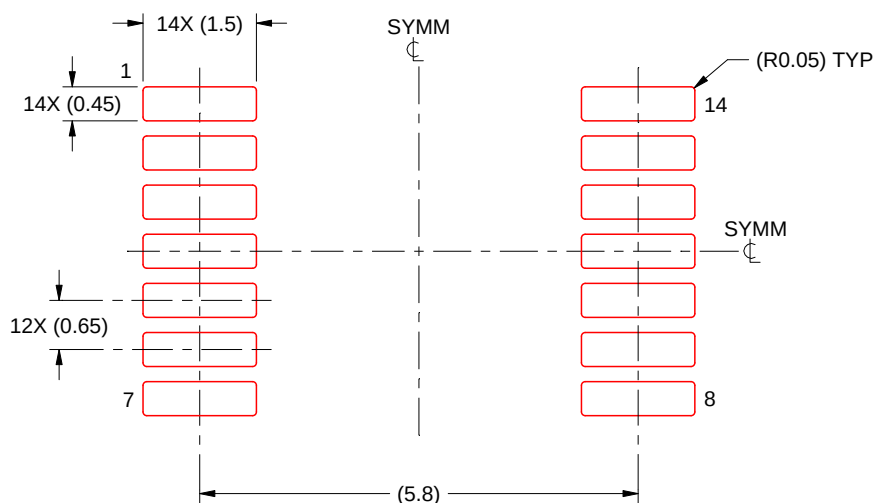
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

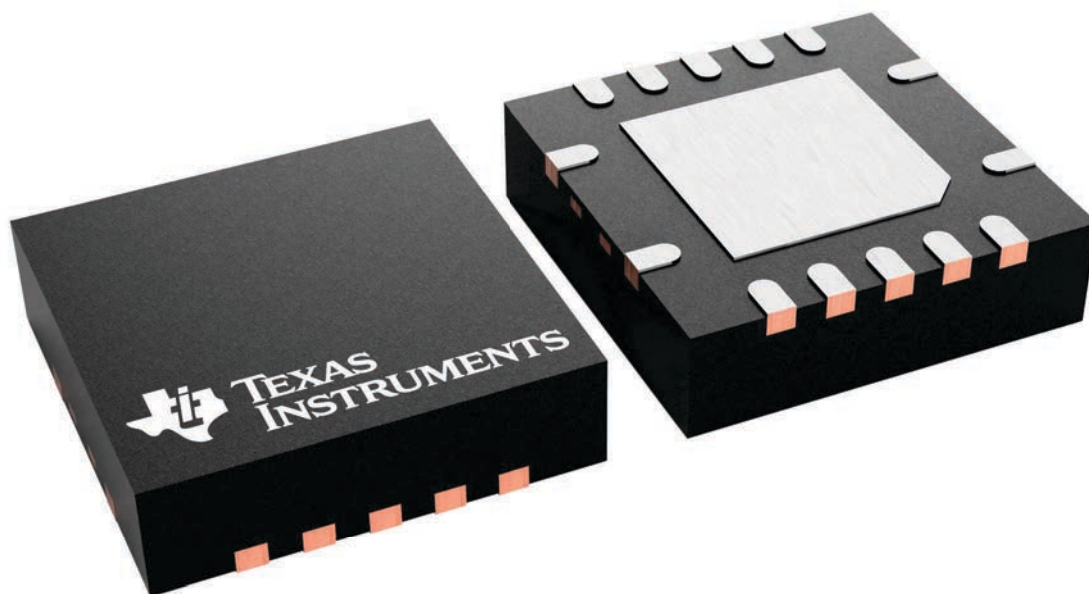
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A



### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



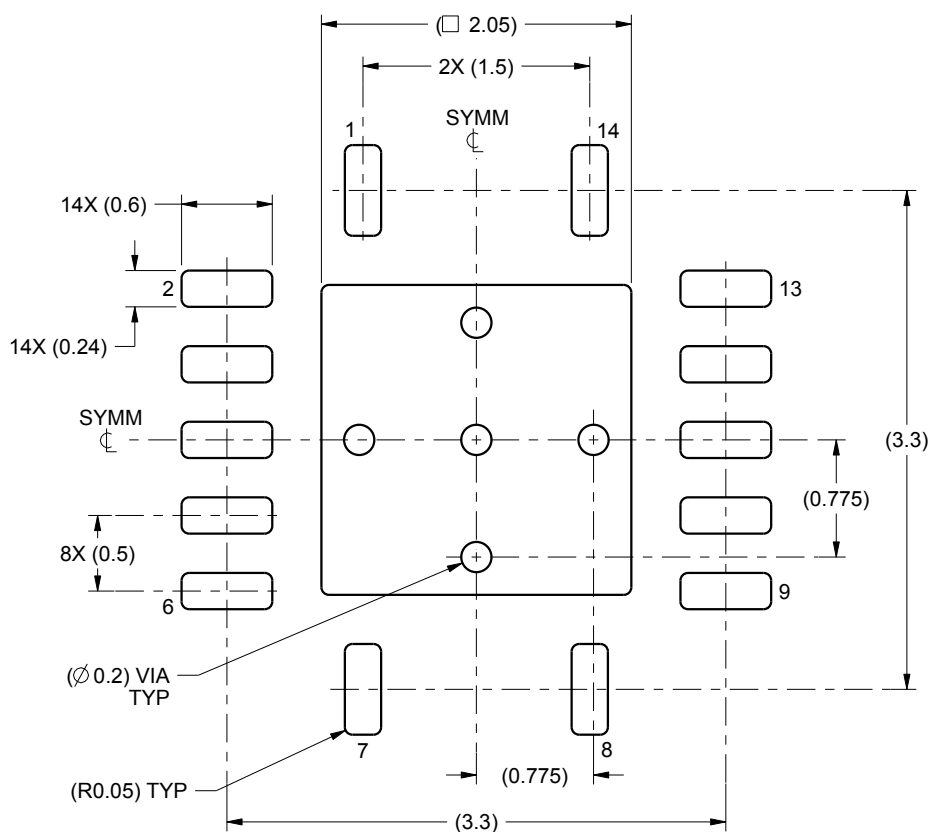
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

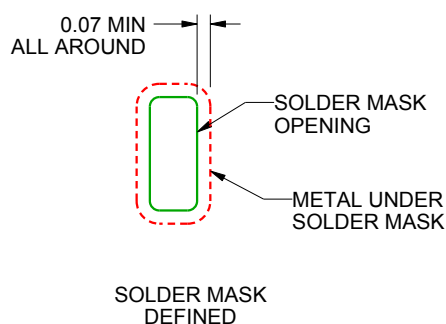
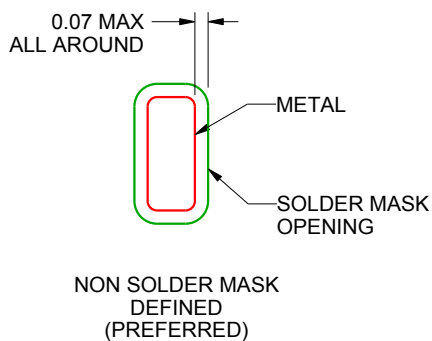
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

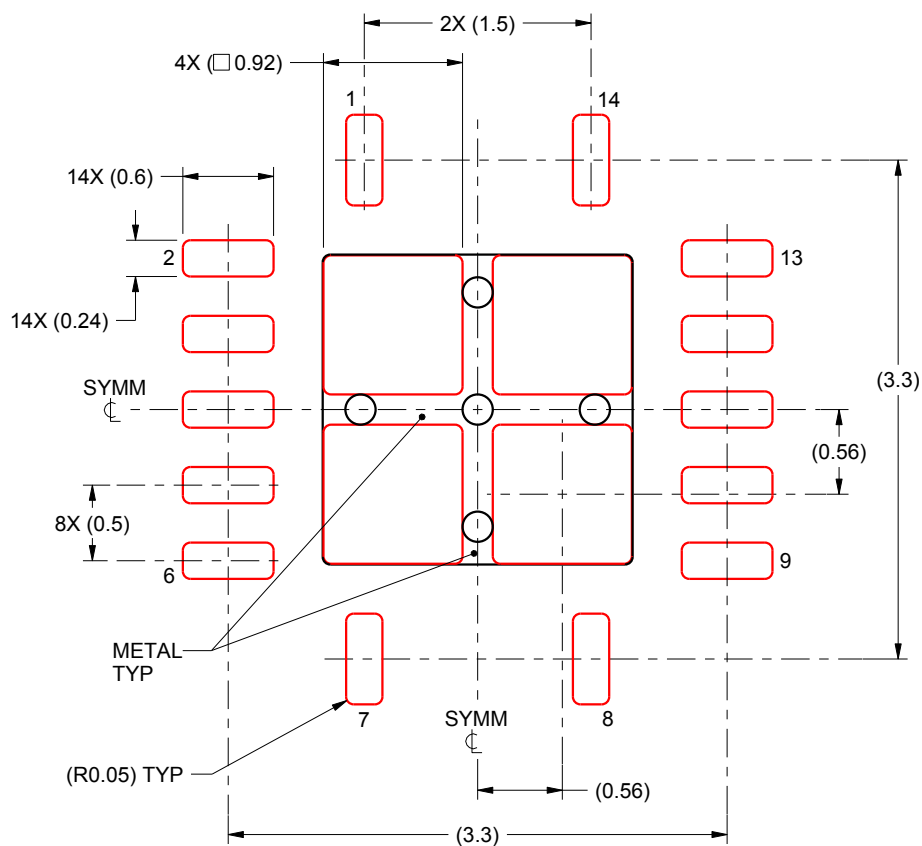
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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