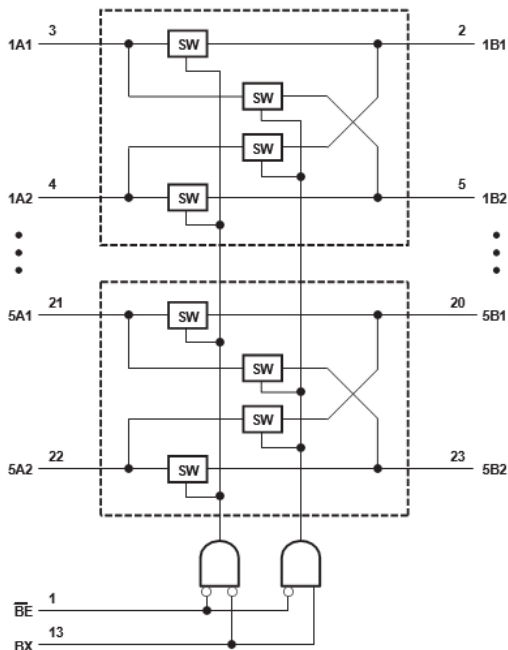


SN74CBT3383C 10 位 FET 总线交换开关 具有 -2V 下冲保护的 5V 总线开关

1 特性

- 针对 A 端口和 B 端口上的断开隔离提供高达 -2V 的下冲保护
- 具有接近零传播延迟的双向数据流
- 低导通状态电阻 (r_{on}) 特性 (r_{on} 典型值 = 3Ω)
- 低输入和输出电容可更大程度减小负载和信号失真 ($C_{io}(\text{OFF})$ 典型值 = 8pF)
- 数据与控制输入提供下冲钳位二极管
- 低功耗 (ICC 最大值为 $3\mu\text{A}$)
- V_{CC} 工作范围为 4V 至 5.5V, 数据 I/O 支持 0 至 5V 的信号电平 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V 和 5V)
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持局部关断模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范
- ESD 性能测试符合 JESD 22-2000V 人体放电模型 (A114-B, II 类) - 1000V 充电器件模型 (C101) 标准
- 支持数字和模拟应用: PCI 接口、内存交错、总线隔离、低失真信号门控



逻辑图 (正逻辑)

2 应用

- 企业级服务器
- 以太网交换机
- 路由器
- 服务器
- 工业 PC

3 说明

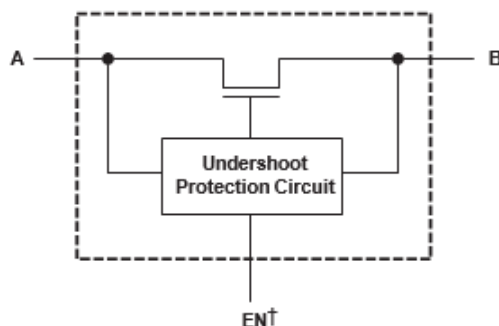
SN74CBT3383C 是一种具备低导通状态电阻 (r_{on}) 的高速 TTL 兼容型 FET 总线交换开关, 可实现超短传播延迟。SN74CBT3383C A 端口和 B 端口上的有源下冲保护电路可检测下冲事件并确保开关保持正常断开状态, 从而对高达 -2V 的下冲事件提供保护。

SN74CBT3383C 可配置为 10 位总线开关, 或具有单路输出使能 ($\overline{be}$) 输入的 5 位总线交换开关, 可在四个信号端口之间提供数据交换。选择 (BX) 输入可控制总线交换开关的数据路径。当 $\overline{BE}$ 为低电平时, A 端口连接到 B 端口, 从而实现端口之间的双向数据流。当 $\overline{BE}$ 为高电平时, A 和 B 端口之间为高阻抗状态。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN74CBT3383C	DBQ (SSOP, 24)	8.65mm × 3.90mm
	DW (SOIC, 24)	15.40mm × 7.50mm
	PW (TSSOP, 24)	7.80mm × 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



每个 FET 开关 (SW) 的简化版原理图)



Table of Contents

1 特性	1	9.3 Feature Description.....	10
2 应用	1	9.4 Device Functional Modes.....	10
3 说明	1	10 Application and Implementation	11
4 Revision History	2	10.1 Application Information.....	11
5 说明 (续)	3	10.2 Typical Application.....	11
6 Pin Configuration and Functions	4	11 Power Supply Recommendations	12
7 Specifications	5	12 Layout	13
7.1 Absolute Maximum Ratings.....	5	12.1 Layout Guidelines.....	13
7.2 ESD Ratings.....	5	12.2 Layout Example.....	13
7.3 Recommended Operating Conditions.....	5	13 Device and Documentation Support	14
7.4 Thermal Information.....	6	13.1 接收文档更新通知.....	14
7.5 Electrical Characteristics.....	6	13.2 支持资源.....	14
7.6 Switching Characteristics.....	7	13.3 Trademarks.....	14
7.7 Undershoot Characteristics.....	7	13.4 Electrostatic Discharge Caution.....	14
8 Parameter Measurement Information	8	13.5 术语表.....	14
9 Detailed Description	9	14 Mechanical, Packaging, and Orderable Information	14
9.1 Overview.....	9		
9.2 Functional Block Diagram.....	9		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2004) to Revision A (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了应用、引脚配置和功能、ESD 等级、热性能信息、详细说明、应用和实施、电源相关建议和布局部分.....	1
• 由于 (RLOI)，删除了数据表中的 DGV 和 DB 封装信息.....	1
• Updated the <i>Design Requirements</i> section.....	11

5 说明 (续)

该器件完全符合使用 I_{off} 的部分断电应用的规范要求。 I_{off} 特性确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

为确保上电或断电期间的高阻抗状态，应通过一个上拉电阻器将 $\overline{BE}$ 连接至 V_{CC} ；该电阻器的最小阻值由驱动器的电流吸收能力来决定。

6 Pin Configuration and Functions

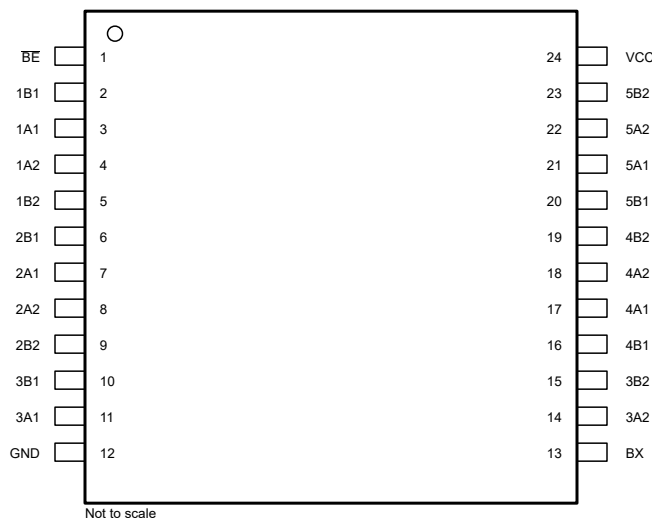


图 6-1. DBQ, DW, or PW Package, 24-Pin SSOP, SOIC, and TSSOP (Top View)

表 6-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BE	1	I	Active-low input enable pin
1B1	2	I/O	I/O pin, can be input or output
1A1	3	I/O	I/O pin, can be input or output
1A2	4	I/O	I/O pin, can be input or output
1B2	5	I/O	I/O pin, can be input or output
2B1	6	I/O	I/O pin, can be input or output
2A1	7	I/O	I/O pin, can be input or output
2A2	8	I/O	I/O pin, can be input or output
2B2	9	I/O	I/O pin, can be input or output
3B1	10	I/O	I/O pin, can be input or output
3A1	11	I/O	I/O pin, can be input or output
GND	12	G	Ground
BX	13	I	Select pin. This controls the data path of the bus exchange. When BX is low xA1 = xB1 and xA2 port = xB2. When BX is high xA1 = xB2 and xA2 = xB1
3A2	14	I/O	I/O pin, can be input or output
3B2	15	I/O	I/O pin, can be input or output
4B1	16	I/O	I/O pin, can be input or output
4A1	17	I/O	I/O pin, can be input or output
4A2	18	I/O	I/O pin, can be input or output
4B2	19	I/O	I/O pin, can be input or output
5B1	20	I/O	I/O pin, can be input or output
5A1	21	I/O	I/O pin, can be input or output
5A2	22	I/O	I/O pin, can be input or output
5B2	23	I/O	I/O pin, can be input or output
V _{CC}	24	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3) (4) (5) (6)}

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		-0.5	7	V
Control input voltage range, V_{IN} (see notes 1 and 2)		-0.5	7	V
Switch I/O voltage range, $V_{I/O}$ (see notes 1, 2, and 3)		-0.5	7	V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		-50		mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		-50		mA
ON-state switch current, I_{IO} (see note 4)		128		mA
Continuous current through V_{CC} or GND terminals		100		mA
Package thermal impedance, θ_{JA} (see note 5):				
T_{stg}	DBQ package	61		°C /W
	DW package	46		°C /W
	PW package	88		°C /W
	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal GND.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused control input of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74CBT3383			UNIT
	DBQ (SSOP)	DW (SOIC)	PW (TSSOP)	
	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	61.0	46.0	88.0	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	22.1	19.9	26.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	—	19.33	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}	Control inputs	$V_{CC} = 4.5\text{ V}$,	$I_{IN} = -18\text{ mA}$				-1.8	V
V_{IKU}	Data inputs	$V_{CC} = 5\text{ V}$,	$0\text{ mA} > I_I \geq -50\text{ mA}$, $V_{IN} = V_{CC}$ or GND,	Switch OFF			-2	V
I_{IN}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_{IN} = V_{CC}$ or GND				± 1	mA
$IOZ^{\dagger(3)}$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0$ to 5.5 V , $V_I = 0$,	Switch OFF, $V_{IN} = V_{CC}$ or GND			± 10	mA
I_{off}		$V_{CC} = 0$,	$V_O = 0$ to 5.5 V , $V_I = 0$	$V_I = 0$			10	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_{IO} = 0$, $V_{IN} = V_{CC}$ or GND,	Switch ON or OFF			3	mA
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V ,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	$V_{IN} = 3\text{ V}$ or 0				3.5		pF
$C_{io(OFF)}$		$V_{IO} = 3\text{ V}$ or 0 ,	Switch OFF, $V_{IN} = V_{CC}$ or GND			8		pF
$C_{io(ON)}$		$V_{IO} = 3\text{ V}$ or 0 ,	Switch ON, $V_{IN} = V_{CC}$ or GND			18.5		pF
$r_{on}^{(5)}$		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$		8	12	Ω
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 64\text{ mA}$		3	6	
				$I_O = 30\text{ mA}$		3	6	
			$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$		5	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All the typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter IOZ includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. The lower of the voltages of the two (A or B) terminals determines the ON-state resistance.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4 V		VCC = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A	0.24			0.15	ns
$t_{pd(s)}$	BX	A or B	5.8		1	5.3	ns
t_{en}	$\overline{BE}$	A or B	6.3		1	5.8	ns
t_{dis}	$\overline{BE}$	A or B	6		1	6	ns

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7.7 Undershoot Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OUTU}	$V_{CC} = 5.5 \text{ V}$,	Switch OFF,	$V_{IN} = V_{CC} \text{ or GND}$	2	$V_{OH} - 0.3$		V

- (1) All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

8 Parameter Measurement Information

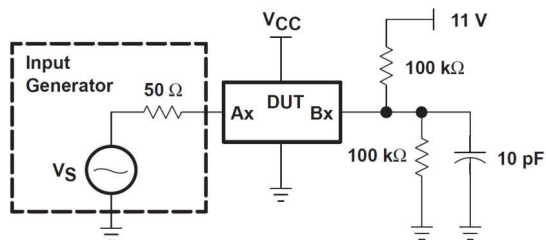


图 8-1. Device Test Setup

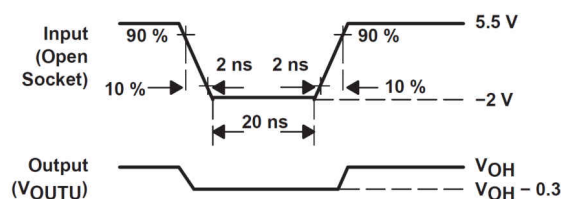
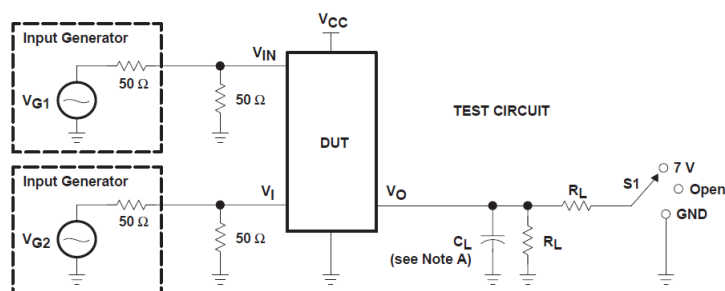
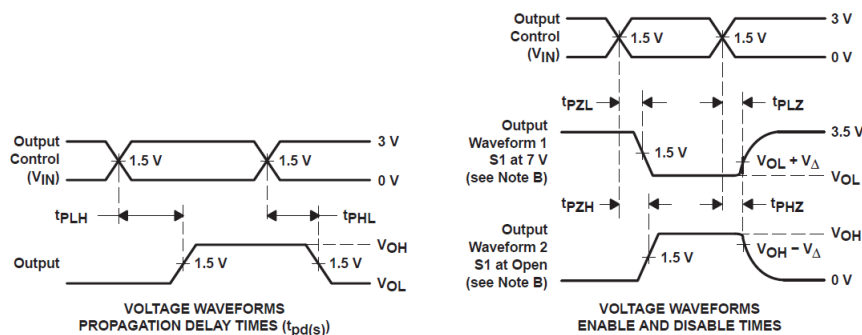


图 8-2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)



TEST	V_{CC}	S1	R_L	V_I	C_L	V_{Δ}
$t_{pd}(s)$	$5 V \pm 0.5 V$ 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	$5 V \pm 0.5 V$ 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	$5 V \pm 0.5 V$ 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as one or more t_{pds} . The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

图 8-3. Test Circuit and Voltage Waveforms

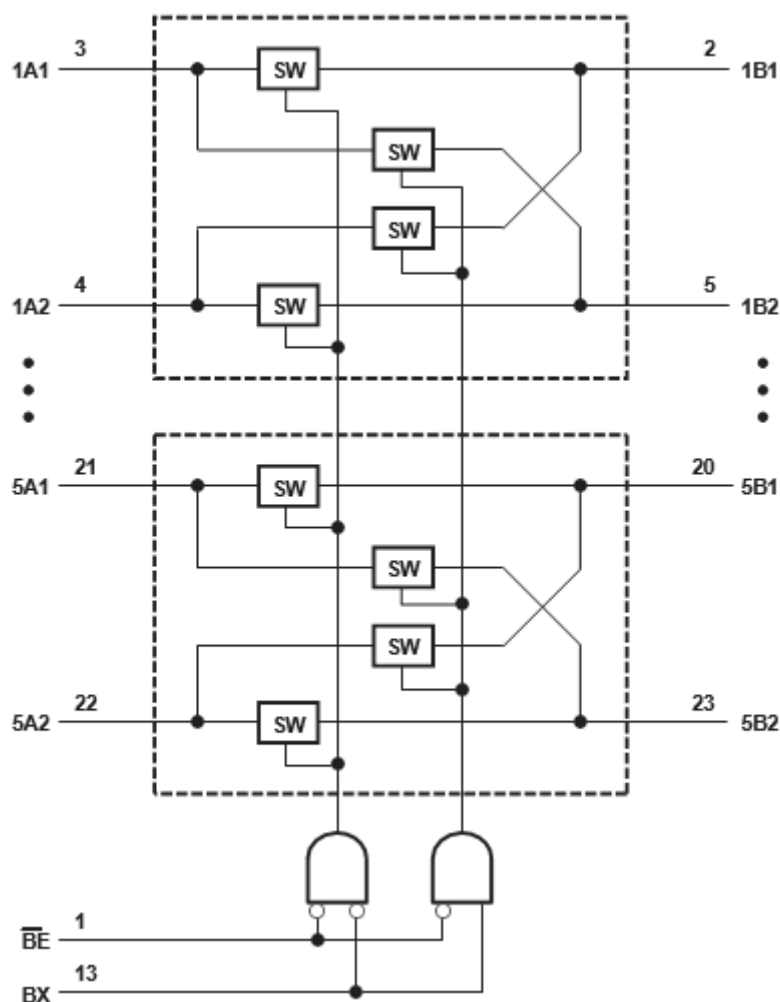
9 Detailed Description

9.1 Overview

The SN74CBT3383C provides ten high-speed CMOS TTL-compatible bus switches. The low ON-resistance of the SN74CBT3383C allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the 1A and 1B pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a 5-wide, 2-to-1 multiplexer, to create low delay barrel shifters, and so forth.

Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3383C provides protection for undershoot up to -2 V by sensing and undershoot event and ensuring that the switch remains in the proper OFF state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bidirectional Data Flow With Near-Zero Propagation Delay

The SN74CBT3383C features a low propagation delay or t_{pd} that works great for multiple rail information transfer (for example, from 1A1 to 1B1 and 1A2 to 1B2). However, the SN74CBT3383C also features BUS exchange functionality, which allows for bidirectional data transfers from the inputs and outputs connected on the B side. By enabling the BX pin, the outputs are now crossed or exchanged. Data can now flow from 1A1 to 1B2 and 1A2 to 1B1 with little to no propagation delay. This can be used to enable byte swapping of buses within a system or to create a 5-wide, 2-to-1 multiplexer.

9.4 Device Functional Modes

**表 9-1. Function Table
(Each 5-Bit Bus-Exchange)**

INPUTS		INPUTS/OUTPUTS		FUNCTION
BE	BX	1A1 – 5A1	1A2 – 5A2	
L	L	1B1 – 5B1	1B2 – 5B2	A1 port = B1 port, A2 port = B2 port
L	H	1B2 – 5B2	1B1 – 5B1	A1 port = B2 port, A2 port = B1 port
H	X	Z	Z	Disconnect

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The SN74CBT3383C can be used to multiplex up to 5 channels simultaneously in a 2:1 configuration. 图 10-1 shows a 2-bit bus being multiplexed between two devices. The $\overline{BE}$ and BX pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires only one bit control or exchange, then remember to tie the unused bit to high or low. By using another bus controller, exchange can be enabled across A1 and A2 to B1 and B2, allowing for greater system communication.

10.2 Typical Application

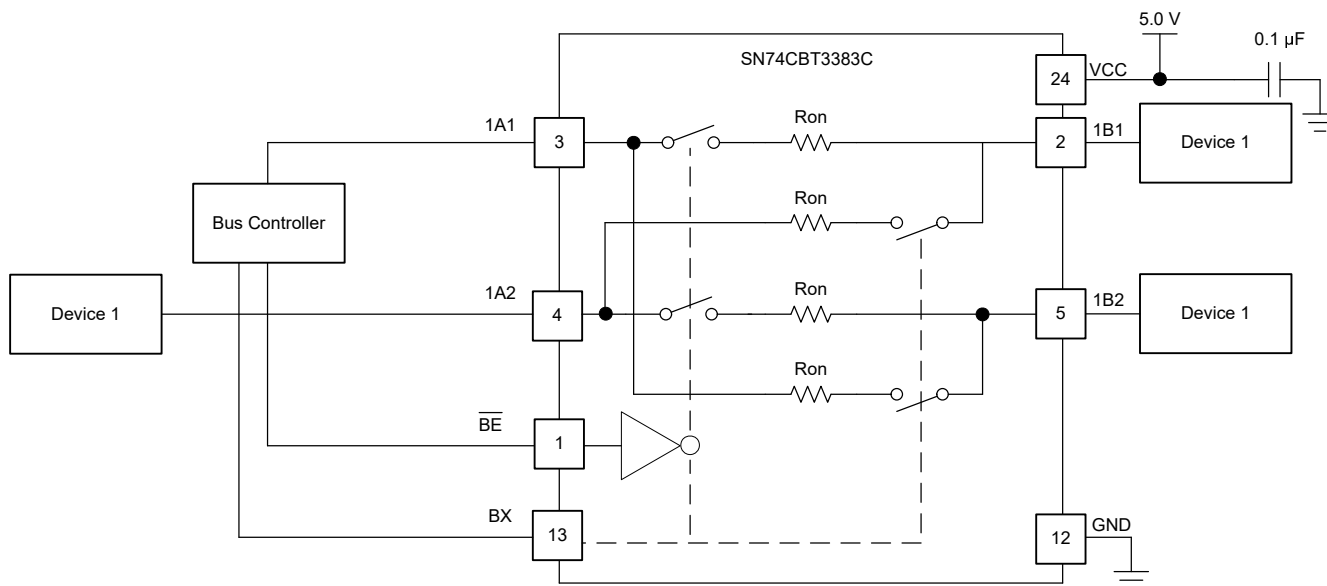


图 10-1. 1:2 Multiplexer or Bus and Selector Using 1 Bus Controller

10.2.1 Design Requirements

- Recommended input conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) section.
- Recommended output conditions:
 - Load currents must not exceed 128 mA per channel.
- Frequency selection criteria:
 - Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in the [Layout](#) section.

10.2.2 Detailed Design Procedure

The 2-bit bus is connected directly to 1A1 and 1A2 on the SN74CBT3383C, which essentially combines in the bus controller to form a single input or split bus bits. When $\overline{BE}$ is low and BX is low, the selected bus uses 1A1 and 1B1 as inputs and outputs. This means that Device 1 is connected to the bus controller and Device 2 is connected to Device 3 when $\overline{BE}$ is low and BX is low. While keeping $\overline{BE}$ low and BX high, communication is enabled from the bus controller to Device 2 and from Device 1 to Device 3. This setup is especially useful when two controllers or devices need to share the same data from Device 1 and Device 2 and the bus addresses are limited or hard coded.

The 0.1- μ F capacitor on V_{CC} is a decoupling capacitor and should be placed as close to the device as possible.

10.2.3 Application Curve

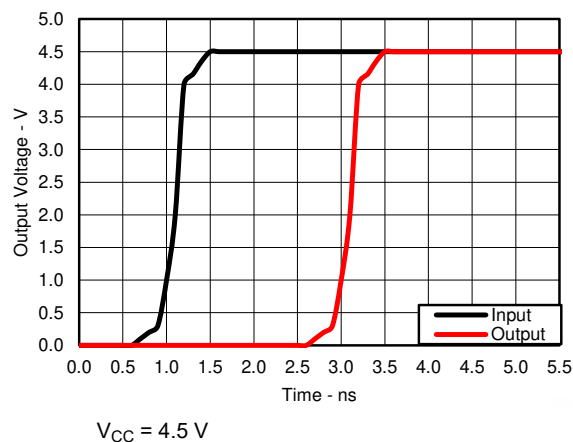


图 10-2. Propagation Delay (t_{pd}) Simulation Results

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of the trace width. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 12-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

12.2 Layout Example

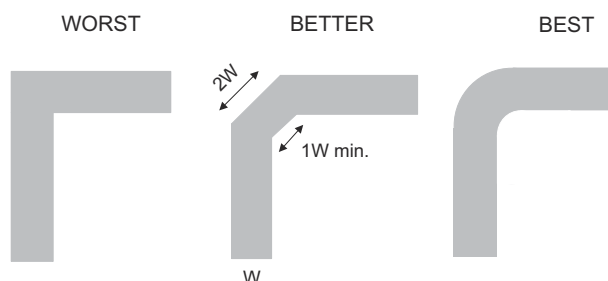


图 12-1. Trace Example

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT3383CDBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383C
SN74CBT3383CDBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383C
SN74CBT3383CDW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CPWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383C
SN74CBT3383CPWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3383CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3383CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CBT3383CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBT3383CPWR	TSSOP	PW	24	2000	353.0	353.0	32.0

TUBE

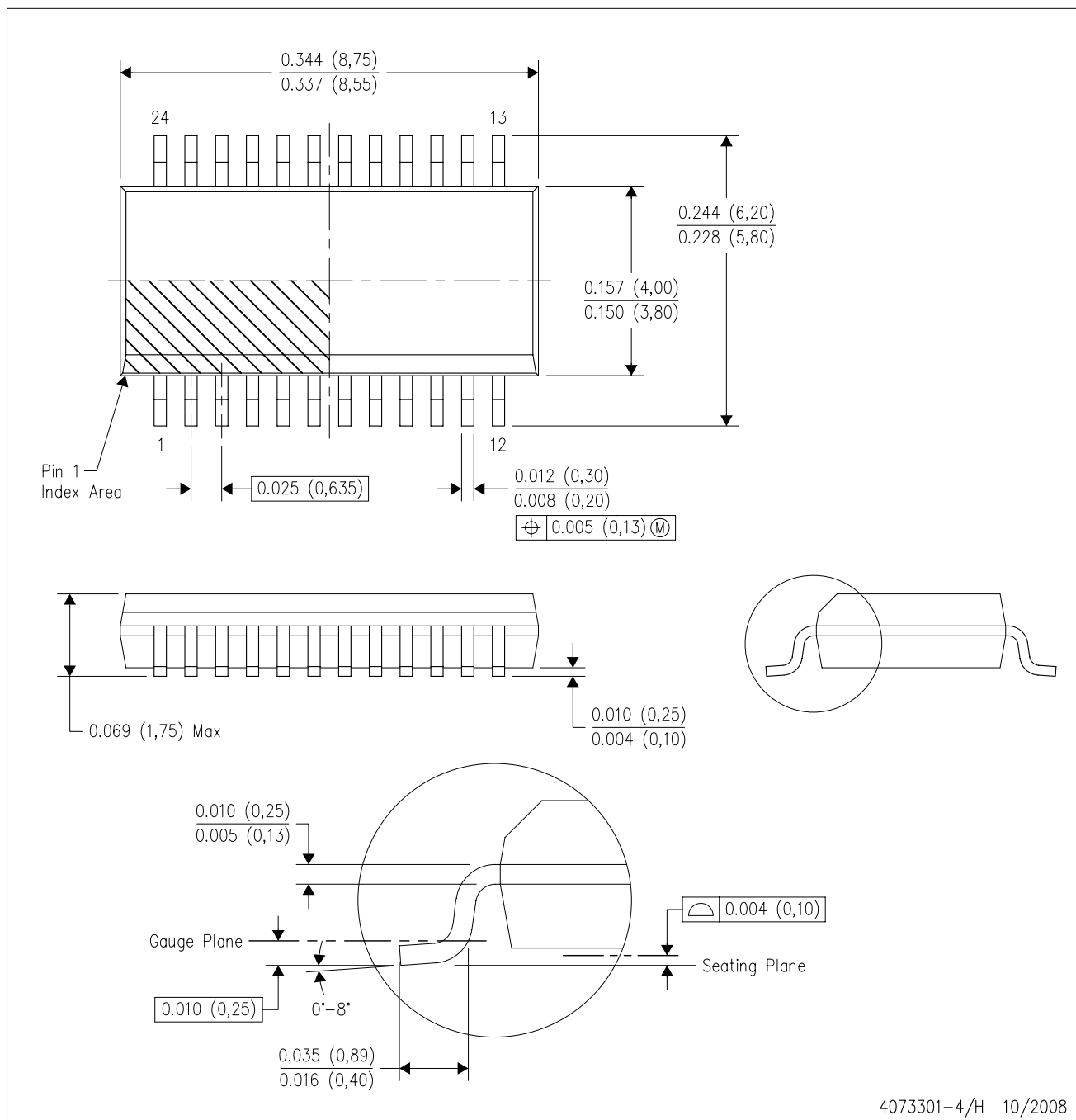


*All dimensions are nominal

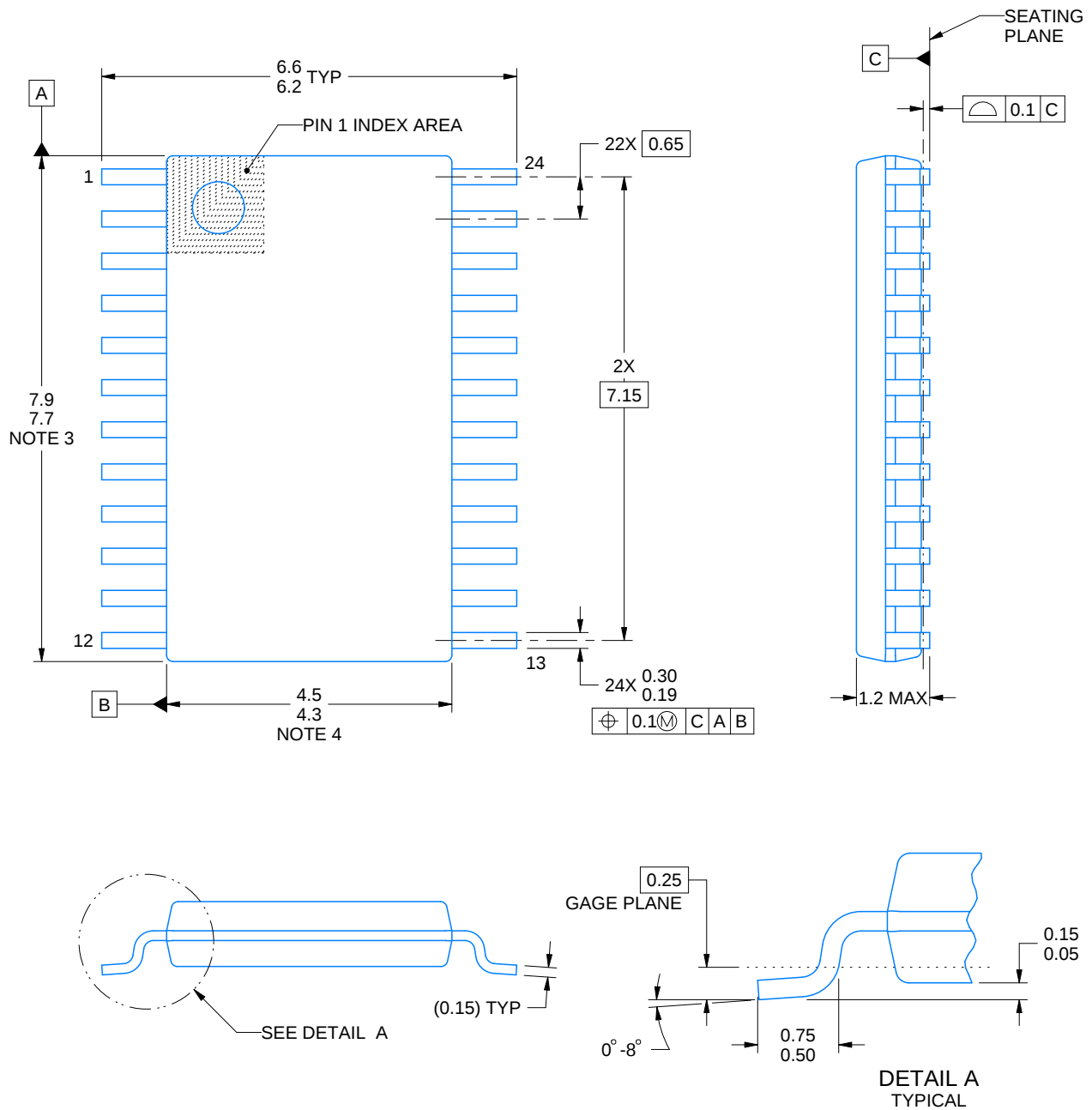
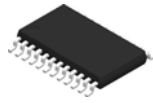
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3383CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBT3383CDW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.



4220208/A 02/2017

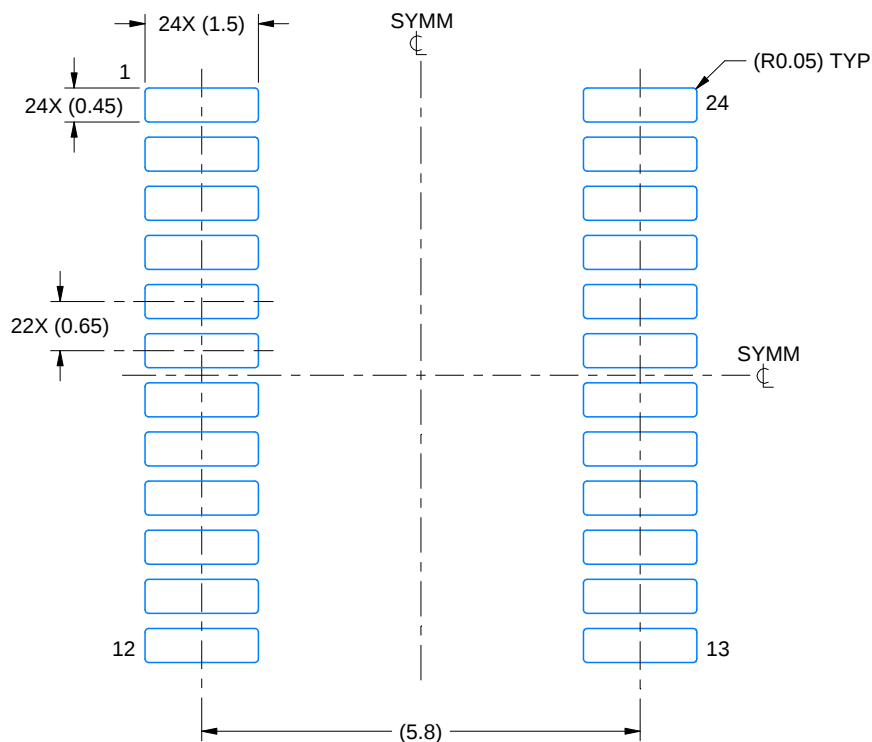
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

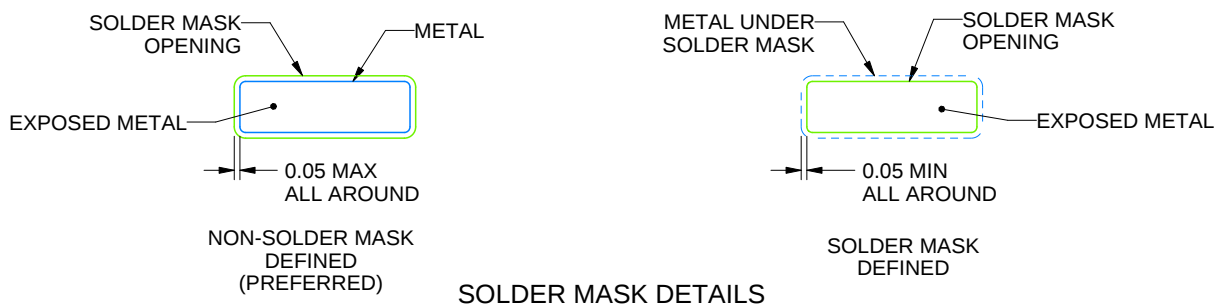
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

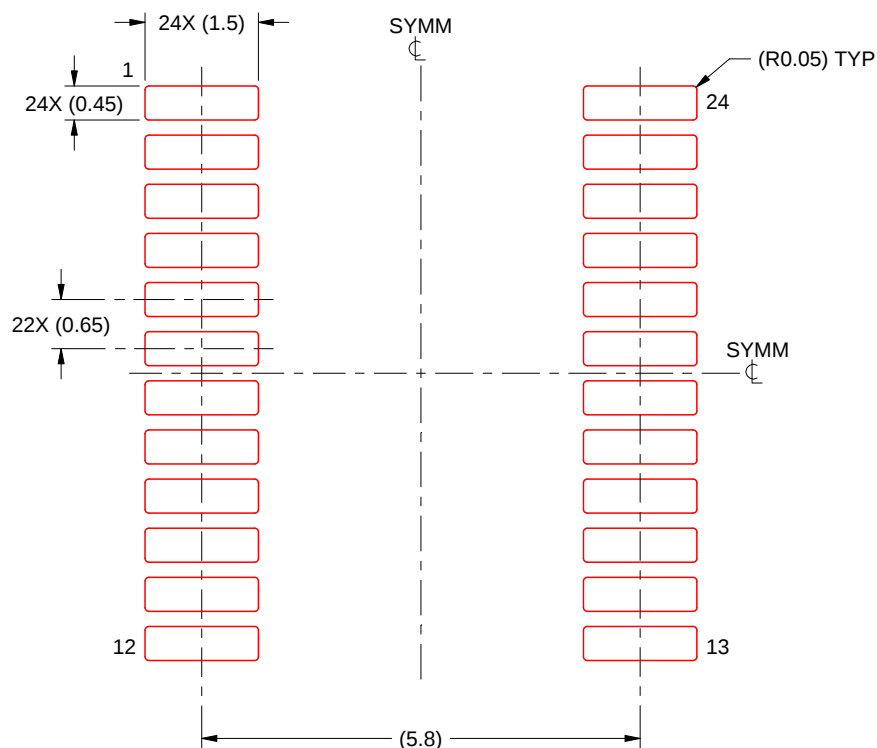
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

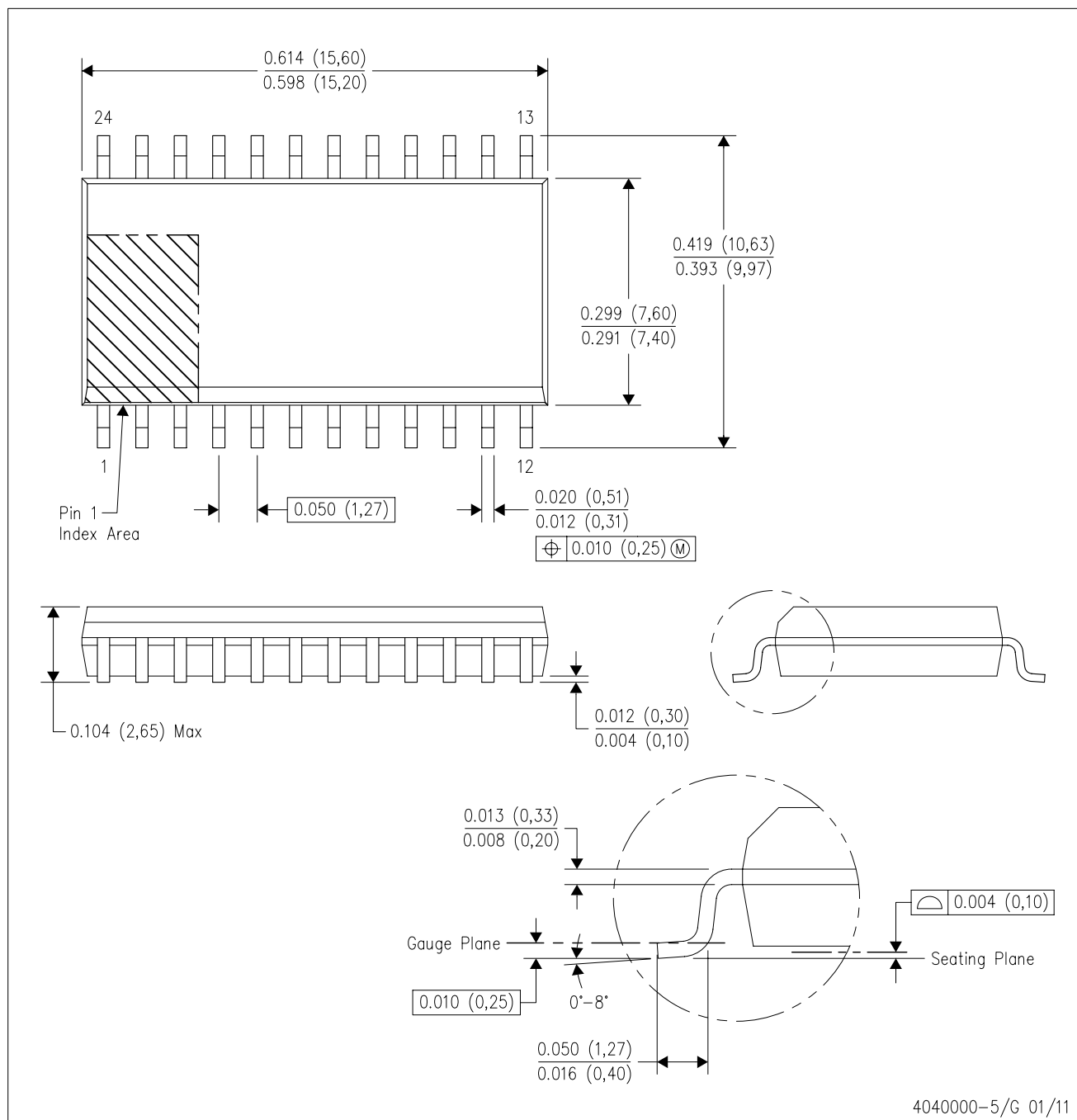
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司