SN74CB3T3257 4 位 2 选 1 FET 多路复用器/多路信号分离器 2.5V/3.3V 低电压总线开关，具有可耐受 5V 电压的电平移位器

1 特性

- 输出电压转换跟踪 V_{CC}
- 所有数据 I/O 端口上均支持以混合模式信号运行
  - 5V 输入降至 3.3V 输出的电平位移，V_{CC} 为 3.3V
  - 5V/3.3V 输入降至 2.5V 输出的电平位移，V_{CC} 为 2.5V
- 可耐受 5V 电压并支持器件加电或断电的 I/O
- 具有接近零传播延迟的双向数据流
- 低导通状态电阻 (r_{on}) 特性（r_{on} 典型值 = 5Ω）
- 低输入/输出电容可更大程度减小负载（$C_{io(OFF)}$ 典型值 = 5pF）
- 数据与控制输入提供下冲钳位二极管
- 低功耗（I_{CC} 最大值 = 20 µA）
- V_{CC} 工作范围为 2.3V 至 3.6V
- 数据 I/O 支持 0V 至 5V 信号电平（0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V）
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 支持数字应用：
  - 电平转换
  - USB 接口
  - 内存交错
  - 总线隔离
- 专为低功耗便携式设备设计

3 说明

SN74CB3T3257 是一种具备低导通状态电阻 (r_{on}) 的高速 TTL 兼容型 FET 多路复用器/多路信号分离器，可实现超短传播延迟。该器件通过提供可跟踪 V_{CC} 的电压转换，完全支持在所有数据 I/O 端口上以混合模式信号运行。SN74CB3T3257 支持使用 5V TTL、3.3V LVTTL 和 2.5V CMOS 开关标准以及用户定义的开关电平的系统。

该器件专用于使用 I_{off} 的局部断电应用。I_{off} 特性可验证器件断电时破坏性电流不会通过器件回流。该器件可在关断时提供隔离。

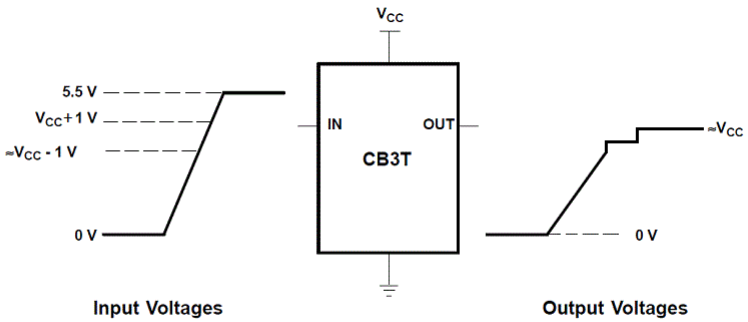
封装信息

器件型号	封装 (1)	本体尺寸（标称值）
SN74CBTLV3257PW	TSSOP (16)	5.00mm × 4.40mm
SN74CBTLV3257DGV	TVSOP (16)	3.60mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件信息

输入		输入/输出 A	功能
$\overline{OE}$	S		
L	L	B1	A 端口 = B1 端口
L	H	B2	A 端口 = B2 端口
H	X	Z	断开



If the input high voltage (V_{IH}) level is greater than or equal to V_{CC}+ 1V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

典型直流电压转换特性

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4 Pin Configuration and Functions

DGV OR PW PACKAGE
(TOP VIEW)

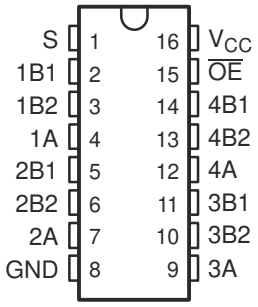


图 4-1. DGV or PW Package, 16 PinTVSOP, and TSSOP (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	TVSOP, TSSOP		
1A	4	I/O	Channel 1 out/in common
1B1	2	I/O	Channel 1 in/out 1
1B2	3	I/O	Channel 1 in/out 2
2A	7	I/O	Channel 2 out/in common
2B1	5	I/O	Channel 2 in/out 1
2B2	6	I/O	Channel 2 in/out 2
3A	9	I/O	Channel 3 out/in common
3B1	11	I/O	Channel 3 in/out 1
3B2	10	I/O	Channel 3 in/out 2
4A	12	I/O	Channel 4 out/in common
4B1	14	I/O	Channel 4 in/out 1
4B2	13	I/O	Channel 4 in/out 2
GND	8	—	Ground
$\overline{OE}$	15	I	Output Enable, active low
S	1	I	Select
V_{CC}	16	—	Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	-0.5	7	V
V_{IN}	Control input voltage(2) (3)	-0.5	7	V
$V_{I/O}$	Voltage range applied to any output in the high-impedance or power-off state(2) (3) (4)	-0.5	7	V
I_{IK}	Control input clamp current V_{IN} < 0	-50		mA
$I_{I/O}$	I/O port diode current $V_{I/O}$ < 0	-50		mA
$I_{I/O}$	On-state switch current(5) $V_{I/O}$ = 0 to V_{CC}	-128	128	mA
	Continuous current through V_{CC} or GND	-100	100	mA
T_J	Junction temperature		150	C
Storage temperature, T_{stg}		-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) V_I, V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I, I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.3		3.6	V
$V_{I/O}$	Switch input or output voltage		0		5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 2.3V to 2.7V	1.7		5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 2.7V to 3.6V	2		5.5	V
V_{IL}	Low-level input voltage, control input	V_{CC} = 2.3V to 2.7V	0		0.7	V
V_{IL}	Low-level input voltage, control input	V_{CC} = 2.7V to 3.6V	0		0.8	V
T_A	Operating free-air temperature		-40		85	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the Implications of Slow or Floating CMOS Inputs application note.

5.4 Thermal Information

THERMAL METRIC (1)		SN74CBTLV3257		UNIT
		DGV	PW	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	129.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Over operating free-air temperature range

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
		V_{CC} V	**$V_{I/o}$ V or Ii or VIN**	**I_O mA or Vo or VIN**	**T_A**				
r_{ON}	ON-state switch resistance	2.3, TYP at 2.5V	V_I = 0 V	I_O = 24 mA	– 40°C to +85°C		5	8	Ω
r_{ON}	ON-state switch resistance	2.3, TYP at 2.5V	V_I = 0 V	I_O = 16 mA	– 40°C to +85°C		5	8	Ω
r_{ON}	ON-state switch resistance	3, TYP at 3.3V	V_I = 0 V	I_O = 64 mA	– 40°C to +85°C		5	7	Ω
r_{ON}	ON-state switch resistance	3, TYP at 3.3V	V_I = 0 V	I_O = 32 mA	– 40°C to +85°C		5	7	Ω
Ioff	Power down switch leakage current	0	V_I = 0 V	$0 \leqslant V_O \leqslant 5.5$ V	– 40°C to +85°C	-10		10	µA
Ioz	Switch OFF leakage current	3.6	V_I = 0 V, Vin = Vcc or GND	$0 \leqslant V_O \leqslant 5.5$ V	– 40°C to +85°C	-10		10	µA
II	ON-state switch leakage current	3.6	V_I = Vcc-0.7 to 5.5V	V_{IN} = V_{CC} or GND	– 40°C to +85°C	-20		20	µA
II	ON-state switch leakage current	3.6	V_I = 0.7 to Vcc-0.7	V_{IN} = V_{CC} or GND	– 40°C to +85°C			-40	µA
I_{II}	ON-state switch leakage current	3.6	V_I = 0 to 0.7V	V_{IN} = V_{CC} or GND	– 40°C to +85°C	-5		5	µA
I_{IN}	Control input current	3.6	$Vcc \leqslant V_{IN} \leqslant 5.5$ or Vin = 0V		– 40°C to +85°C	-10		10	µA
I_{CC}	Supply current	3.6	V_I = Vcc or GND, Ii/o = 0	V_{IN} = V_{CC} or GND	– 40°C to +85°C			20	µA
I_{CC}	Supply current	3.6	V_I = 5.5V, Ii/o = 0	V_{IN} = V_{CC} or GND	– 40°C to +85°C			20	µA
ΔI_{CC}	Quiescent Device Current w.r.t Control inputs	3 to 3.6V	V_{IN} = Vcc - 0.6V	Other inputs at 0/VCC	– 40°C to +85°C			300	µA
C_I	Control input capacitance	3.3	V_{IN} = Vcc or GND		25°C		3		pF
$C_{io(off)}$	A port: Switch input/output capacitance	3.3	V_I = 5.5V, 3.3V, 0V	V_{IN} = 0/Vcc s.t switch is off	25°C		8		pF
$C_{io(on)}$	A port: Switch input/output capacitance	3.3	V_I = 5.5V or 3.3V	V_{IN} = 0/Vcc s.t switch is on	25°C		6		pF
$C_{io(on)}$	A port: Switch input/output capacitance	3.3	V_I = 0V	V_{IN} = 0/Vcc s.t switch is on	25°C		16		pF
$C_{io(off)}$	B port: Switch input/output capacitance	3.3	V_I = 5.5V, 3.3V, 0V	V_{IN} = 0/Vcc s.t switch is off	25°C		5		pF
$C_{io(on)}$	B port: Switch input/output capacitance	3.3	V_I = 5.5V or 3.3V	V_{IN} = 0/Vcc s.t switch is on	25°C		4		pF
$C_{io(on)}$	B port: Switch input/output capacitance	3.3	V_I = 0V	V_{IN} = 0/Vcc s.t switch is on	25°C		16		pF
V_{ik}	Clamp voltage	3	I_I = -18mA		– 40°C to +85°C			-1.2	V

5.6 Switching Characteristics 85C

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER WITH TEST CONDITIONS		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 1GΩ, C_L = 30pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	2.5 V ± 0.2 V			0.15	ns
t_{pd}	R_L = 1GΩ, C_L = 50pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	3.3 V ± 0.3 V			0.25	ns
t_{en}	ZL: R_L = 250Ω, C_L = 30pF, V_{load} = VCC, ZH: RL = 500Ω, CL = 30pF, Vload = GND, 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V	1		10.4	ns
t_{en}	ZL: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC} ZH: RL = 500Ω, CL = 50pF, Vload = GND, 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V	1		8.3	ns
t_{dis}	LZ: R_L = 250Ω, C_L = 30pF, V_{load} = V_{CC}, V▲ = 0.15V; HZ: RL = 500Ω, CL = 30pF, Vload = GND, V▲ = 0.15V; 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V	1		7.4	ns
t_{dis}	LZ: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, V▲ = 0.3V; HZ: RL = 500Ω, CL = 50pF, Vload = GND, V▲ = 0.3V; 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V	1		8	ns
$t_{pd(s)}$	R_L = 500Ω, C_L = 30pF, V_{load} = 0V. Vinput = 3.6V domain. 50ohm termination at input	S	A	2.5 V ± 0.2 V			13.4	ns
$t_{pd(s)}$	R_L = 500Ω, C_L = 50pF, V_{load} = 0V. Vinput = 5.5V domain. 50ohm termination at input	S	A	3.3 V ± 0.3 V			10.1	ns
$t_{en(s)}$	ZL: R_L = 250Ω, C_L = 30pF, V_{load} = VCC, ZH: RL = 500Ω, CL = 30pF, Vload = GND; 50ohm termination at input	S	B	2.5 V ± 0.2 V	1		13	ns
$t_{en(s)}$	ZL: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC} ZH: RL = 500Ω, CL = 50pF, Vload = GND; 50ohm termination at input	S	B	3.3 V ± 0.3 V	1		10.1	ns
$t_{dis(s)}$	LZ: R_L = 250Ω, C_L = 30pF, V_{load} = V_{CC}, V▲ = 0.15V; HZ: RL = 500Ω, CL = 30pF, Vload = GND, V▲ = 0.15V; 50ohm termination at input	S	B	2.5 V ± 0.2 V	1		9.1	ns
$t_{dis(s)}$	LZ: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, V▲ = 0.3V; HZ: RL = 500Ω, CL = 50pF, Vload = GND, V▲ = 0.3V; 50ohm termination at input	S	B	3.3 V ± 0.3 V	1		8.3	ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impednace).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.

5.7 Typical Characteristics

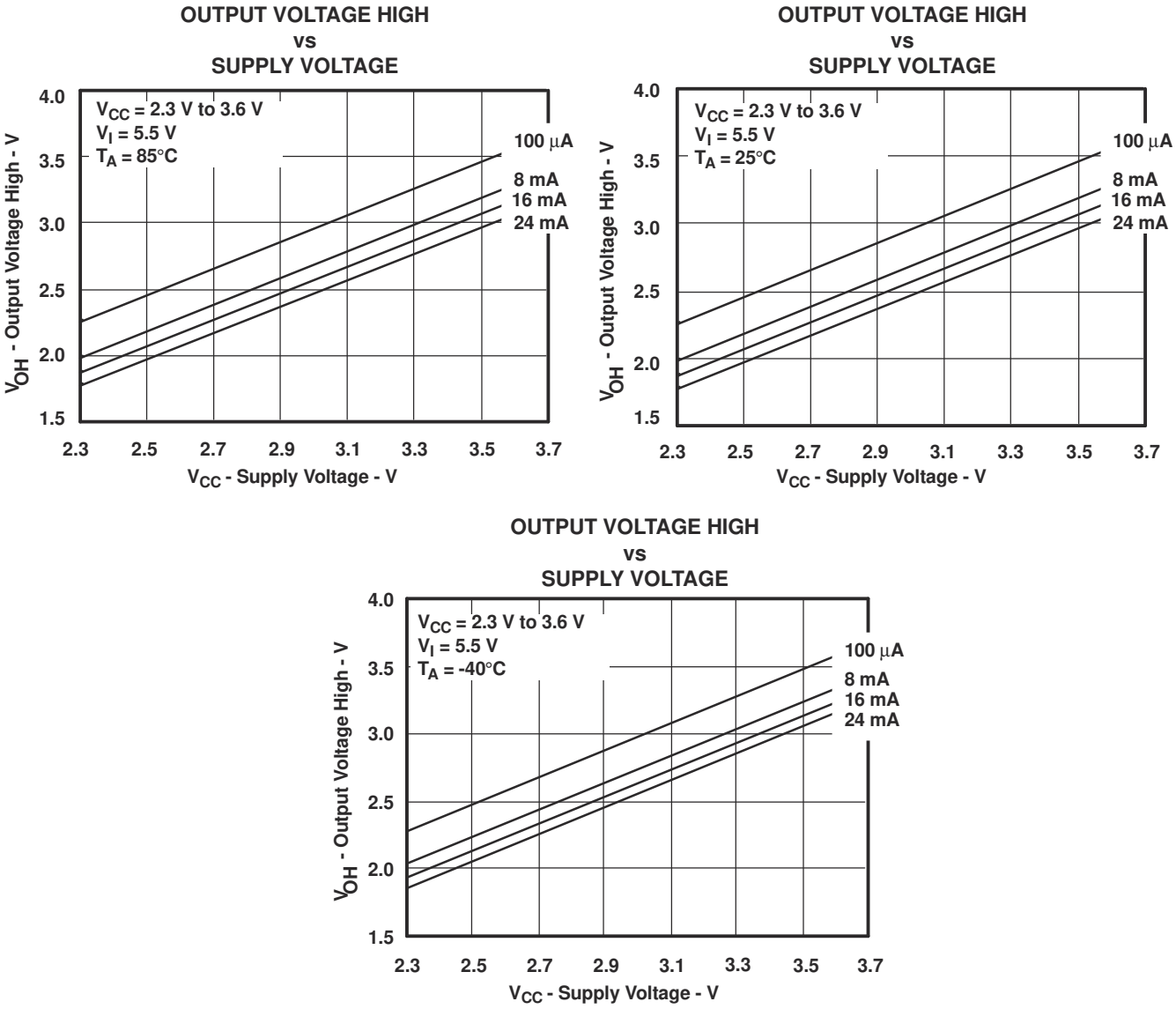
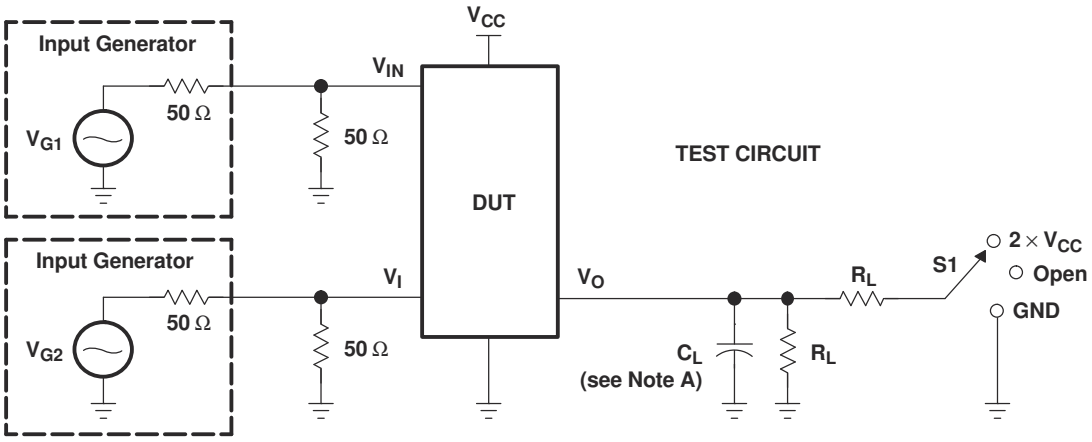
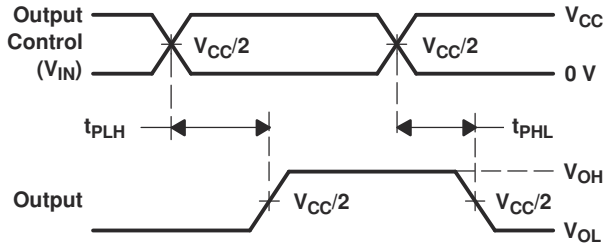


图 5-1. V_{OH} Values

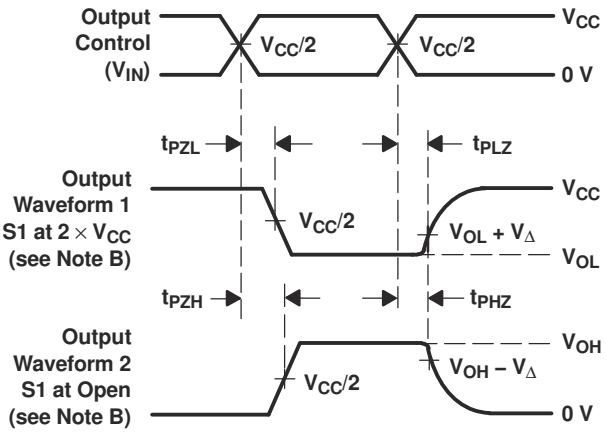
6 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	$2 \times V_{CC}$ $2 \times V_{CC}$	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

图 6-1. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

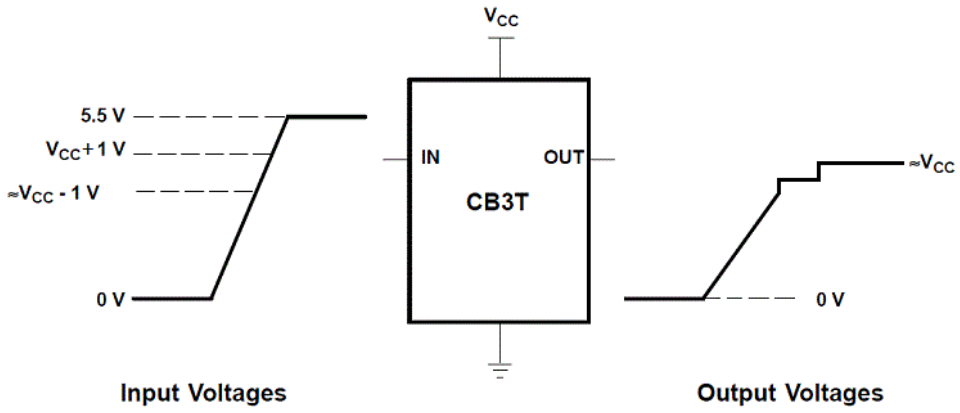
The SN74CB3T3257 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3257 supports systems using 5V TTL, 3.3V LVTTL, and 2.5V CMOS switching standards, as well as user-defined switching levels (see 典型直流电压转换特性).

The SN74CB3T3257 is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S) input controls the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature verifies that damaging current does not backflow through the device when the device is powered down. The device has isolation during power off.

To confirm the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



If the input high voltage (V_{IH}) level is greater than or equal to V_{CC}+ 1V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

图 7-1. Typical DC Voltage-Translation Characteristics

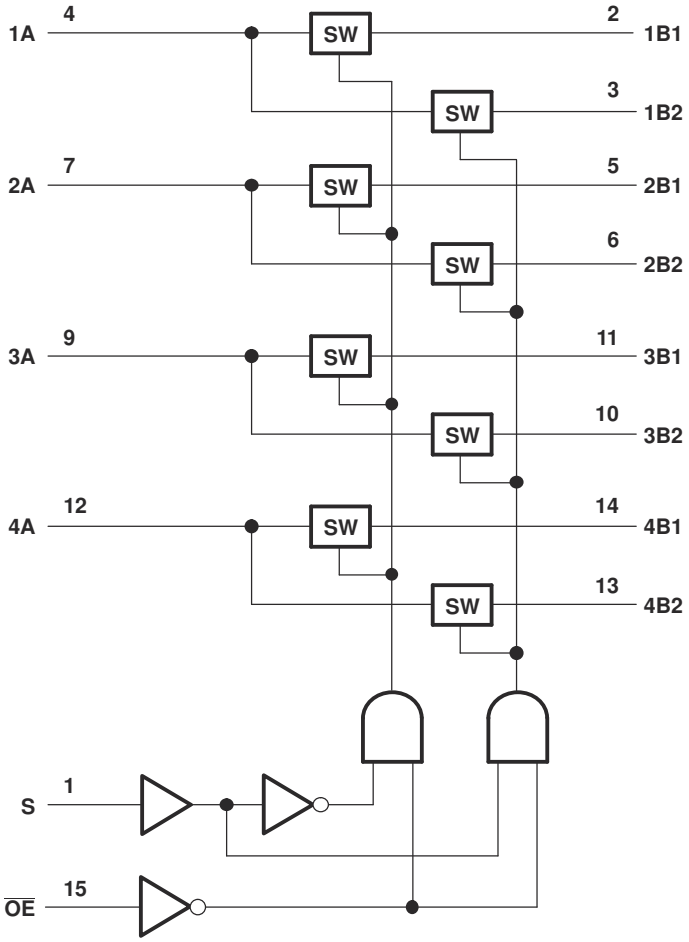
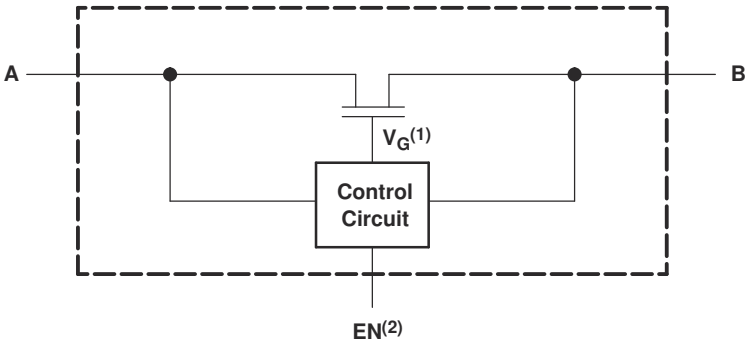


图 7-2. Logic Diagram (Positive Logic)



(1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) EN is the internal enable signal applied to the switch.

图 7-3. Simplified Schematic, Each FET Switch (SW)

7.3 Feature Description

The SN74CB3T3257 features 5 Ω switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I_{off} supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 250mA per JESD 17.

7.4 Device Functional Modes

表 7-1 shows the functional modes of SN74CBTLV3257.

表 7-1. Function Table

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74CB3T3257 is used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus, multiplexed between two devices. The $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a generic example, and can apply to many situations. If an application requires less than 4 bits, tie the A side to either high or low on unused channels.

8.2 Typical Application

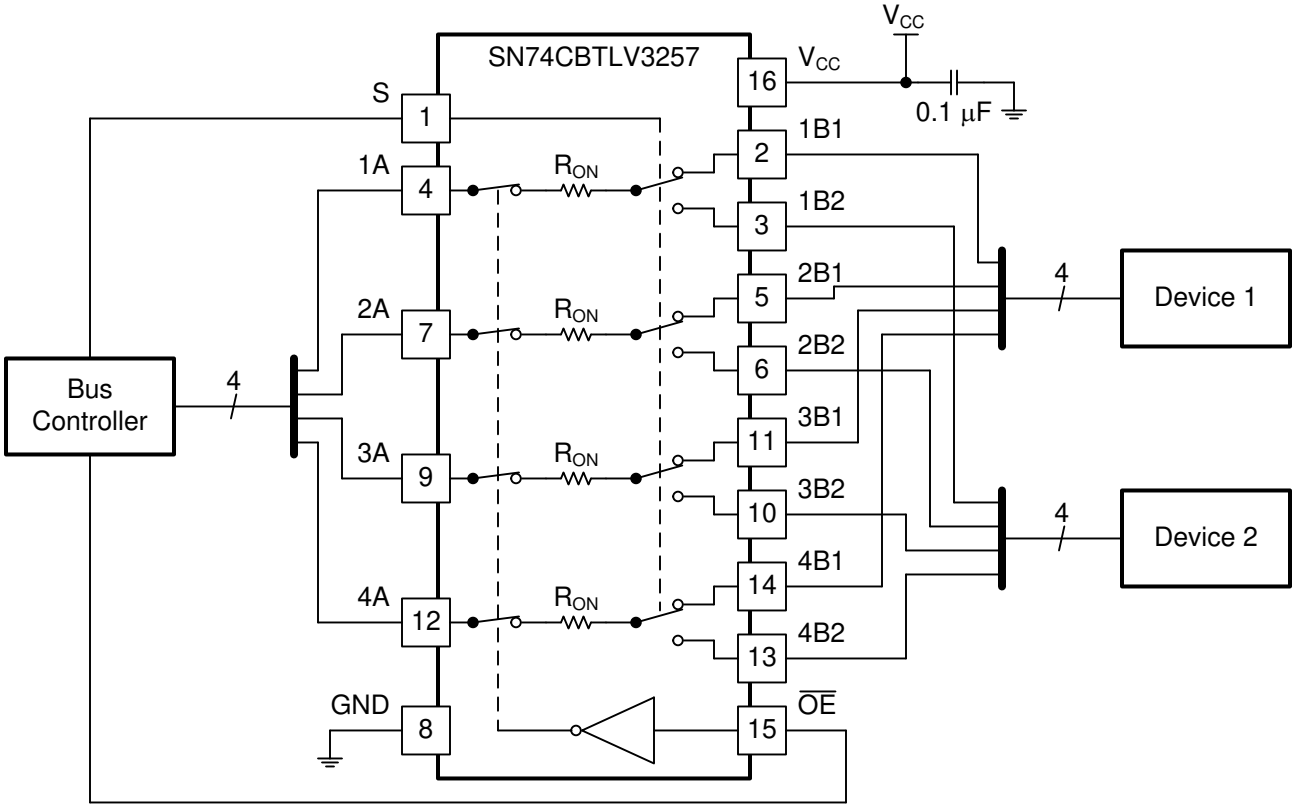


图 8-1. Typical Application of the SN74CBTLV3257

8.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in 节 5.3.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed ±128mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 200MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in 节 8.4.

8.2.2 Detailed Design Procedure

The 4-bit bus is connected directly to the 1A, 2A, 3A, and 4A ports (known as the xA port) on the SN74CBTLV3257. This splits into two busses, out of the xB1 and xB2 ports. When S is high, xB2 is the active bus, and when S is low, xB1 is the active bus. This means that Device 2 is connected to the bus controller when S is high, and Device 1 is connected to the bus controller when S is low. This setup is useful when two devices are hard coded with the same address and only one bus is available. The $\overline{OE}$ connection can be used to disconnect all devices from the bus controller if necessary.

The 0.1µF capacitor on V_{CC} is a decoupling capacitor and must be placed as close as possible to the device.

8.2.3 Application Performance Plots

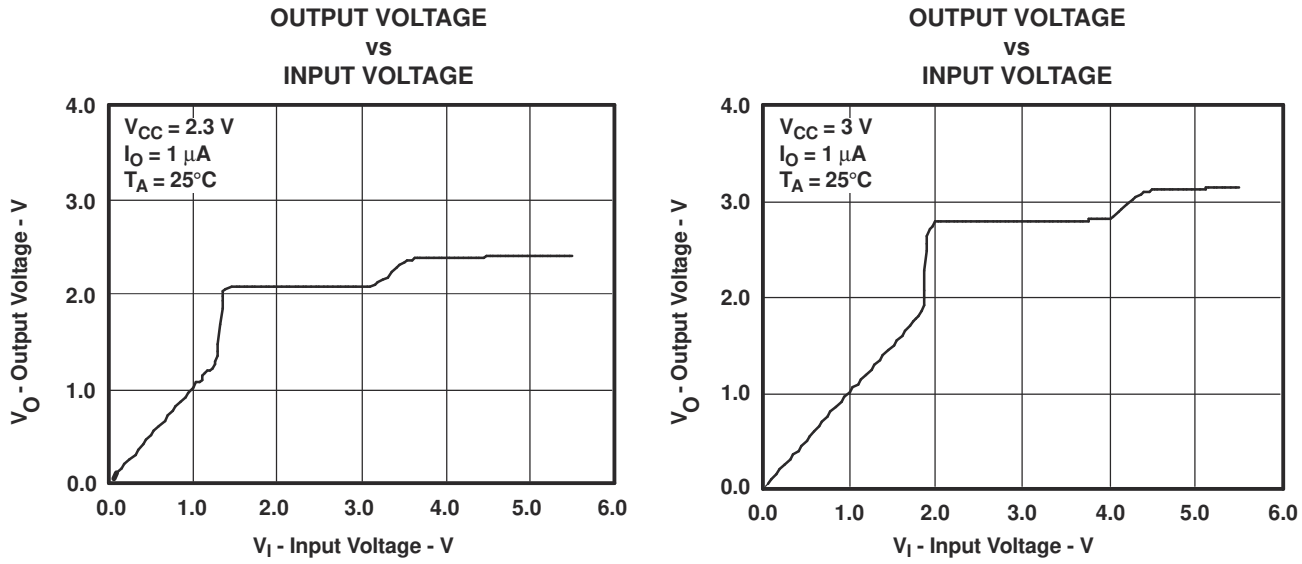


图 8-2. Data Output Voltage vs Data Input Voltage

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the 节 5.3 table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01 μF or 0.022 μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

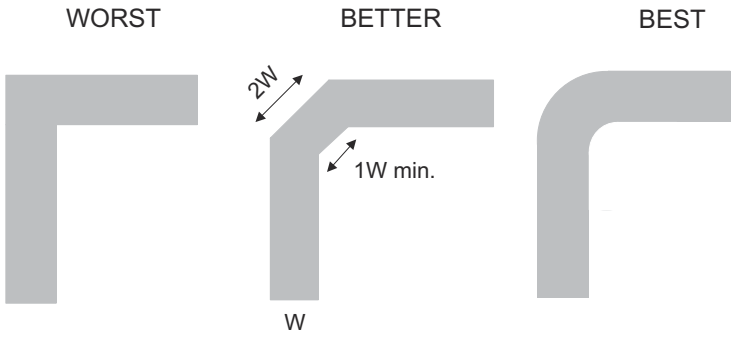


图 8-3. Trace Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch*

9.1.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.1.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.1.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.1.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (October 2003) to Revision A (May 2025) **Page**

- 添加了*引脚配置和功能*、*规格*、*ESD 等级*、*热性能信息*、*概述*、*功能方框图*、*器件功能模式*、*应用和实现*、*典型应用*、*电源相关建议*、*布局*、*布局指南*、*布局示例*、*器件和文档支持*，以及*机械、封装和可订购信息*部分 .. 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Updated specs in the *Electrical Characteristics* table 6
- Updated specs in the *Switching Characteristics 85C* table 7

DATE	REVISION	NOTES
October 2003	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3T3257DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257DGVRG4	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257DGVRG4.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	KS257
SN74CB3T3257PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257
SN74CB3T3257PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS257

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

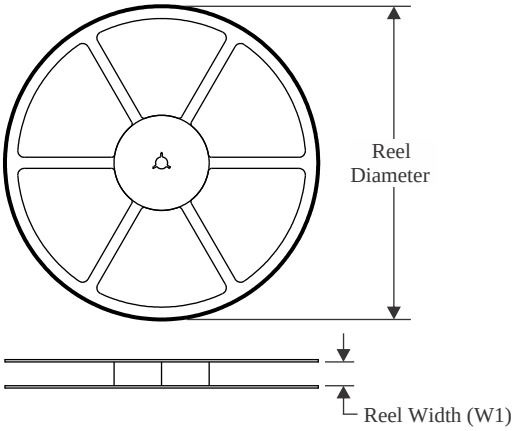
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

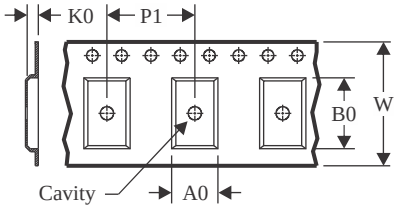
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

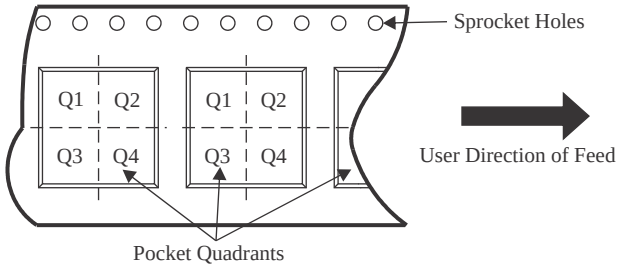


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

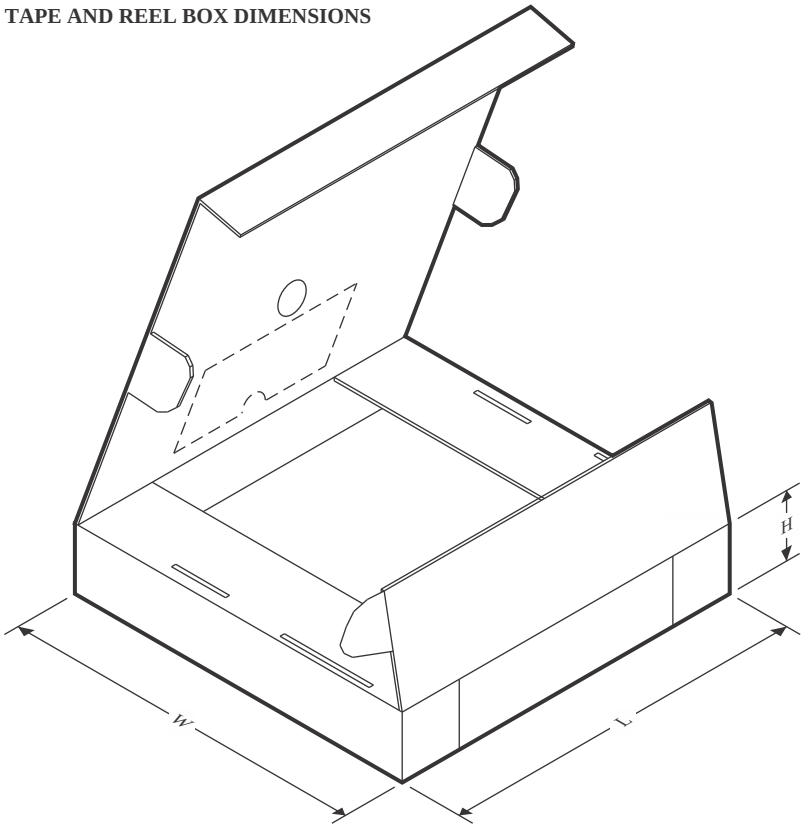
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

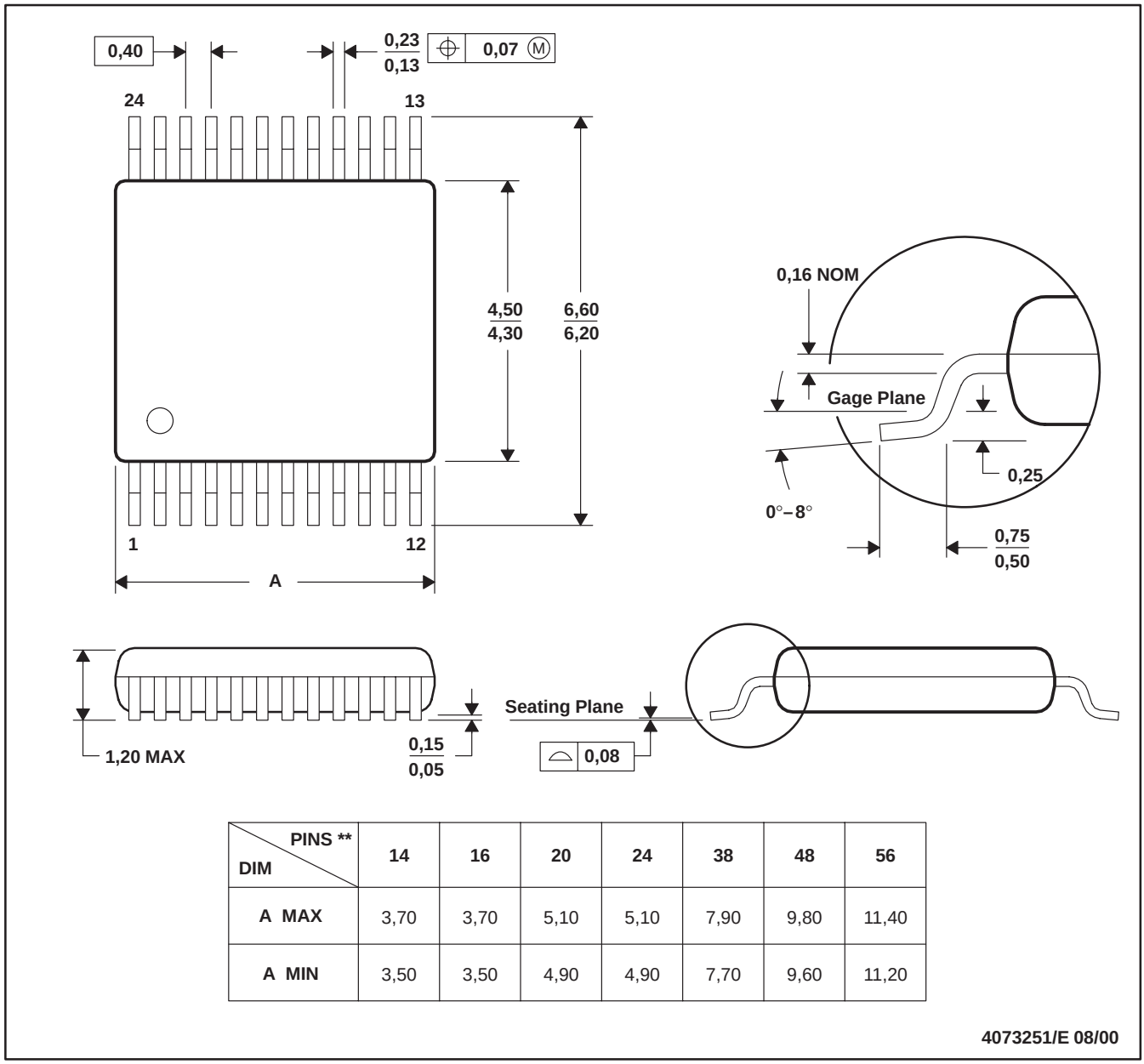


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3257DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

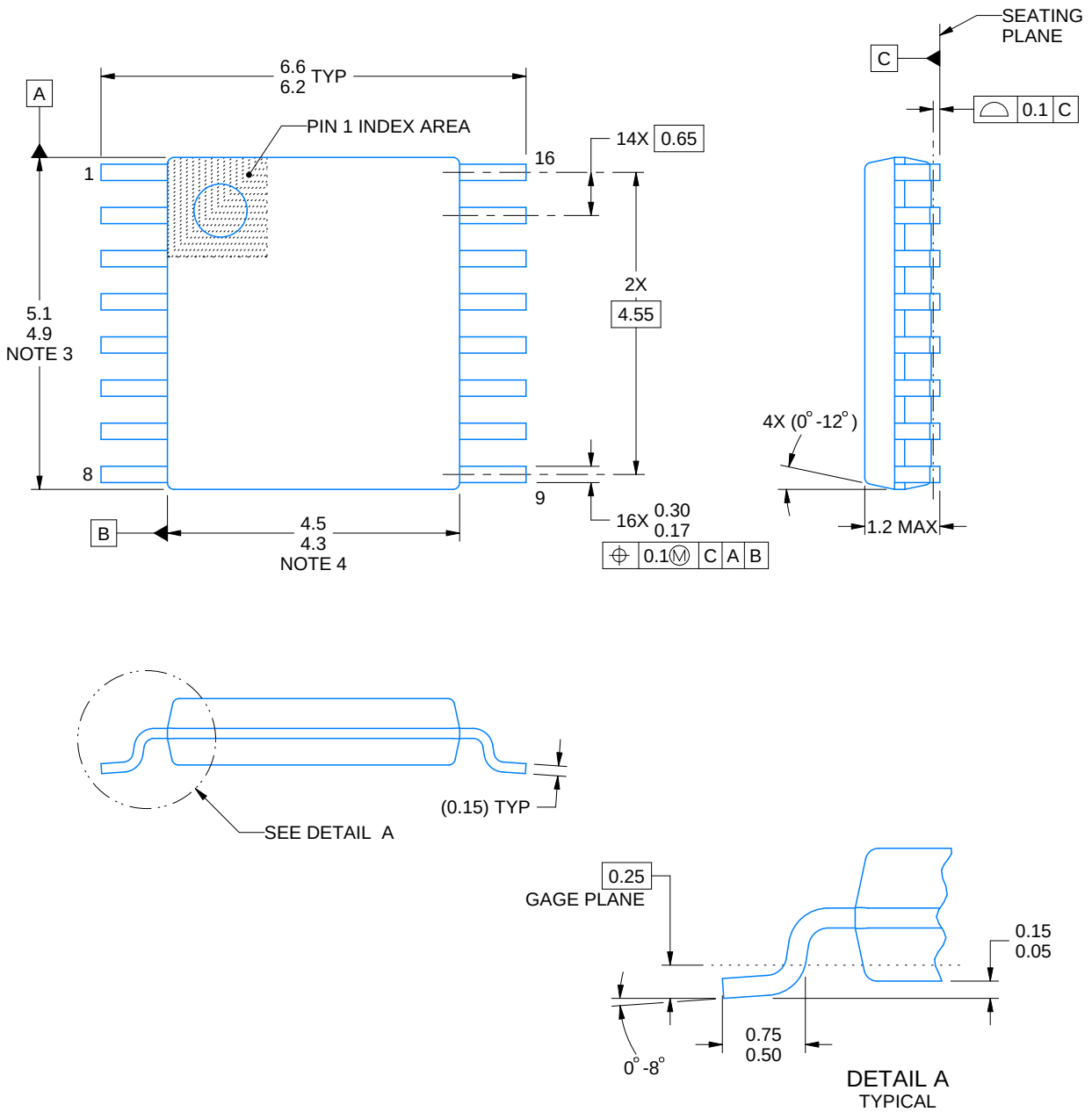
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

PW0016A

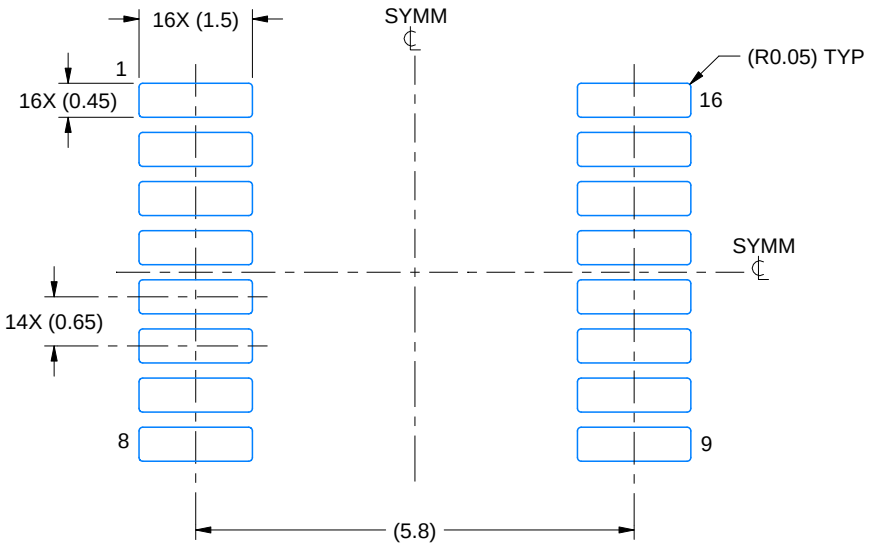
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



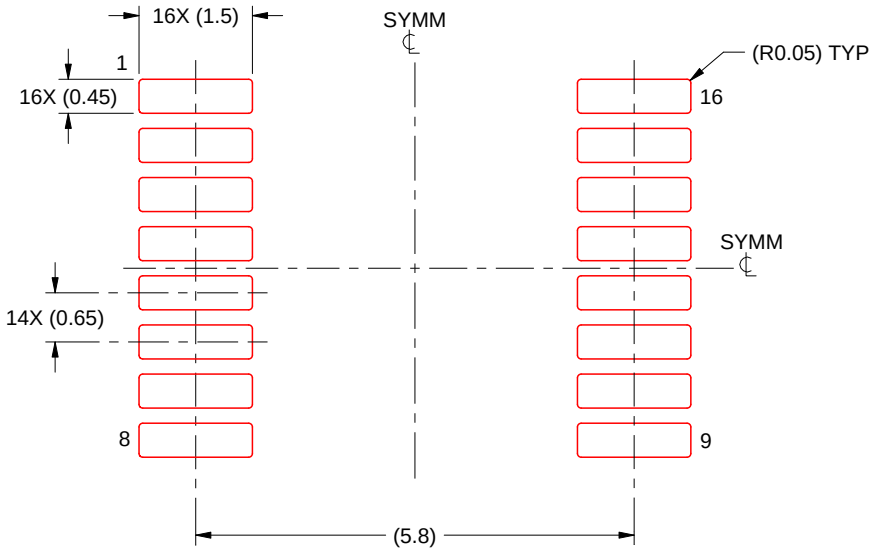
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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