

20 位 FET 总线开关

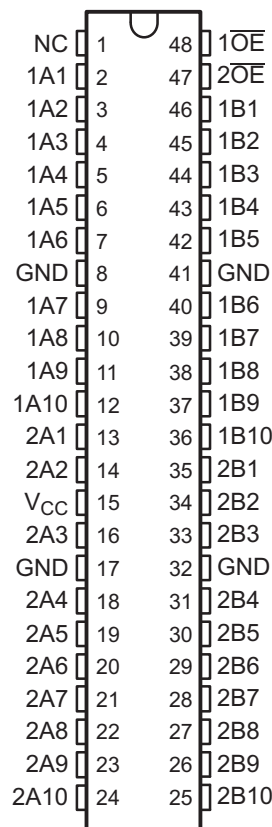
具有 5 V 容限电平转换器的 2.5 V/3.3 V 低电压总线开关

查询样品: [SN74CB3T16210-Q1](#)

特性

- 符合汽车应用要求
- 德州仪器 (TI) Widebus Widebus™ 系统的成员
- 输出电压转换跟踪 V_{CC}
- 在所有数据 I/O 端口上支持混合模式信号运行
 - 通过 3.3 V V_{CC} 提供 5 V 输入与低至 3.3 V 的输出电平转换
 - 通过 2.5 V V_{CC} 提供 5 V/3.3 V 输入与低至 2.5 V 的输出电平转换
- 支持器件上电与断电的 5 V 容限 I/O
- 支持近零传播延迟的双向数据流
- 低导通阻抗 (r_{on}) 特性 ($r_{on} = 5 \Omega$ 典型值)
- 低输入 / 输出电容可最大限度地减少加载 ($C_{io(OFF)} = 5 \text{ pF}$ 典型值)
- 数据与控制输入提供下冲钳位二极管
- 低功耗
 - ($I_{CC} = 40 \mu\text{A}$ 最大值)
- V_{CC} 工作电压范围: 2.3 V 至 3.6 V
- 数据 I/O 支持 0 至 5 V 信号级 (0.8 V、1.2 V、1.5 V、1.8 V、2.5 V、3.3 V、5 V)
- 可通过 TTL 或 5 V/3.3 V CMOS 输出驱动控制输入
- I_{off} 支持部分断电模式工作
- 支持数字应用: 电平转换、PCI 接口、USB 接口、存储器交错以及总线隔离
- 是低功耗便携式应用的理想选择

DGG 封装
(顶视图)



NC - No internal connection

说明 / 订购信息

SN74CB3T16210-Q1 是支持低导通电阻 (r_{on}) 并兼容于 TTL 的高速 FET 总线开关, 支持最小传播延迟。该器件提供可跟踪 V_{CC} 的电压转换, 能够在所有数据 I/O 端口上全面支持混合模式信号运行。SN74CB3T16210-Q1 支持采用 5 V TTL、3.3 V LVTTTL 与 2.5 V CMOS 开关标准的系统以及用户定义开关电平 (见 Figure 1)。



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

说明/订购信息（继续）

SN74CB3T16210-Q1 可组成两个 10 位总线开关，能够提供具有分离式输出功能的 ($\overline{1OE}$, $\overline{2OE}$) 输入。它即可用作 2 个 10 位总线开关，也可用作 1 个 20 位总线开关。 $\overline{OE}$ 为低时，相关 10 位总线开关打开，A 端口连接至 B 端口，可在两个端口之间实现双向数据流。 $\overline{OE}$ 为高时，相关 10 位总线开关关闭，A 与 B 端口之间存在高阻抗状态。

该器件专用于采用 I_{off} 的部分关断应用。 I_{off} 特性可在关断时防止损坏电流通过器件回流。该器件可在关闭时提供隔离。

要在上电或关断过程中确保高阻抗状态， $\overline{OE}$ 必须通过上拉电阻器由 V_{CC} 进行控制；驱动器电流吸收性能可检测电阻器的最小值。

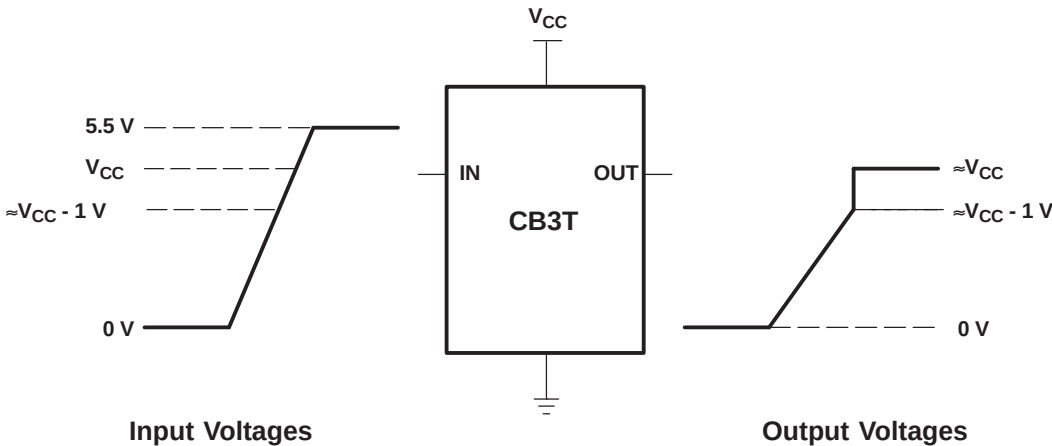
ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – DGG	Reel of 2000	CCB3T16210QDGGRQ1	CB3T16210Q

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(EACH 10-BIT BUS SWITCH)

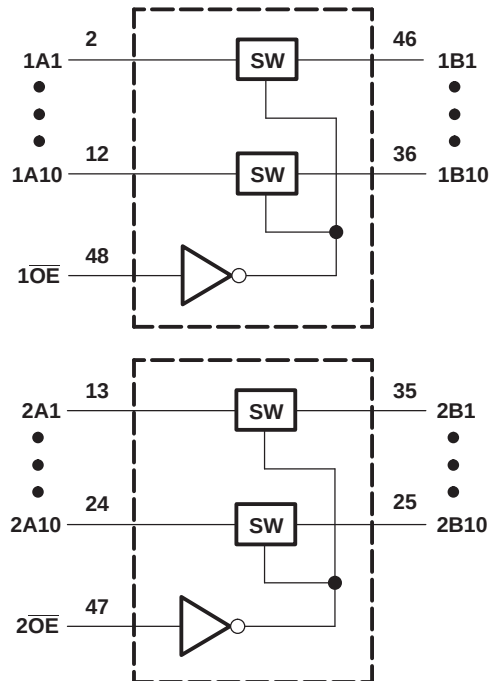
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect



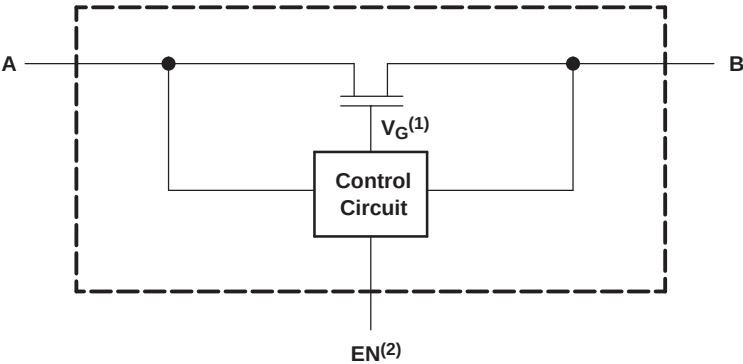
If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1\text{ V}$, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- (1) Gate voltage (V_G) is equal to approximately $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_{IN}	Control input voltage range ^{(2) (3)}	–0.5	7	V
$V_{I/O}$	Switch I/O voltage range ^{(2) (3) (4)}	–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50 mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50 mA
I_{IO}	ON-state switch current ⁽⁵⁾			±128 mA
Continuous current through V_{CC} or GND				±100 mA
θ_{JA}	Package thermal impedance ⁽⁶⁾	DGG package		70 °C/W
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V _{CC} = 2.7 V to 3.6 V	2	5.5	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		–40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

PARAMETER		TEST CONDITIONS	T _A = –40°C TO 125°C			UNIT
			MIN	TYP ⁽²⁾	MAX	
V _{IK}		V _{CC} = 3 V, I _I = –18 mA			–1.2	V
V _{OH}		See Figure 3 and Figure 4				
I _{IN}	Control inputs	V _{CC} = 3.6 V, V _{IN} = 3.6 V to 5.5 V or GND			±10	µA
I _I		V _{CC} = 3.6 V, Switch ON, V _{IN} = V _{CC} or GND	V _I = V _{CC} – 0.7 V to 5.5 V		±20	µA
			V _I = 0.7 V to V _{CC} – 0.7 V		–40	
			V _I = 0 to 0.7 V		±5	
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V, V _O = 0 to 5.5 V, V _I = 0, Switch OFF, V _{IN} = V _{CC} or GND			±10	µA
I _{off}		V _{CC} = 0, V _O = 0 to 5.5 V, V _I = 0,			10	µA
I _{CC}		V _{CC} = 3.6 V, I _{I/O} = 0, Switch ON or OFF, V _{IN} = V _{CC} or GND	V _I = V _{CC} or GND		40	µA
			V _I = 5.5 V		40	
ΔI _{CC} ⁽⁴⁾	Control inputs	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			300	µA
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND		4		pF
C _{io(OFF)}		V _{CC} = 3.3 V, V _{I/O} = 5.5 V, 3.3 V, or GND, Switch OFF, V _{IN} = V _{CC} or GND		5		pF
C _{io(ON)}		V _{CC} = 3.3 V, Switch ON, V _{IN} = V _{CC} or GND	V _{I/O} = 5.5 V or 3.3 V		5	pF
			V _{I/O} = GND		13	
r _{on} ⁽⁵⁾		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V, V _I = 0	I _O = 24 mA		5	Ω
			I _O = 16 mA		5	
		V _{CC} = 3 V, V _I = 0	I _O = 24 mA		5	
			I _O = 16 mA		5	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

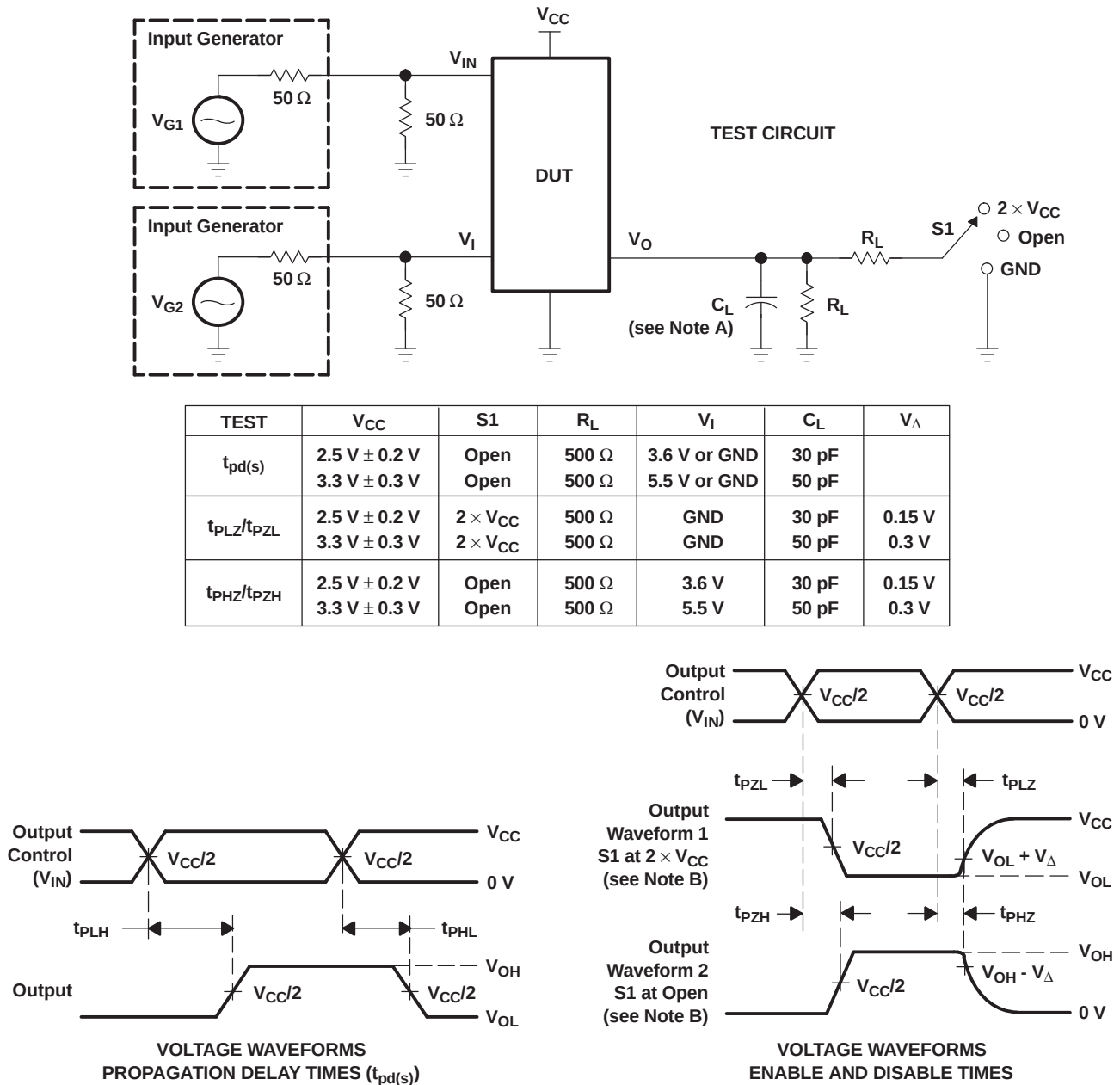
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

for $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{en}	$\overline{OE}$	A or B	1	14	1	12	ns
t_{dis}	$\overline{OE}$	A or B	1	9.5	1	10.5	ns

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

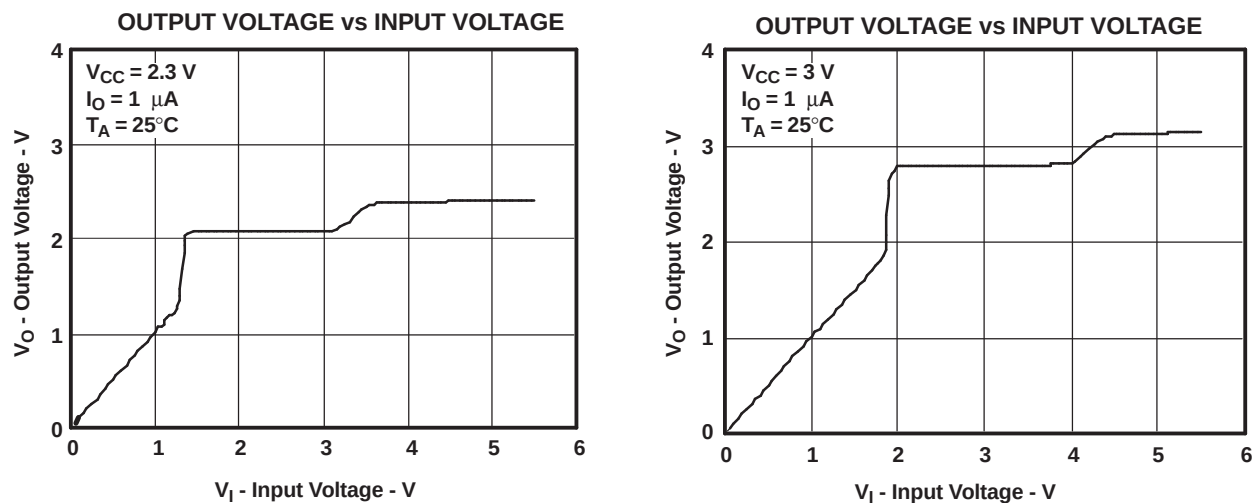


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS

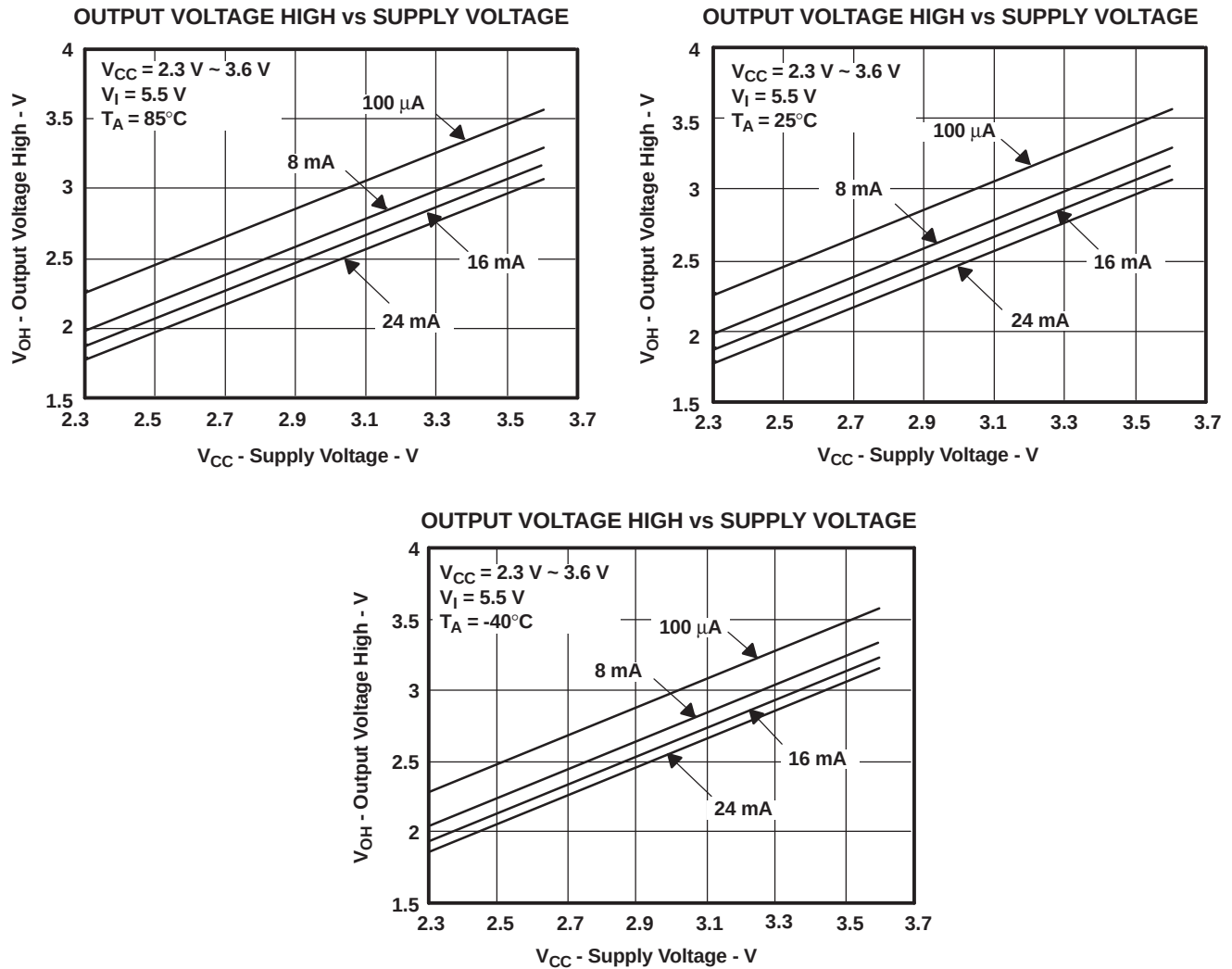


Figure 4. V_{OH} Values

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CCB3T16210QDGGRQ1	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CB3T16210Q
CCB3T16210QDGGRQ1.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CB3T16210Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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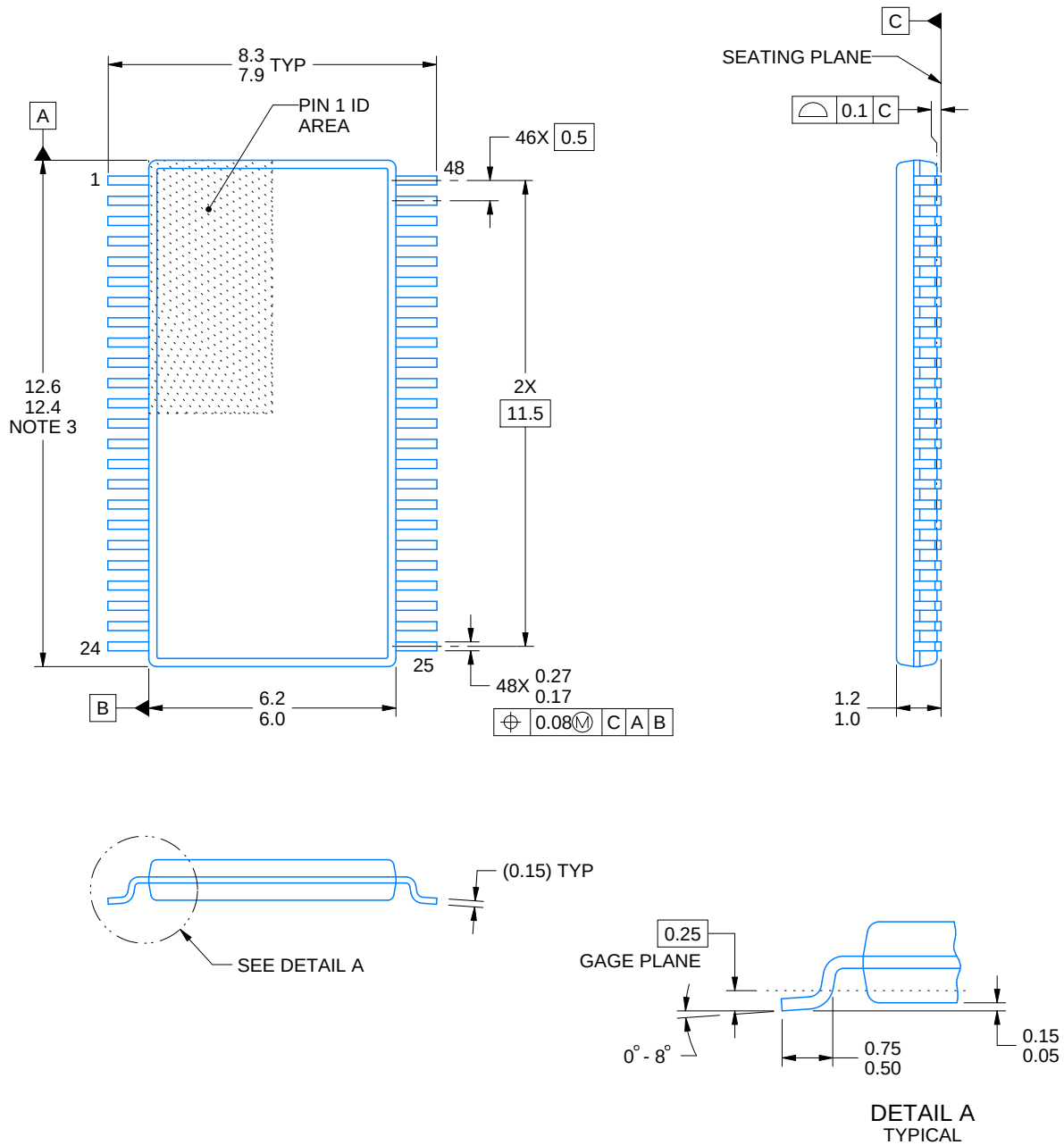
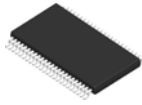
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OTHER QUALIFIED VERSIONS OF SN74CB3T16210-Q1 :

- Catalog : [SN74CB3T16210](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



4214859/B 11/2020

NOTES:

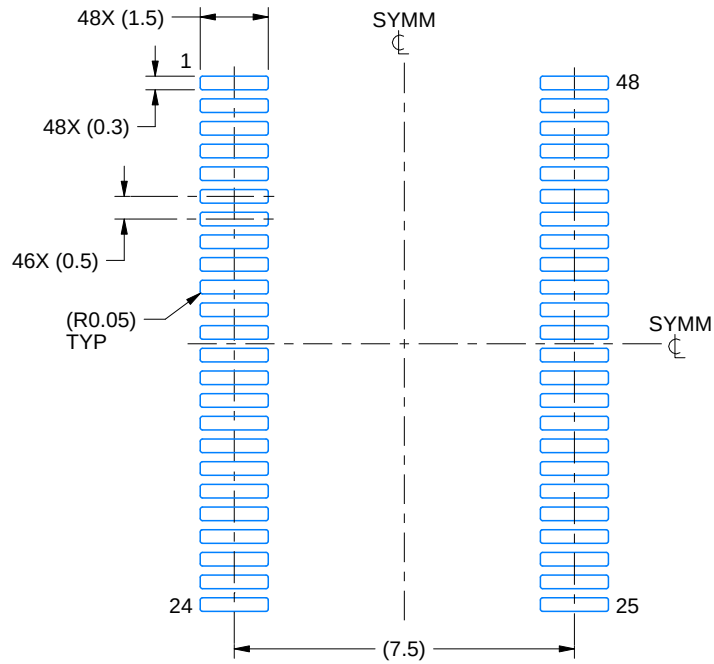
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

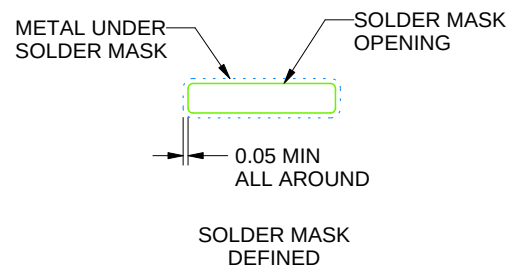
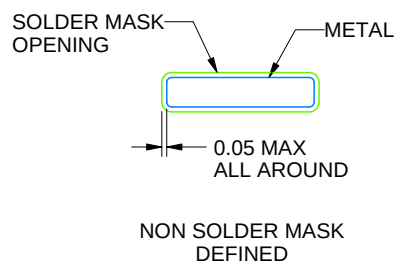
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

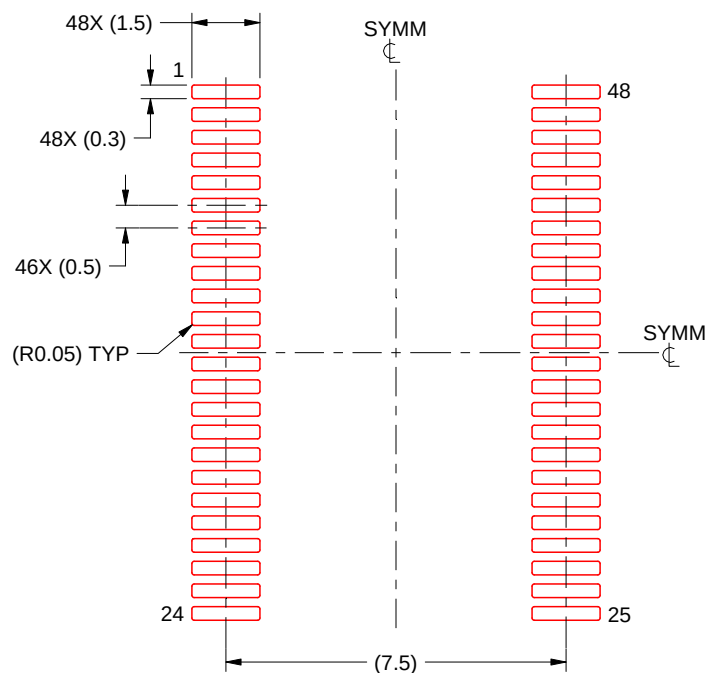
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

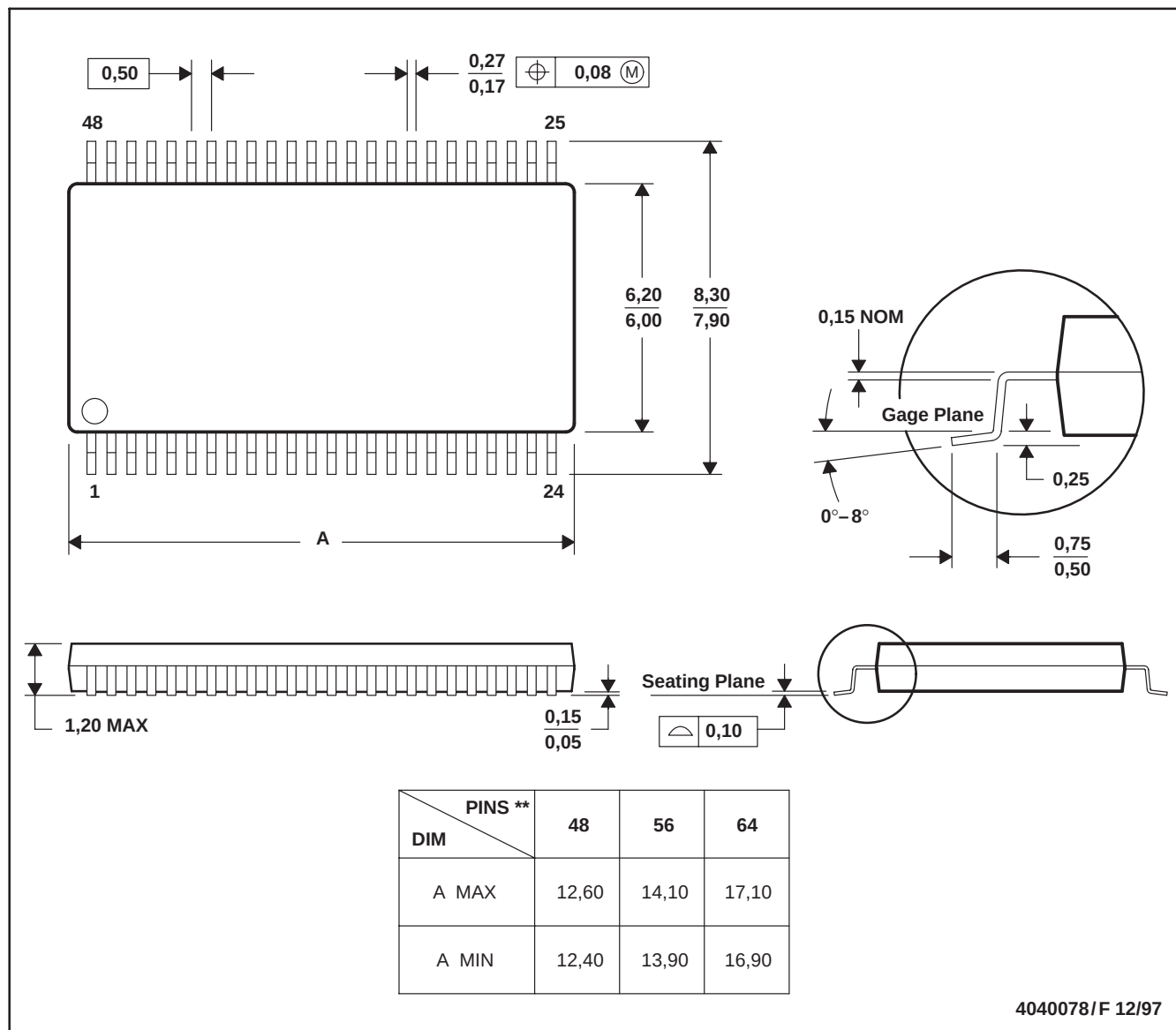
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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