双 FET 总线开关 2.5V/3.3V 低压高带宽总线开关

查询样片: **SN74CB3Q3306A-EP**

特性

- 高带宽数据路径（高达 **500MHz**[(1)]）
- 支持器件加电与断电的 **5V** 容限 **I/O**
- 工作范围内低且平的导通状态电阻 (r_{on}) 特性
  （r_{on} = 4Ω 典型值）
- 数据 **I/O** 端口上的轨到轨切换
  - **3.3V** V_{CC} 时的 **0** 至 **5V** 切换
  - **2.5V** V_{CC} 时的 **0** 至 **3.3V** 切换
- 支持近零传播延迟的双向数据流
- 低输入/输出电容最大限度地减少加载和信号失真
  （$C_{io(OFF)}$ = 3.5pF 典型值）
- 快速开关频率（$f_{\overline{OE}}$ = **20MHz** 最大值）
- 数据与控制输入提供下冲钳位二极管
- 低功耗（I_{CC} = 0.25mA 典型值）
- **2.3V** 至 **3.6V** 的 V_{CC} 工作电压范围
- 数据 **I/O** 支持 **0** 至 **5 V** 信号传输级
  (0.8V，1.2V，1.5V，1.8V，2.5V，3.3V，5V）
- 控制输入可由 **TTL** 或
  5V/3.3V CMOS 输出驱动
- I_{off} 支持部分断电模式工作

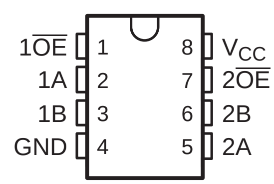
(1) 要获得与 CB3Q 系列性能特点相关的额外信息，请参考 TI 应用报告，《*CBT-C，CB3T 和 CB3Q 信号开关系列*》，文献编号 SCDA008。

- 锁断性能超过 **100mA**
  符合 **JESD 78**，**II** 类规范的要求
- 静电放电 **(ESD)** 性能测试符合 **JESD 22** 标准
  - **2000V** 人体模型
    （**A114-B**，**II** 类）
  - **1000V** 充电器件模型 **(C101)**
- 支持数字和模拟应用：**USB** 接口，差分信号接口，总线隔离，低失真信号选通

支持国防、航空航天、和医疗应用

- 受控基线
- 同一组装和测试场所
- 同一制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

PW PACKAGE
(TOP VIEW)



订购信息

T_J	封装[(1)]		可订购器件型号	正面标记	VID 号
-55°C 至 125°C	薄型小外形尺寸封装 (TSSOP)-PW	管	CCB3Q3306AMPWEP	U306AM	V62/14606-01XE-T
		卷带	CCB3Q3306AMPWREP		V62/14606-01XE

(1) 封装图示、标准包装数量、散热数据、符号以及印刷电路板 (PCB) 设计指南可从以下网址内获得 www.ti.com/sc/package。

English Data Sheet: SCDS352

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明

SN74CB3Q3306A 是一款高带宽 FET 总线开关，此开关利用一个电荷泵来提升导通晶体管的栅极电压，从而提供一个低平的导通状态电阻 (r_{on})。 低平导通状态电阻可实现最小传播延迟，并且支持数据输入/输出 (I/O) 端口上的轨到轨切换。 此器件还特有低数据 I/O 电容，以最大限度地减少数据总线上的电容负载和信号失真。 专门设计用于支持高带宽应用，SN74CB3Q3306A 提供非常适合于宽带通信、网络互联、以及数据密集型计算系统的经优化的接口解决方案。

SN74CB3Q3306A 可组成两个 1 位开关，此开关具有分离输出使能 (1$\overline{OE}$，2$\overline{OE}$) 输入。 它即可用作 2 个 1 位总线开关，也可用作 1 个 2 位总线开关。 当 $\overline{OE}$ 为低电平时，相关 1 位总线开关打开，并且 A 端口被连接至 B 端口，从而实现两个端口之间的双向数据流。 当 $\overline{OE}$ 为高电平时，相关 1 位总线开关关闭，并且在 A 与 B 端口之间存在高阻抗状态。

该器件完全符合使用 I_{off} 的部分断电应用的规范要求。 I_{off} 电路可防止在器件断电时电流回流对器件造成损坏。 该器件可在关闭时提供隔离。

为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸入能力来决定。

Table 1. FUNCTION TABLE (EACH BUS SWITCH)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)

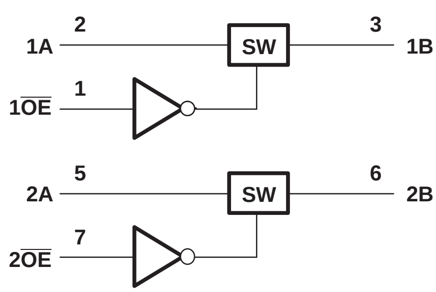
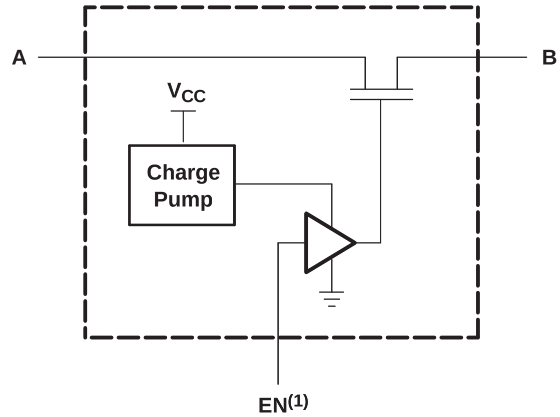


Figure 1. SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS[1]

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range[2] [3]		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current[5]			±64	mA
	Continuous current through each V_{CC} or GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

THERMAL INFORMATION

THERMAL METRIC[1]		SN74CB3Q3306A-EP PW 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	190.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	74	
θ_{JB}	Junction-to-board thermal resistance[4]	119.4	
ψ_{JT}	Junction-to-top characterization parameter[5]	12	
ψ_{JB}	Junction-to-board characterization parameter[6]	117.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_J	Operating junction temperature		–55	125	°C

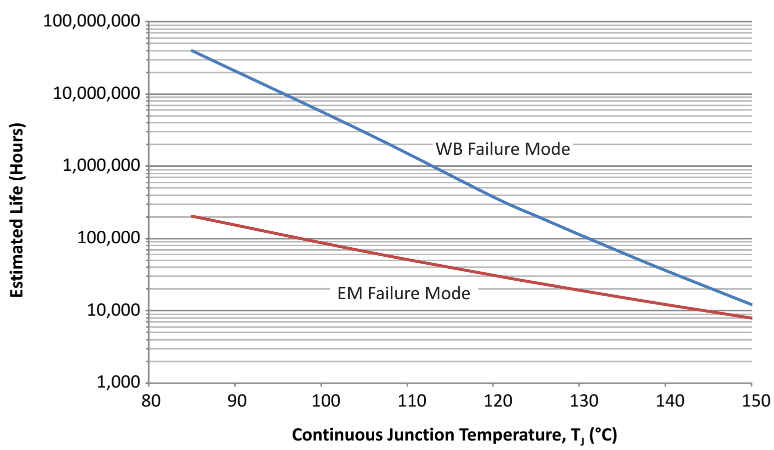
(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS(1)

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = –18 mA					–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					±1	μA
I_{OZ} (3)		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC}				±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND			0.25	0.7	mA
ΔI_{CC} (4)	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND	T_J = -55°C to 85°C			25	μA
					T_J = 125°C			36	
I_{CCD} (5)	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,				0.03		mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0				2.5		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC},	$V_{I/O}$ = 5.5 V, 3.3 V, or 0			3.5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0			8		pF
r_{on} (6)		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA	T_J = -55°C to 85°C		4	8	Ω
					T_J = 125°C			10	
			V_I = 1.7 V,	I_O = –15 mA	T_J = -55°C to 85°C		5	9	
					T_J = 125°C			58	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA	T_J = -55°C to 85°C		4	6	
					T_J = 125°C			8	
			V_I = 2.4 V,	I_O = –15 mA	T_J = -55°C to 85°C		5	8	
					T_J = 125°C			66	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
(3) Enhanced plastic product disclaimer applies.

Figure 2. SN74CB3Q3306A-EP Operating Life Derating Chart

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted) (see Figure 5)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ (1)		$\overline{OE}$	A or B		10		20	MHz
t_{pd} (2)	T_J = -55° to 85°C	A or B	B or A		0.2		0.3	ns
	T_J = 125°C				1.2		2.3	
t_{en}		$\overline{OE}$	A or B	1.5	12	1.5	10	ns
t_{dis}		$\overline{OE}$	A or B	1	14	1	9	ns

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

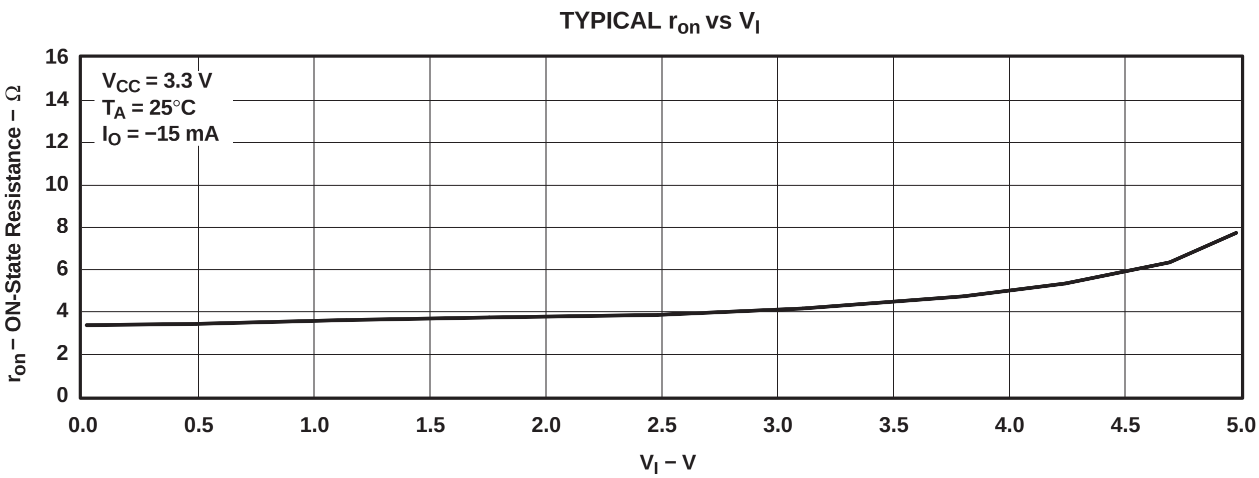


Figure 3. Typical r_{on} vs V_I

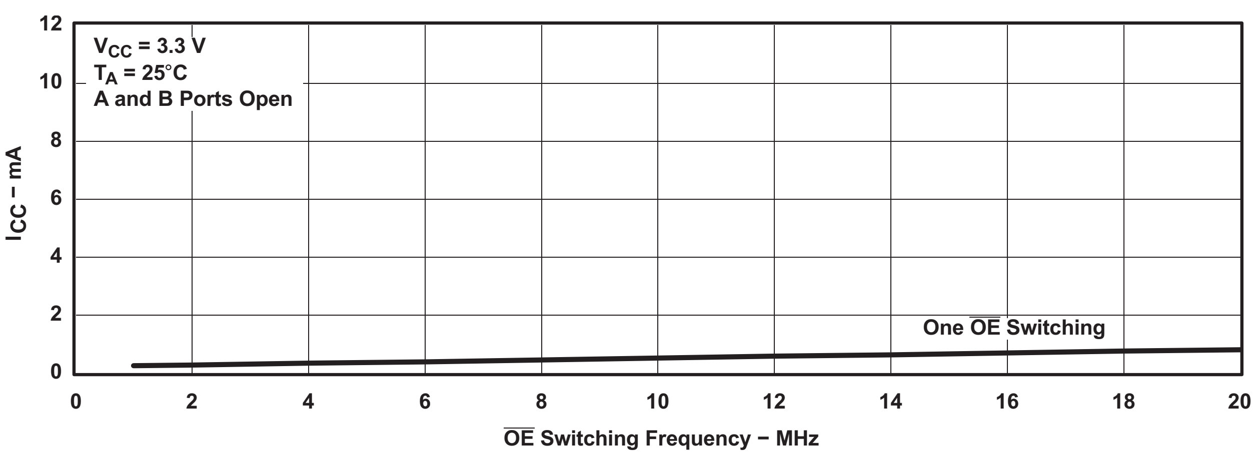
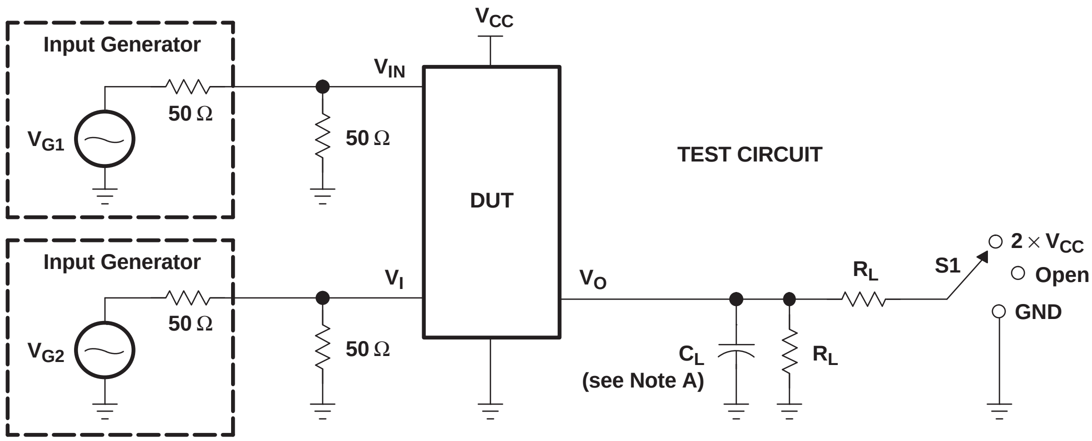
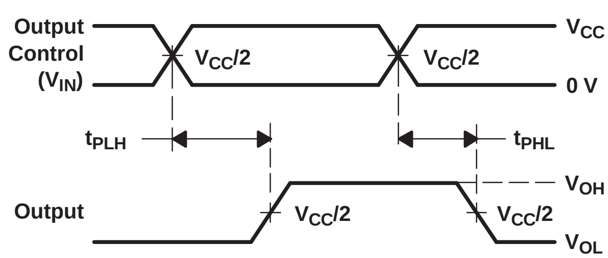


Figure 4. Typical I_{CC} vs $\overline{OE}$ Switching Frequency

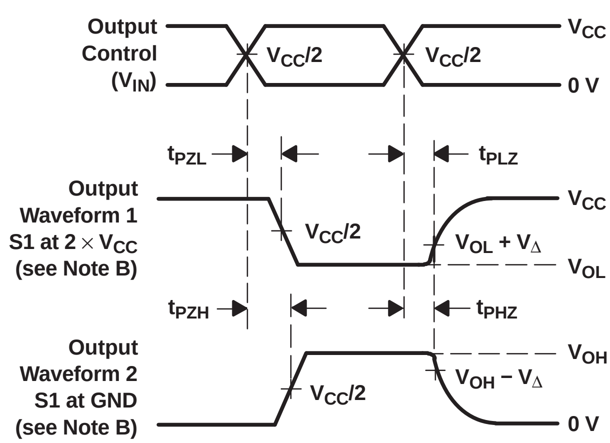
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CCB3Q3306AMPWEP	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
CCB3Q3306AMPWREP	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
V62/14606-01XE	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
V62/14606-01XE-T	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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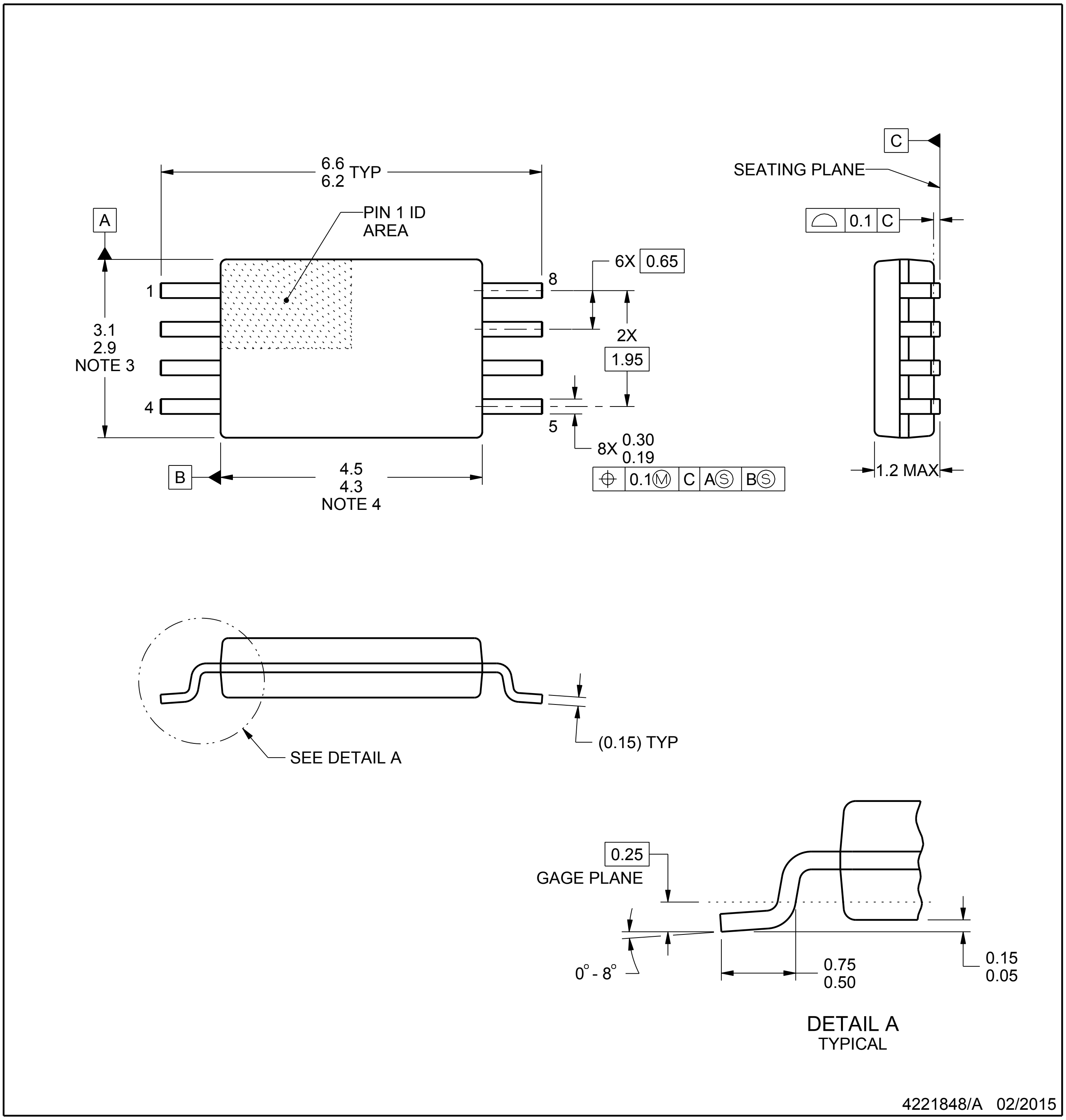
OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A-EP :

- Catalog : SN74CB3Q3306A

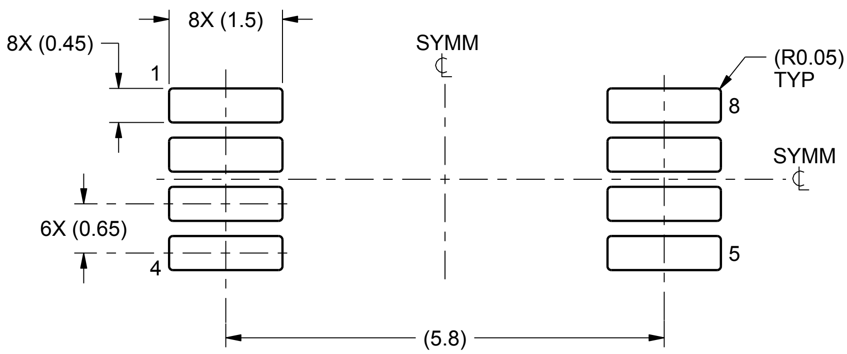
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

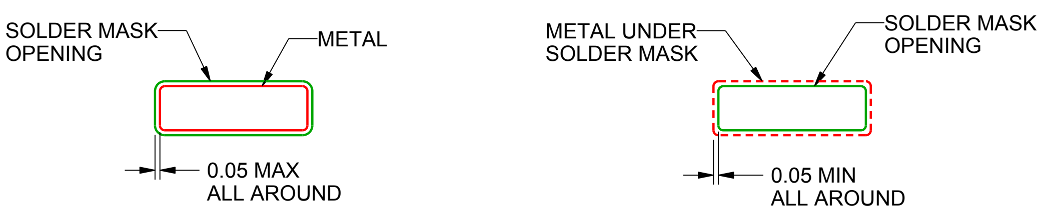


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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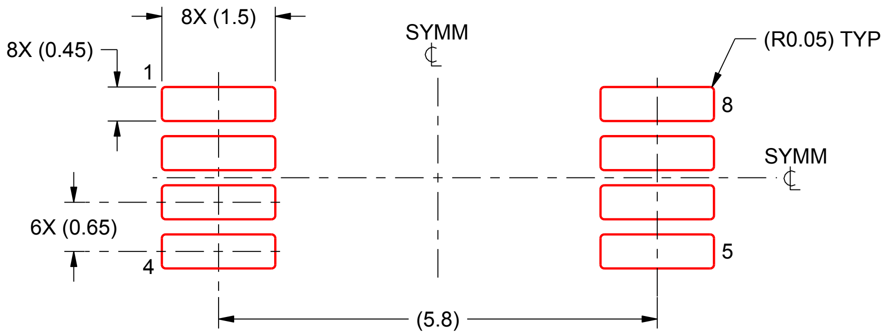
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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