

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Dynamic Output Control (DOC™) Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCB} Voltage
- If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B-port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCBH164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCBH164245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCB} .

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCBH164245GR	AVCBH164245
	TVSOP – DGV	Tape and reel	SN74AVCBH164245VR	WBH4245
	VFBGA – GQL	Tape and reel	SN74AVCBH164245KR	WBH4245
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74AVCBH164245ZQLR	WBH4245

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

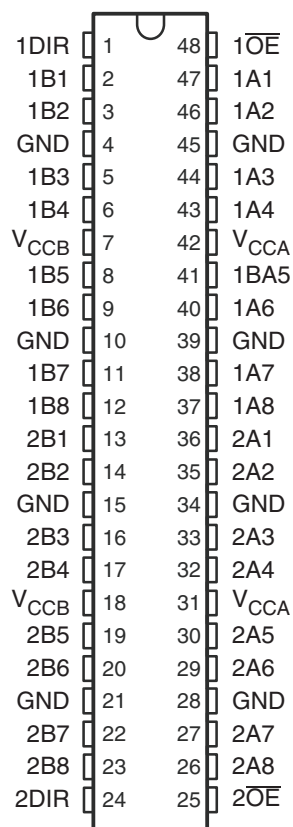


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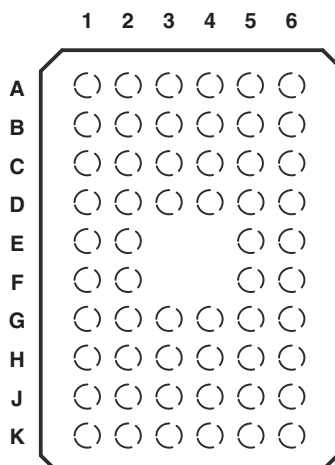
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TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)



GQL/ZQL PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS
(56-Ball GQL/ZQL Package)⁽¹⁾

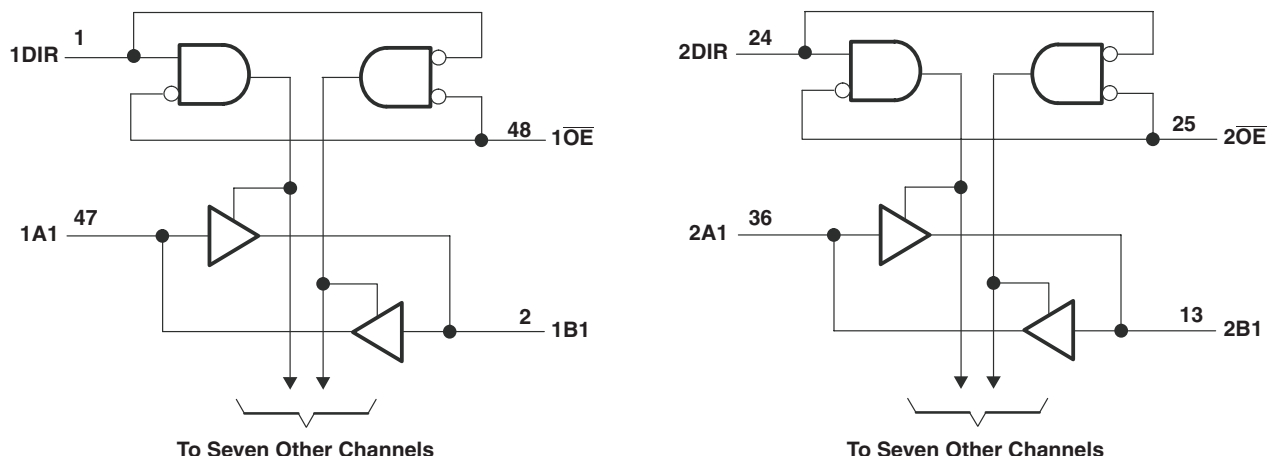
	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1OE
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	VCCB	VCCA	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

(1) NC - No internal connection

**FUNCTION TABLE
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	I/O ports (A port)	-0.5	4.6
		I/O ports (B port)	-0.5	4.6
		Control inputs	-0.5	4.6
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	4.6
		B port	-0.5	4.6
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	-0.5	$V_{CCA} + 0.5$
		B port	-0.5	$V_{CCB} + 0.5$
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CCA} , V_{CCB} , or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DGV package	58	
		GQL/ZQL package	28	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.4	3.6	V
V _{CCB}	Supply voltage				1.4	3.6	V
V _{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _{IH}	High-level input voltage	Control inputs (referenced to V _{CCB})	1.4 V to 1.95 V		V _{CCB} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Control inputs (referenced to V _{CCB})	1.4 V to 1.95 V		V _{CCB} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.4 V to 1.6 V	−2		mA
				1.65 V to 1.95 V	−4		
				2.3 V to 2.7 V	−8		
				3 V to 3.6 V	−12		
I _{OL}	Low-level output current			1.4 V to 1.6 V	2		mA
				1.65 V to 1.95 V	4		
				2.3 V to 2.7 V	8		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T _A	Operating free-air temperature				−40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.(2) V_{CCO} is the V_{CC} associated with the data output port.(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	MIN TYP ⁽³⁾ MAX	UNIT
V _{OH}		I _{OH} = −100 μA	V _I = V _{IH}	1.4 V to 3.6 V	1.4 V to 3.6 V	V _{CCO} − 0.2	V
		I _{OH} = −2 mA	V _I = V _{IH}	1.4 V	1.4 V	1.05	
		I _{OH} = −4 mA	V _I = V _{IH}	1.65 V	1.65 V	1.2	
		I _{OH} = −8 mA	V _I = V _{IH}	2.3 V	2.3 V	1.75	
		I _{OH} = −12 mA	V _I = V _{IH}	3 V	3 V	2.3	
V _{OL}		I _{OH} = 100 μA	V _I = V _{IL}	1.4 V to 3.6 V	1.4 V to 3.6 V	0.2	V
		I _{OH} = 2 mA	V _I = V _{IL}	1.4 V	1.4 V	0.35	
		I _{OH} = 4 mA	V _I = V _{IL}	1.65 V	1.65 V	0.45	
		I _{OH} = 8 mA	V _I = V _{IL}	2.3 V	2.3 V	0.55	
		I _{OH} = 12 mA	V _I = V _{IL}	3 V	3 V	0.7	
I _I	Control inputs	V _I = V _{CCB} or GND		1.4 V to 3.6 V	3.6 V	±2.5	μA
I _{BHL} ⁽⁴⁾		V _I = 0.49 V		1.4 V	1.4 V	11	μA
		V _I = 0.57 V		1.65 V	1.65 V	25	
		V _I = 0.7 V		2.3 V	2.3 V	45	
		V _I = 0.8 V		3 V	3 V	75	
I _{BHH} ⁽⁵⁾		V _I = 0.49 V		1.4 V	1.4 V	−11	μA
		V _I = 0.57 V		1.65 V	1.65 V	−25	
		V _I = 0.7 V		2.3 V	2.3 V	−45	
		V _I = 0.8 V		3 V	3 V	−75	
I _{BHLO} ⁽⁶⁾		V _I = 0 to V _{CC}		1.6 V	1.6 V	100	μA
				1.95 V	1.95 V	200	
				2.7 V	2.7 V	300	
				3.6 V	3.6 V	525	
I _{BHHO} ⁽⁷⁾		V _I = 0 to V _{CC}		1.6 V	1.6 V	−100	μA
				1.95 V	1.95 V	−200	
				2.7 V	2.7 V	−300	
				3.6 V	3.6 V	−525	
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V	±10	μA
	B port			0 to 3.6 V	0 V	±10	
I _{OZ} ⁽⁸⁾	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{OE}$ = V _{IH}	3.6 V	3.6 V	±12.5	μA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V	±12.5	
	A port			3.6 V	0 V	±12.5	
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0		1.6 V	1.6 V	20	μA
				1.95 V	1.95 V	20	
				2.7 V	2.7 V	30	
				0 V	3.6 V	−40	
				3.6 V	0 V	40	
				3.6 V	3.6 V	40	

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

(3) All typical values are at T_A = 25°C.

(4) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

(5) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

(6) An external driver must source at least I_{BHLO} to switch this node from low to high.

(7) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(8) For I/O ports, the parameter I_{OZ} includes the input leakage current.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP ⁽³⁾	MAX	UNIT
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.6 V	1.6 V			20	μA
			1.95 V	1.95 V			20	
			2.7 V	2.7 V			30	
			0 V	3.6 V			40	
			3.6 V	0 V			–40	
			3.6 V	3.6 V			40	
C _i	Control inputs	V _I = 3.3 V or GND	3.3 V	3.3 V		4		pF
C _{io}	A or B ports	V _O = 3.3 V or GND	3.3 V	3.3 V		5		pF

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t _{en}	$\overline{OE}$	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t _{dis}	$\overline{OE}$	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.15.1	1.6	4.8	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t _{en}	$\overline{OE}$	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t _{dis}	$\overline{OE}$	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t _{en}	$\overline{OE}$	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t _{dis}	$\overline{OE}$	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	$\overline{OE}$	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

OPERATING CHARACTERISTICS

V_{CCA} and $V_{CCB} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	20	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

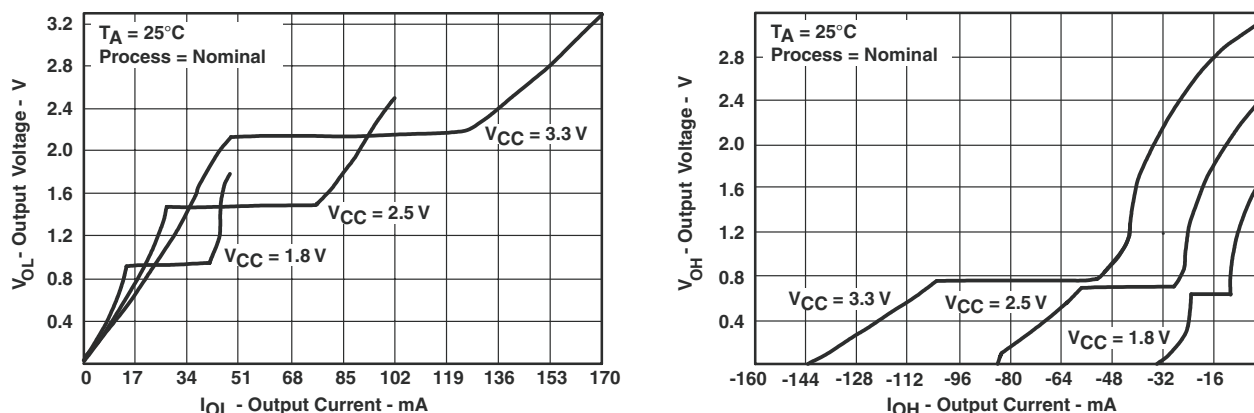
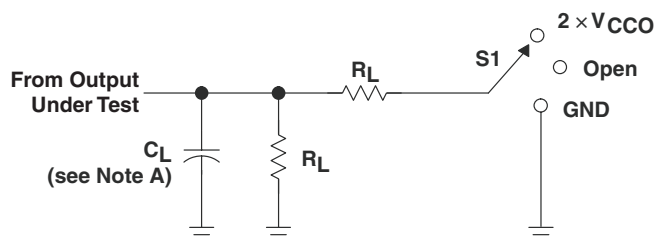


Figure 1. Typical Output Voltage vs Output Current

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
$1.5\text{ V} \pm 0.1\text{ V}$	15 pF	2 k Ω	0.1 V
$1.8\text{ V} \pm 0.15\text{ V}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	30 pF	500 Ω	0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

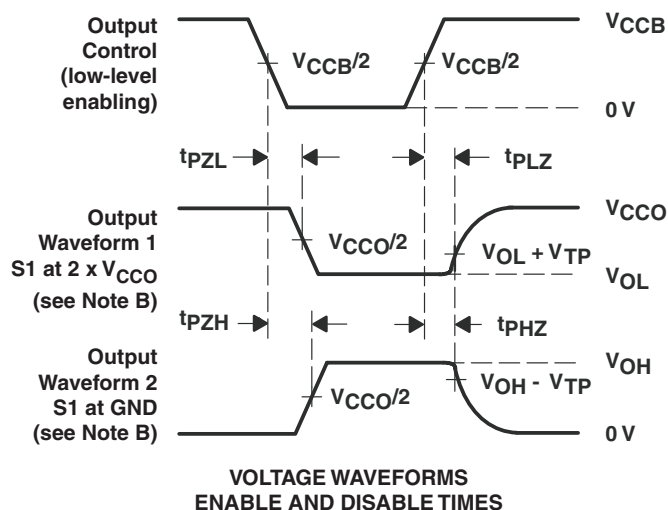
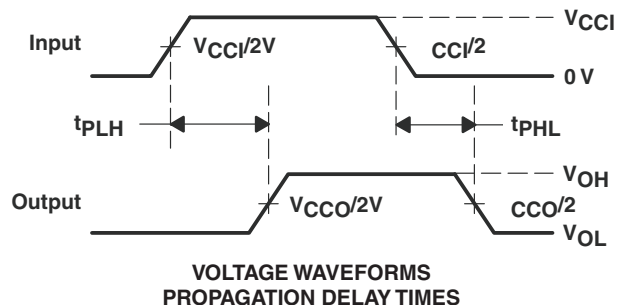
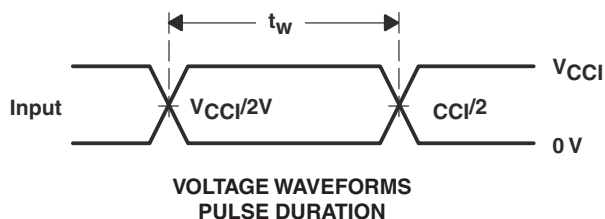


Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AVCBH164245GRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCBH164245
74AVCBH164245GRG4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCBH164245
SN74AVCBH164245GR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCBH164245
SN74AVCBH164245GR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCBH164245
SN74AVCBH164245VR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WBH4245
SN74AVCBH164245VR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WBH4245

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

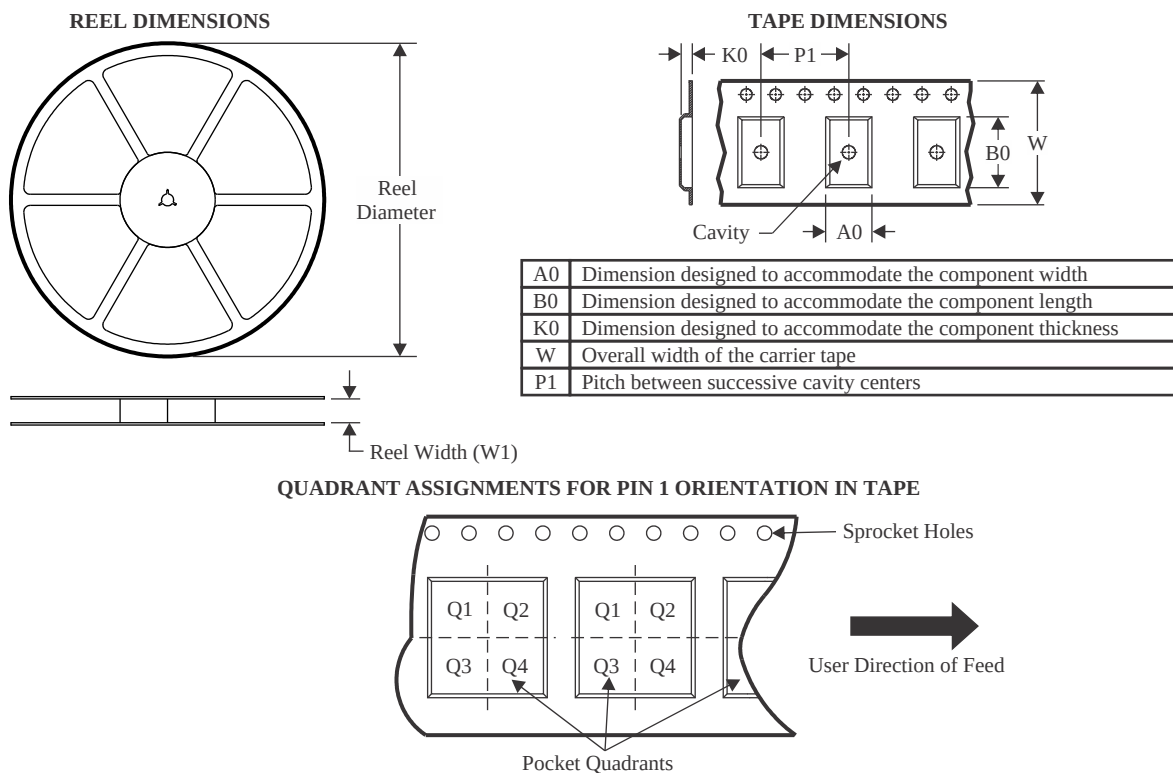
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

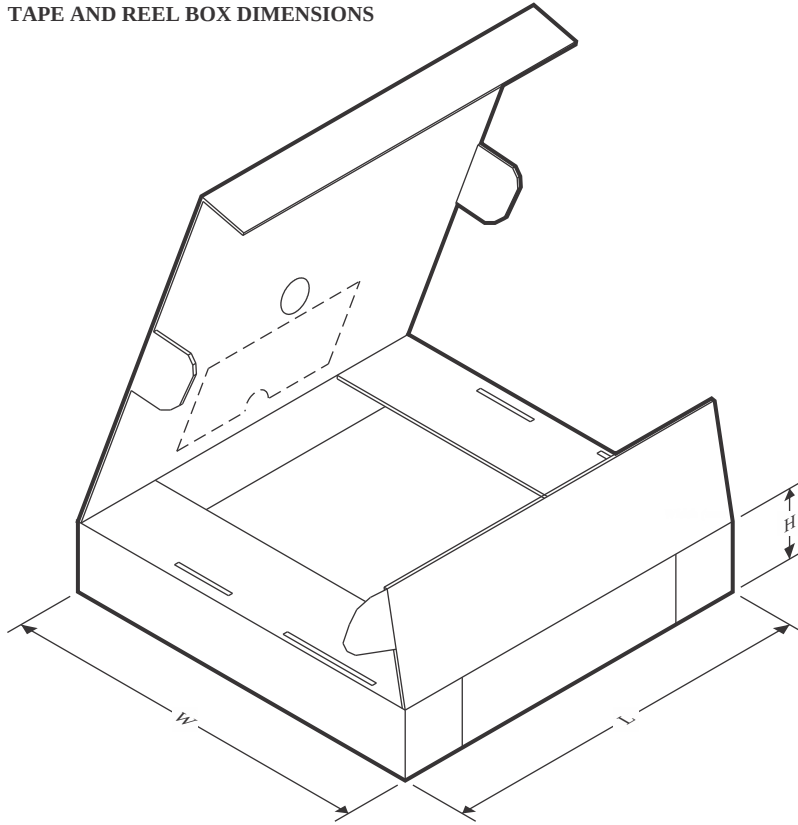
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCBH164245GRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVCBH164245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVCBH164245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



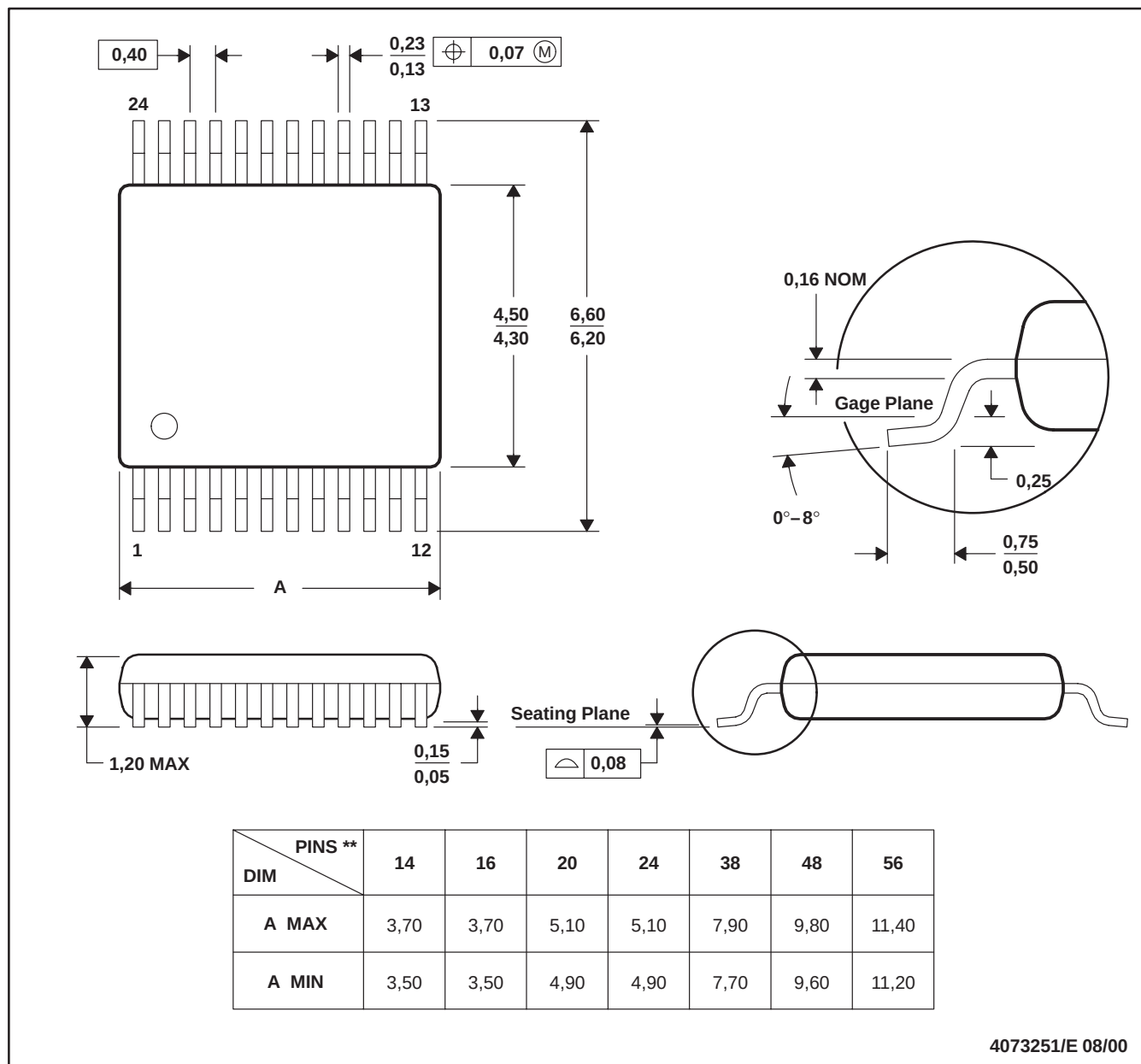
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCBH164245GRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AVCBH164245GR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AVCBH164245VR	TVSOP	DGV	48	2000	353.0	353.0	32.0

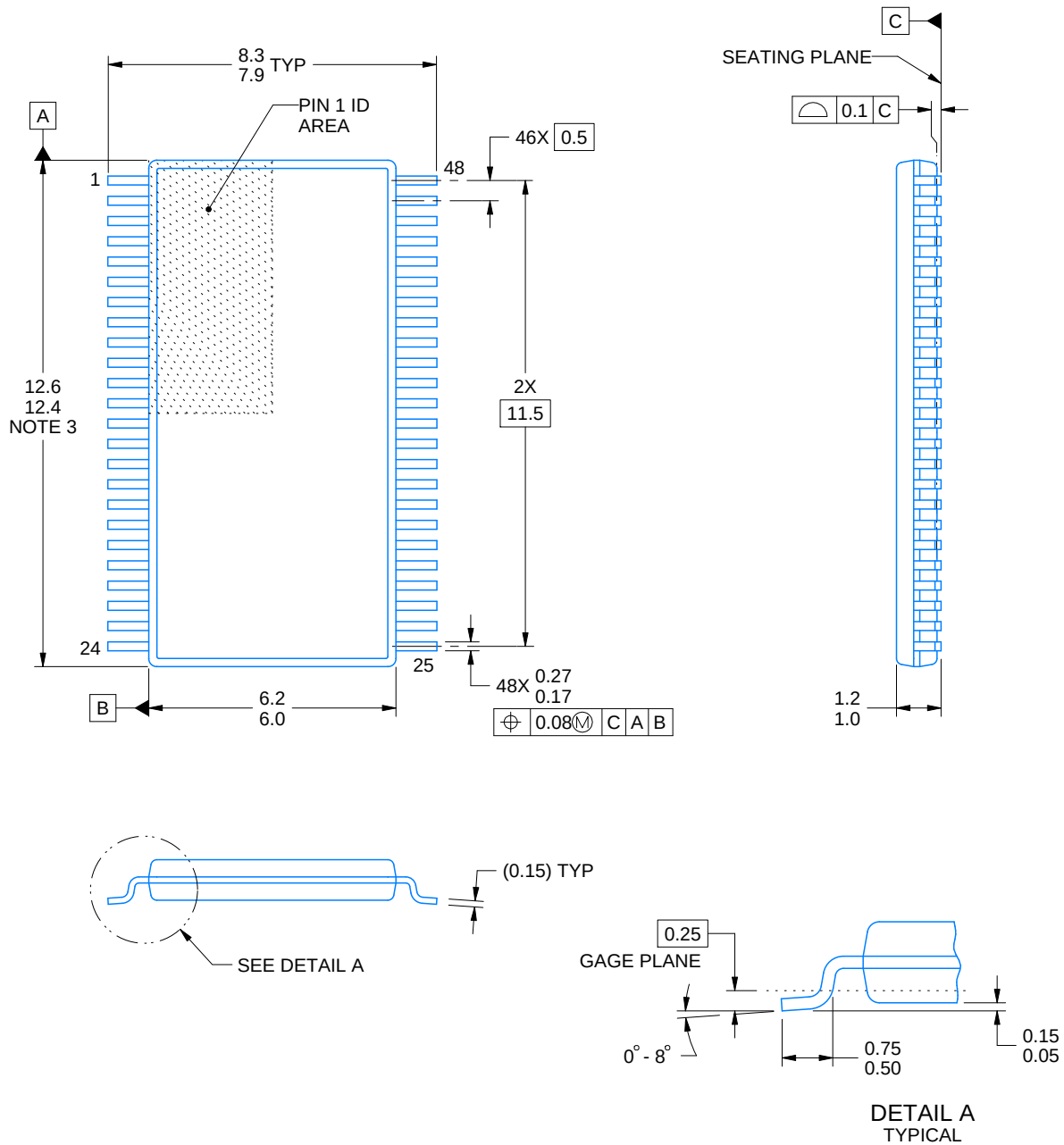
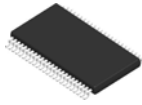
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

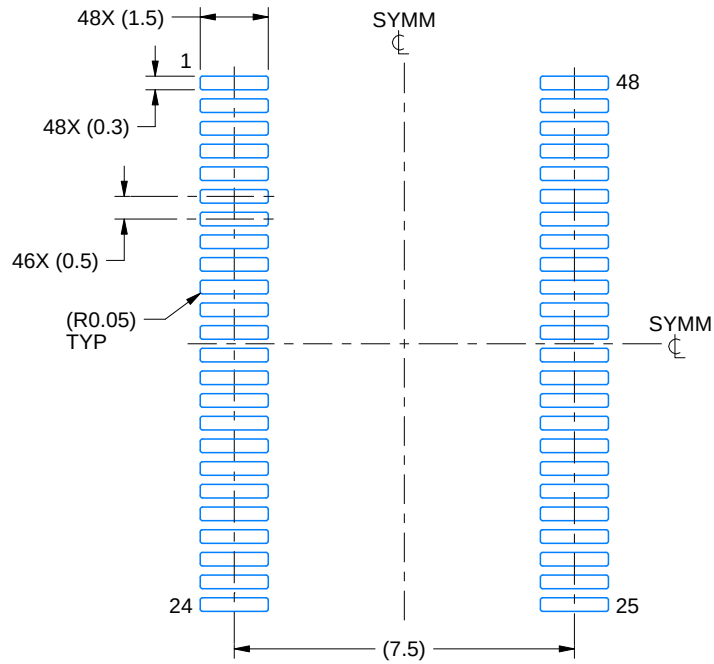
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

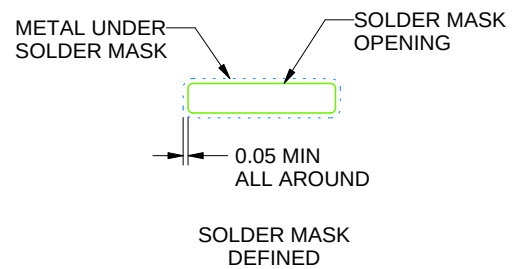
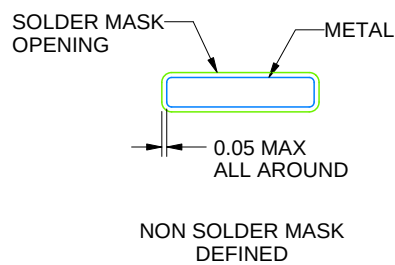
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

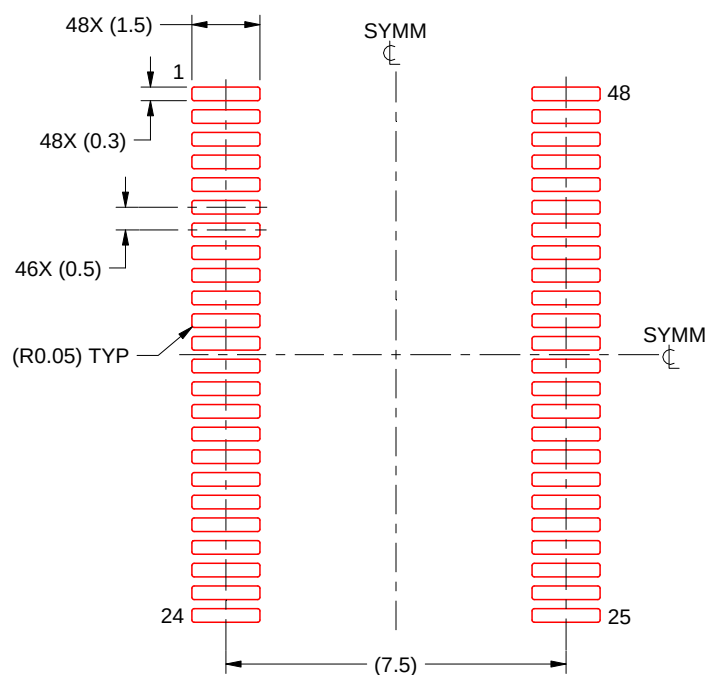
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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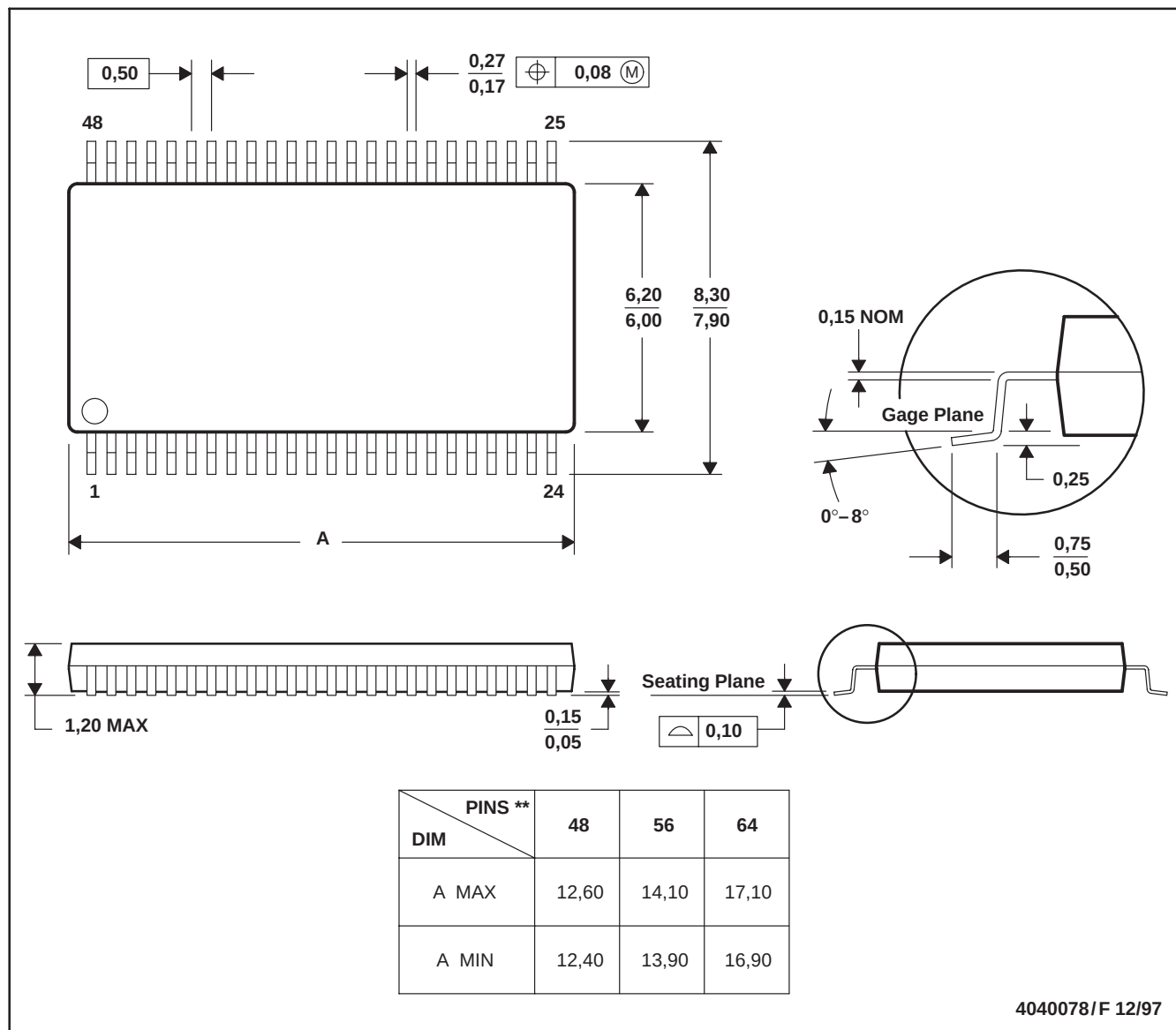
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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