# SN74AUP1T97 具有九个可配置门逻辑功能的单电源电压电平转换器

## 1 特性

- 可采用德州仪器 (TI) 的 NanoStar™ 封装
- 单电源电压转换器
- 1.8V 至 3.3V ( $V_{CC}$=3.3V 时 )
- 2.5V 至 3.3V ( $V_{CC}$=3.3V 时 )
- 1.8V 至 2.5V ( $V_{CC}$=2.5V 时 )
- 3.3V 至 2.5V ( $V_{CC}$ = 2.5V 时 )
- 九个可配置的门逻辑功能
- 施密特触发器输入可抑制输入噪声并提供更佳的输出信号完整性
- $I_{off}$ 支持局部断电模式，具有低泄漏电流 (0.5μA)
- 超低的静态和动态功耗
- 可提供无铅封装：SON ( DRY 或 DSF )、SOT-23 (DBV)、SC-70 (DCK) 和 NanoStar WCSP
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型{13} ( A114-B，II 类 )
  - 1000V 充电器件模型 (C101)
- 相关器件：SN74AUP1T98、SN74AUP1T57 和 SN74AUP1T58

## 2 说明

AUP 技术是业内功耗超低的逻辑技术，适用于电池供电或带有备用电池的设备。SN74AUP1T97 专门用于逻辑电平转换应用，其输入转换电平可接受 1.8V 的 LVCMOS 信号，同时可由单个 3.3V 或 2.5V V{17}CC{18} 电源供电。

利用 2.3V 至 3.6V 的宽 $V_{CC}$ 范围，可在系统运行期间实现电池压降，并确保在该范围内正常运行。

施密特触发器输入 ( 正负输入转换之间的 $\Delta V_T$=210mV ) 改进了开关转换期间的抗扰度，这对于模拟混合模式设计十分有用。施密特触发器输入抑制输入噪声、确保输出信号的完整性并可实现慢输入信号转换。

通过将 A、B 和 C 输入连接到 $V_{CC}$ 或接地，可轻松将 SN74AUP1T97 配置为执行所需的门功能 ( 请参阅功能选择表 )。最多可执行九个常用的逻辑门功能。

$I_{关闭}$特性可实现省电条件 ($V_{CC}$=0V)，这在便携式和移动应用中十分重要。当 $V_{CC}$=0V 时，介于 0V 至 3.6V 范围内的信号可被施加到器件的输入和输出上。在这些条件下，不会对器件造成损坏。

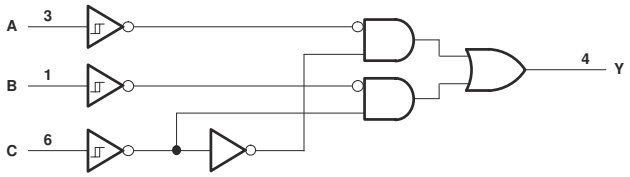
SN74AUP1T97 经设计优化具有 4mA 电流驱动能力，可减少由高驱动输出导致的线路反射、过冲和下冲。

NanoStar 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

**器件信息**

| 器件型号 | 封装(1) | 封装尺寸 ( 标称值 ) |
|---|---|---|
| SN74AUP1T97DBV | SOT-23 (6) | 2.9mm x 1.6mm |
| SN74AUP1T97DCK | SC70 (6) | 2.0mm x 1.25mm |
| SN74AUP1T97DRY | SON (6) | 1.45mm x 1.0mm |
| SN74AUP1T97DSF | SON (6) | 1.0mm x 1.0mm |
| SN74AUP1T97YFP | DSBGA (6) | 1.0mm x 1.4mm |
| SN74AUP1T97YZP | DSBGA (6) | 1.75mm x 1.25mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




逻辑图 ( 正逻辑 )

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (May 2010) to Revision J (September 2020) | Page |
|---|---|
| • 添加了*器件信息* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 | 1 |
| • 删除了*器件信息* 表，请参阅数据表末尾的*机械、封装和可订购信息* | 1 |
| • 更新了整个文档的表、图和交叉参考的编号格式 | 1 |


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## 4 Pin Configuration and Functions

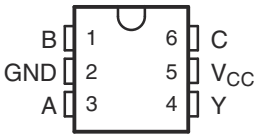


**图 4-1. DBV OR DCK Package 6-Pin SOT-23 or SC70 Top View**

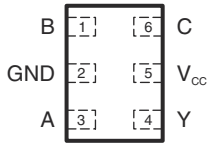


**图 4-2. DRY OR DSF Package 6-Pin SON Top View**

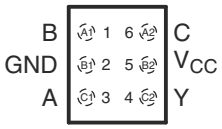


**图 4-3. YFP OR YZP Package 6-Pin DSBGA Top View**

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.6 | V |
| $V_O$ | Output voltage range in the high or low state(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±20 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

See(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | –3.1 | mA |
| | | $V_{CC}$ = 3 V | | –4 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 3.1 | mA |
| | | $V_{CC}$ = 3 V | | 4 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.


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## 5.4 Thermal Information

| THERMAL METRIC[1] | | SN74AUP1T97 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRY (SON) | DSF (SON) | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 165 | 259 | 340 | 300 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | | | | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | | | | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | | | | | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | | | | | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | | | | | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Thermal Information

| THERMAL METRIC[1] | | SN74AUP1T97 | | UNIT |
|---|---|---|---|---|
| | | YFP (DSBGA) | YZP (DSBGA) | |
| | | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 123 | 123 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | | | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | | | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | | | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 2.3 V to 2.7 V | 0.6 | | 1.1 | 0.6 | 1.1 | V |
| | | 3 V to 3.6 V | 0.75 | | 1.16 | 0.75 | 1.19 | |
| $V_{T-}$ Negative-going input threshold voltage | | 2.3 V to 2.7 V | 0.35 | | 0.6 | 0.35 | 0.6 | V |
| | | 3 V to 3.6 V | 0.5 | | 0.85 | 0.5 | 0.85 | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 2.3 V to 2.7 V | 0.23 | | 0.6 | 0.1 | 0.6 | V |
| | | 3 V to 3.6 V | 0.25 | | 0.56 | 0.15 | 0.56 | |
| $V_{OH}$ | $I_{OH}$ = –20 µA | 2.3 V to 3.6 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | V |
| | $I_{OH}$ = –2.3 mA | 2.3 V | 2.05 | | | 1.97 | | |
| | $I_{OH}$ = –3.1 mA | | 1.9 | | | 1.85 | | |
| | $I_{OH}$ = –2.7 mA | 3 V | 2.72 | | | 2.67 | | |
| | $I_{OH}$ = –4 mA | | 2.6 | | | 2.55 | | |
| $V_{OL}$ | $I_{OL}$ = 20 µA | 2.3 V to 3.6 V | | | 0.1 | | 0.1 | V |

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### 5.6 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| | | $I_{OL}$ = 2.3 mA | 2.3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 3.1 mA | | | | 0.44 | | 0.45 | |
| | | $I_{OL}$ = 2.7 mA | 3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 4 mA | | | | 0.44 | | 0.45 | |
| $I_I$ | All inputs | $V_I$ = 3.6 V or GND | 0 V to 3.6 V | | | 0.1 | | 0.5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V | | | 0.1 | | 0.5 | µA |
| $\Delta I_{off}$ | | $V_I$ or $V_O$ = 3.6 V | 0 V to 0.2 V | | | 0.2 | | 0.5 | µA |
| $I_{CC}$ | | $V_I$ = 3.6 V or GND, $I_O$ = 0 | 2.3 V to 3.6 V | | | 0.5 | | 0.9 | µA |
| $\Delta I_{CC}$ | | One input at 0.3 V or 1.1 V, Other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 2.3 V to 2.7 V | | | | | 4 | µA |
| | | One input at 0.45 V or 1.2 V, Other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 3 V to 3.6 V | | | | | 12 | |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.5 | | | | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 3.3 V | | 3 | | | | pF |

### 5.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V, $V_I$ = 1.8 V ± 0.15 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 1.8 | 2.3 | 2.9 | 0.5 | 6.8 | ns |
| | | | 10 pF | 2.3 | 2.8 | 3.4 | 1 | 7.9 | |
| | | | 15 pF | 2.6 | 3.1 | 3.8 | 1 | 8.7 | |
| | | | 30 pF | 3.8 | 4.4 | 5.1 | 1.5 | 10.8 | |

### 5.8 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V, $V_I$ = 2.5 V ± 0.2 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 1.8 | 2.3 | 3.1 | 0.5 | 6 | ns |
| | | | 10 pF | 2.2 | 2.8 | 3.5 | 1 | 7.1 | |
| | | | 15 pF | 2.6 | 3.2 | 5.2 | 1 | 7.9 | |
| | | | 30 pF | 3.7 | 4.4 | 5.2 | 1.5 | 10 | |

### 5.9 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V, $V_I$ = 3.3 V ± 0.3 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 2 | 2.7 | 3.5 | 0.5 | 5.5 | ns |


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### 5.9 Switching Characteristics (continued)

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V, $V_I$ = 3.3 V ± 0.3 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| | | | 10 pF | 2.4 | 3.1 | 3.9 | 1 | 6.5 | |
| | | | 15 pF | 2.8 | 3.5 | 4.3 | 1 | 7.4 | |
| | | | 30 pF | 4 | 4.7 | 5.5 | 1.5 | 9.5 | |

### 5.10 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $V_I$ = 1.8 V ± 0.15 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 1.6 | 2 | 2.5 | 0.5 | 8 | ns |
| | | | 10 pF | 2 | 2.4 | 2.9 | 1 | 8.5 | |
| | | | 15 pF | 2.3 | 2.8 | 3.3 | 1 | 9.1 | |
| | | | 30 pF | 3.4 | 3.9 | 4.4 | 1.5 | 9.8 | |

### 5.11 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $V_I$ = 2.5 V ± 0.2 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 1.6 | 1.9 | 2.4 | 0.5 | 5.3 | ns |
| | | | 10 pF | 2 | 2.3 | 2.7 | 1 | 6.1 | |
| | | | 15 pF | 2.3 | 2.7 | 3.1 | 1 | 6.8 | |
| | | | 30 pF | 3.4 | 3.8 | 4.2 | 1.5 | 8.5 | |

### 5.12 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $V_I$ = 3.3 V ± 0.3 V (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | 5 pF | 1.6 | 2.1 | 2.7 | 0.5 | 4.7 | ns |
| | | | 10 pF | 2 | 2.4 | 3 | 1 | 5.7 | |
| | | | 15 pF | 2.3 | 2.7 | 3.3 | 1 | 6.2 | |
| | | | 30 pF | 3.4 | 3.8 | 4.4 | 1.5 | 7.8 | |

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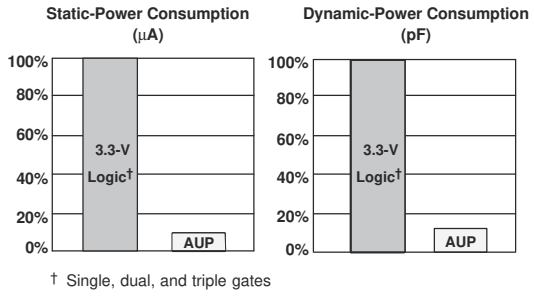
## 5.13 Operating Characteristics

$T_A$ = 25°C

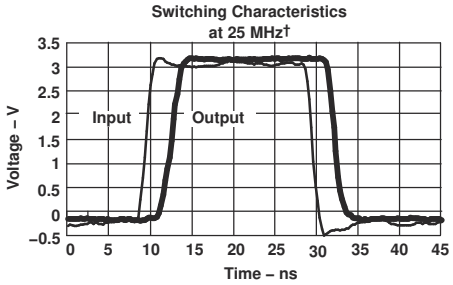
| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|
| | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 4 | 5 | pF |

## 5.14 Typical Characteristics




† Single, dual, and triple gates

**图 5-1. AUP – The Lowest-Power Family**




† AUP1G08 data at $C_L$ = 15 pF

**图 5-2. Excellent Signal Integrity**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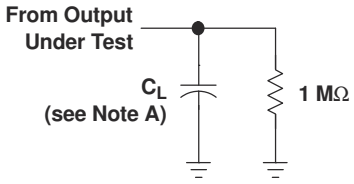
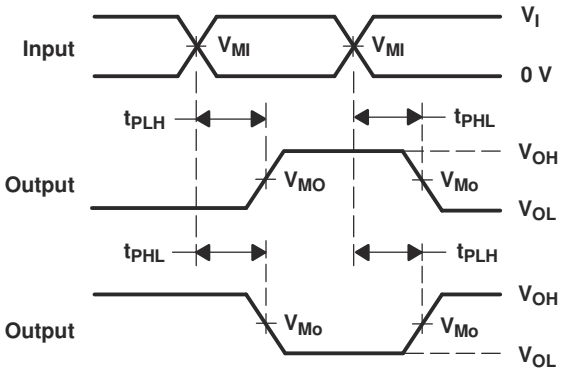
# 6 Parameter Measurement Information




LOAD CIRCUIT

| | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_{MI}$ | $V_I/2$ | $V_I/2$ |
| $V_{MO}$ | $V_{CC}/2$ | $V_{CC}/2$ |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**图 6-1. Load Circuit and Voltage Waveforms**

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# 7 Detailed Description

## 7.1 Functional Block Diagram

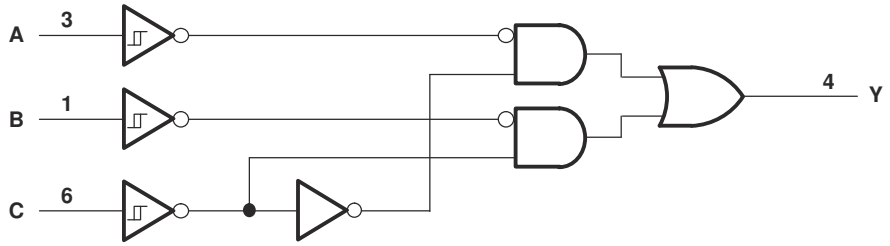


图 7-1. Logic Diagram (Positive Logic)

## 7.2 Feature Description

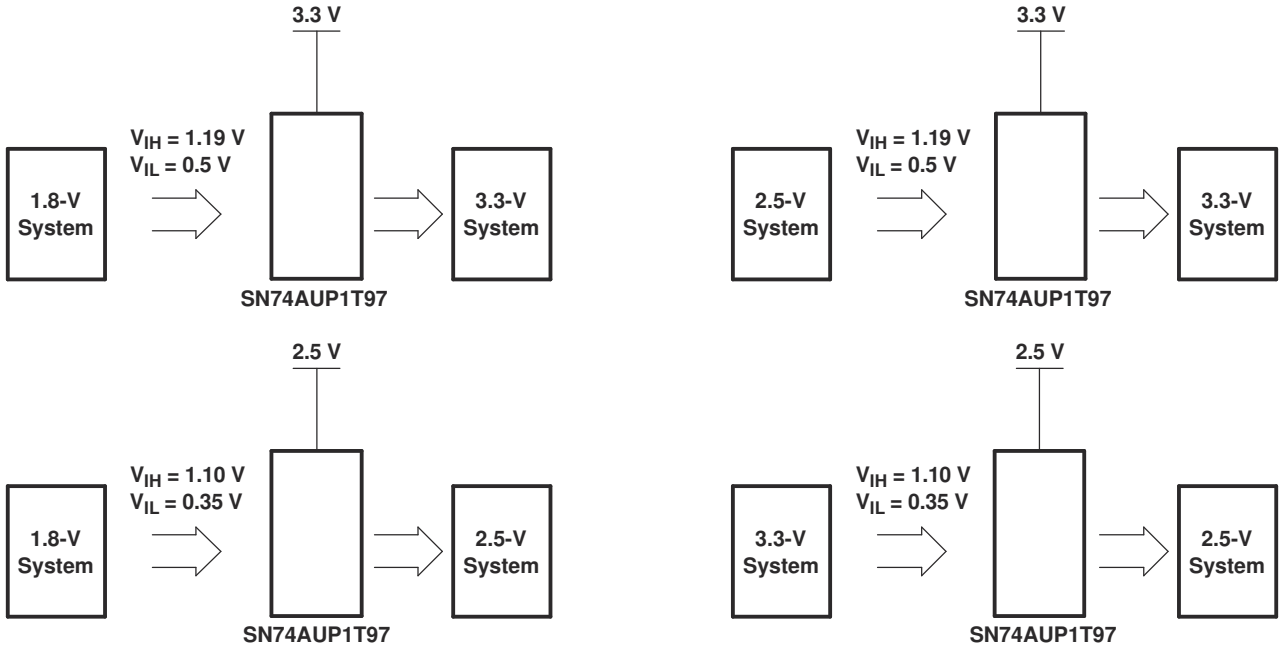


图 7-2. Possible Voltage-Translation Combinations

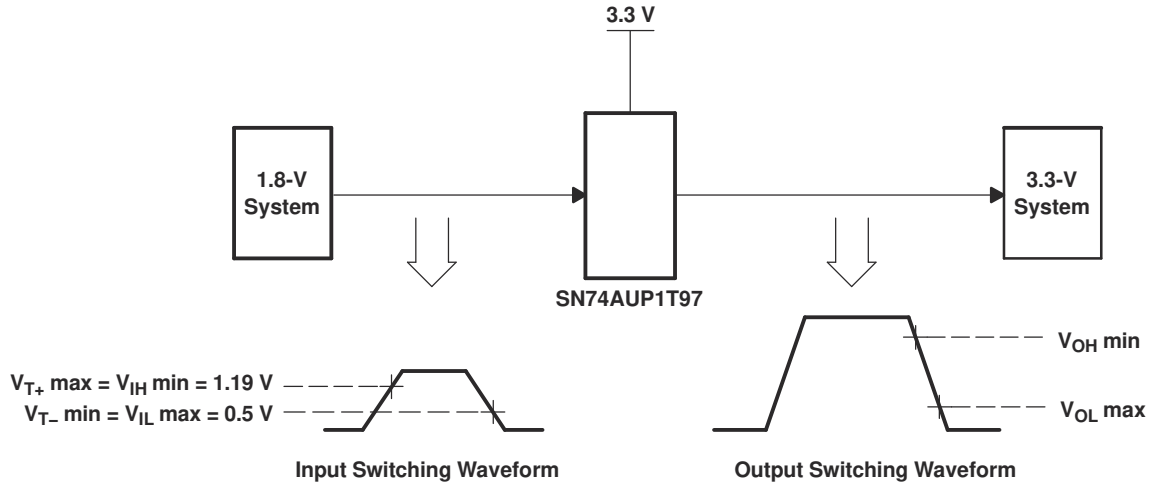


图 7-3. Switching Thresholds for 1.8-V to 3.3-V Translation


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## 7.3 Device Functional Modes

表 7-1 lists the functional modes of the SN74AUP1T97.

**Table 7-1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| C | B | A | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

### 7.3.1 Logic Configurations

**Table 7-2. Function Selection Table**

| LOGIC FUNCTION | FIGURE NO. |
|---|---|
| 2-to-1 data selector | 7-4 |
| 2-input AND gate | 7-5 |
| 2-input OR gate with one inverted input | 7-6 |
| 2-input NAND gate with one inverted input | 7-6 |
| 2-input AND gate with one inverted input | 7-7 |
| 2-input NOR gate with one inverted input | 7-7 |
| 2-input OR gate | 7-8 |
| Inverter | 7-9 |
| Noninverted buffer | 7-10 |

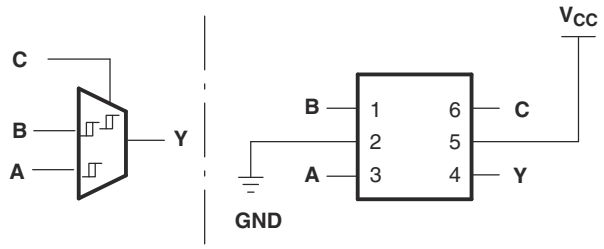


**图 7-4. 157: 2-to-1 Data Selector/MUX**
**When C is L, Y = B**
**When C is H, Y = A**

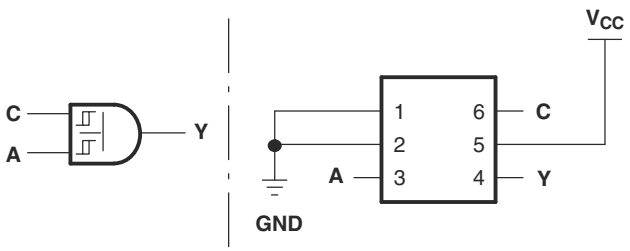


**图 7-5. 08: 2-Input AND Gate**

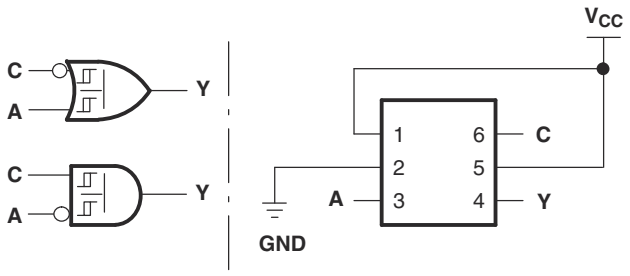


图 7-6. 14+32/14+00: 2-Input OR/NAND Gate With One Inverted Input

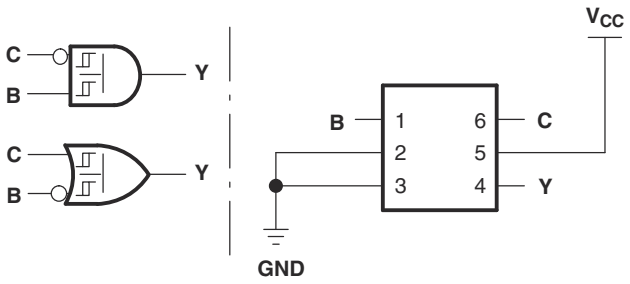


图 7-7. 14+08/14+02: 2-Input AND/NOR Gate With One Inverted Input

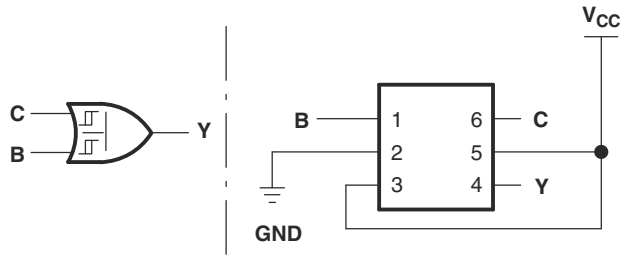


图 7-8. 32: 2-Input OR Gate

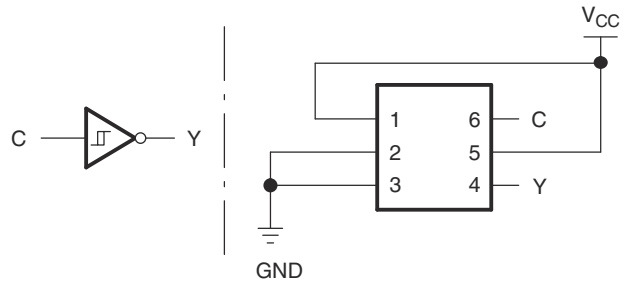


图 7-9. 04/14: Inverter

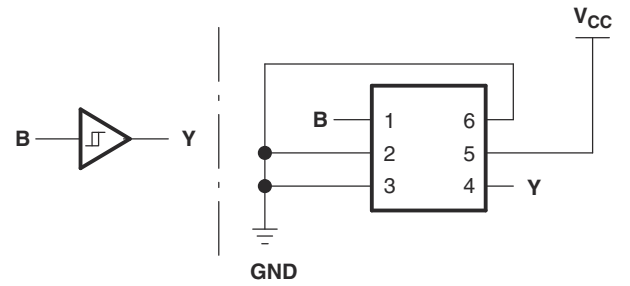


图 7-10. 17/34: Noninverted Buffer


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# 8 Device and Documentation Support

## 8.1 Documentation Support

### 8.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.5 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T97DBVR | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT4R |
| SN74AUP1T97DBVR.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT4R |
| SN74AUP1T97DBVRG4 | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT4R |
| SN74AUP1T97DBVRG4.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT4R |
| SN74AUP1T97DBVT | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT4F, HT4R) |
| SN74AUP1T97DBVT.B | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT4F, HT4R) |
| SN74AUP1T97DCKR | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (THF, THR) |
| SN74AUP1T97DCKR.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (THF, THR) |
| SN74AUP1T97DCKRG4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (THF, THR) |
| SN74AUP1T97DRYR | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97DRYR.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97DSFR | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97DSFR.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97DSFRG4 | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97DSFRG4.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TH |
| SN74AUP1T97YFPR | Active | Production | DSBGA (YFP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (TH2, THN) |
| SN74AUP1T97YFPR.B | Active | Production | DSBGA (YFP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (TH2, THN) |
| SN74AUP1T97YZPR | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (TH2, THN) |
| SN74AUP1T97YZPR.B | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (TH2, THN) |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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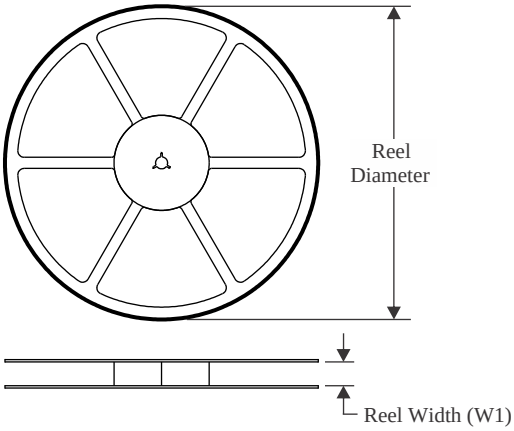
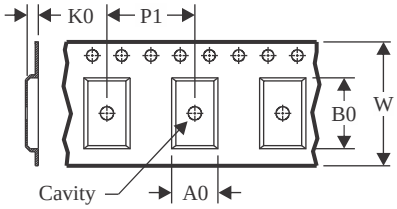
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

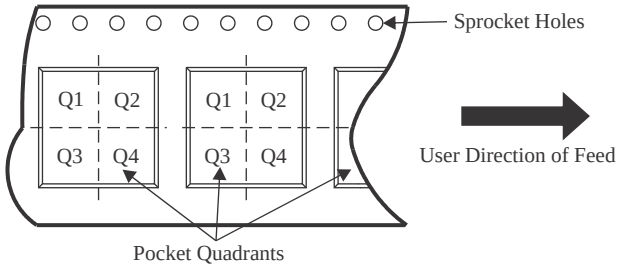



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

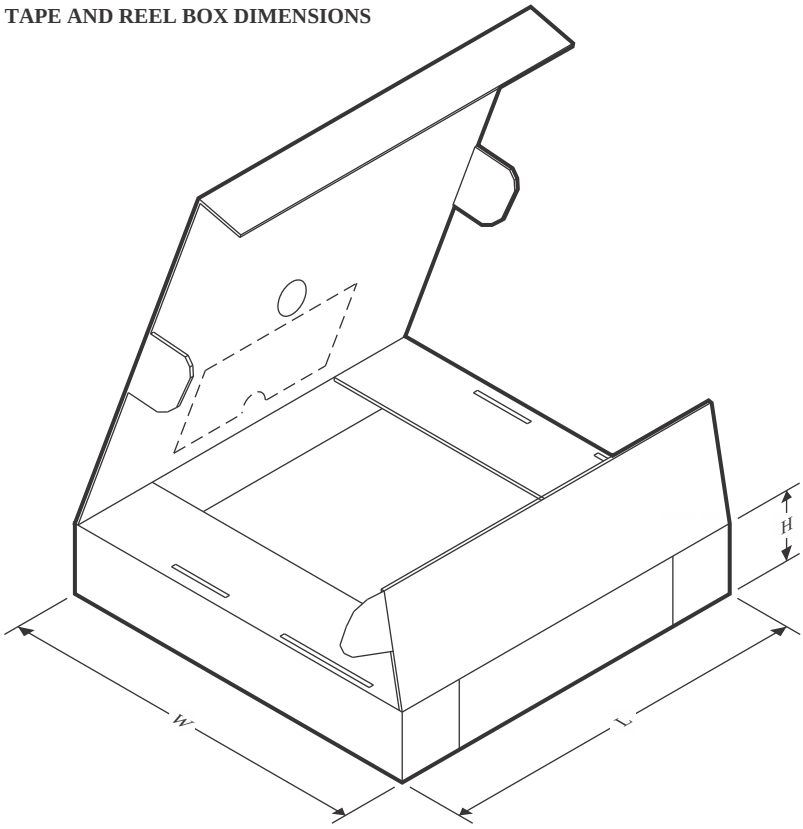
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T97DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1T97DBVRG4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1T97DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1T97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1T97DRYR | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.25 | 1.6 | 0.7 | 4.0 | 8.0 | Q1 |
| SN74AUP1T97DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1T97DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1T97YFPR | DSBGA | YFP | 6 | 3000 | 178.0 | 9.2 | 0.89 | 1.29 | 0.62 | 4.0 | 8.0 | Q1 |
| SN74AUP1T97YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

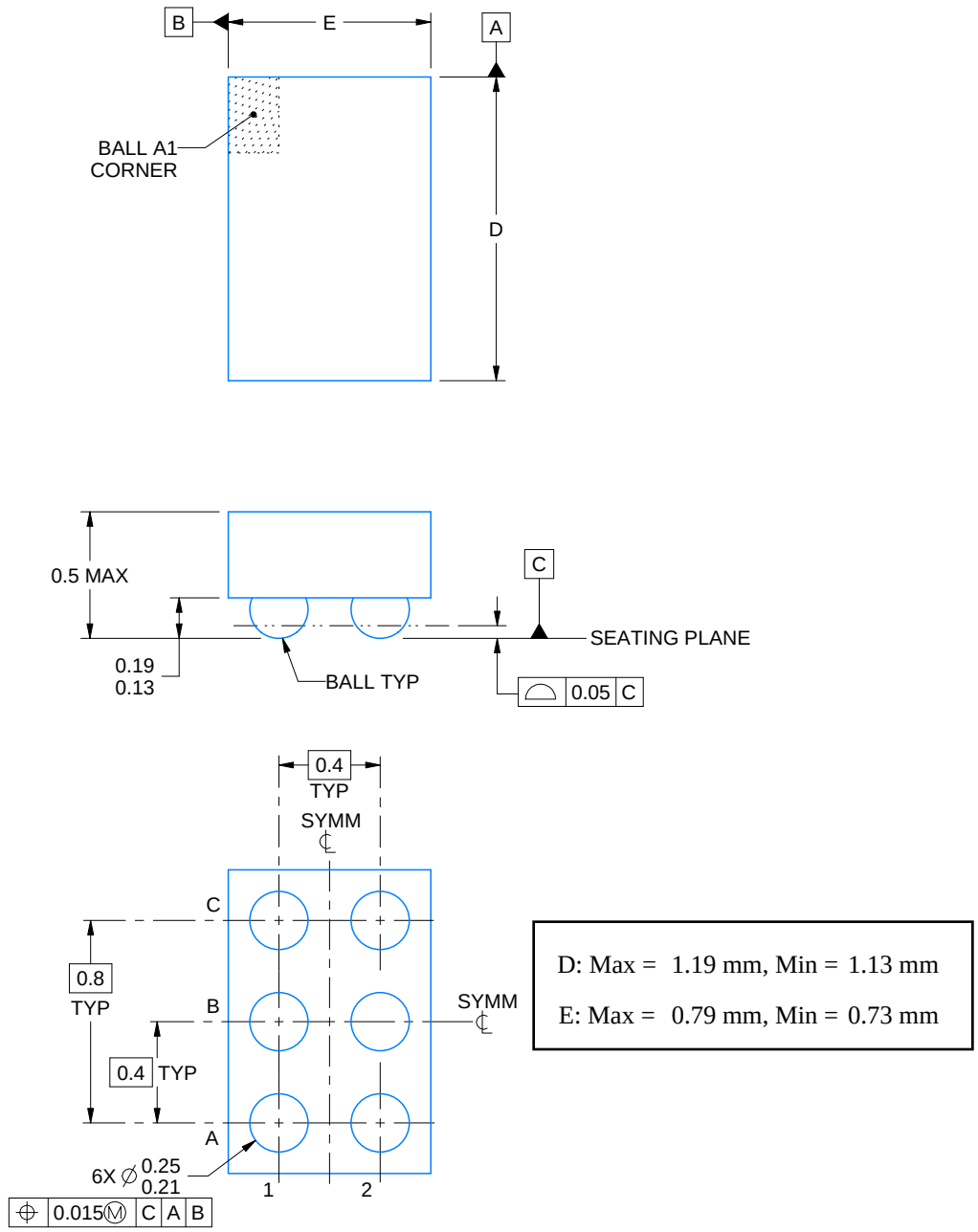
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1T97DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1T97DBVRG4 | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1T97DBVT | SOT-23 | DBV | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1T97DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1T97DRYR | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1T97DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1T97DSFRG4 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1T97YFPR | DSBGA | YFP | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74AUP1T97YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

# PACKAGE OUTLINE

## YFP0006

## DSBGA - 0.5 mm max height

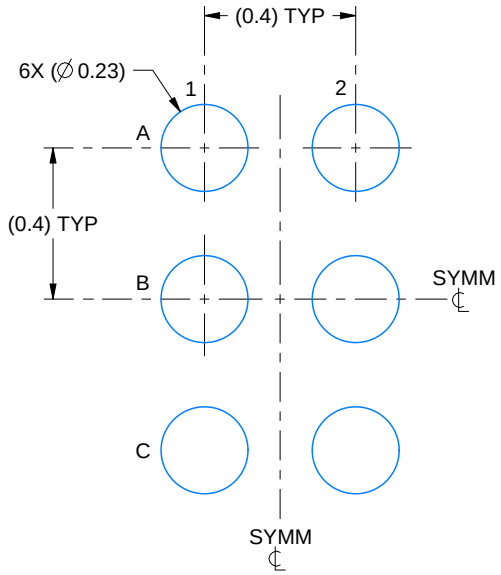
DIE SIZE BALL GRID ARRAY



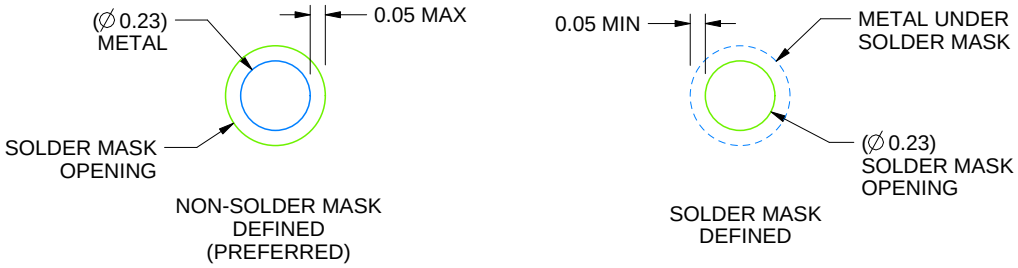

4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:50X

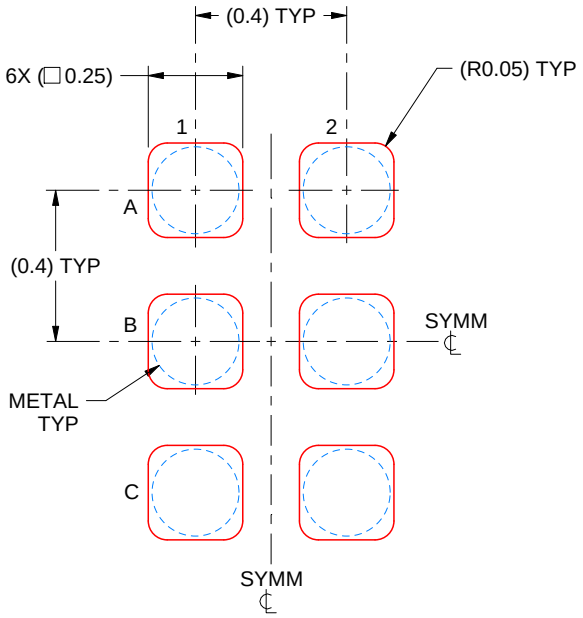



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

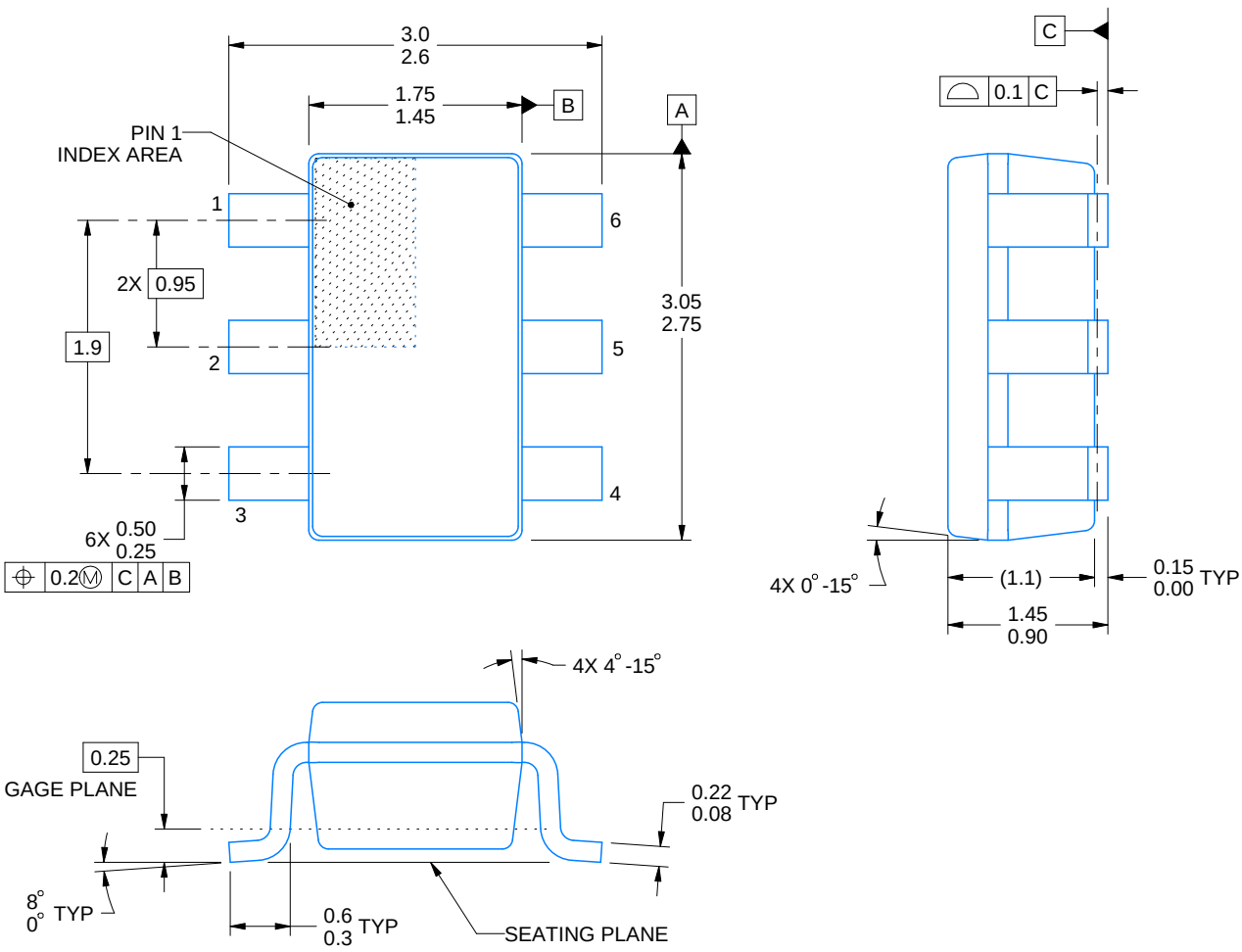
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

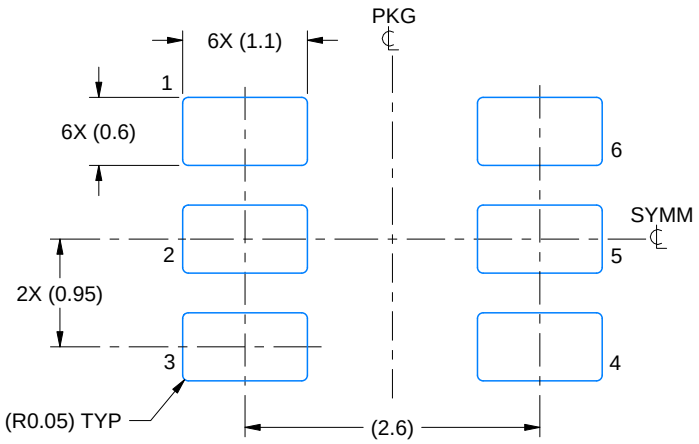
SMALL OUTLINE TRANSISTOR



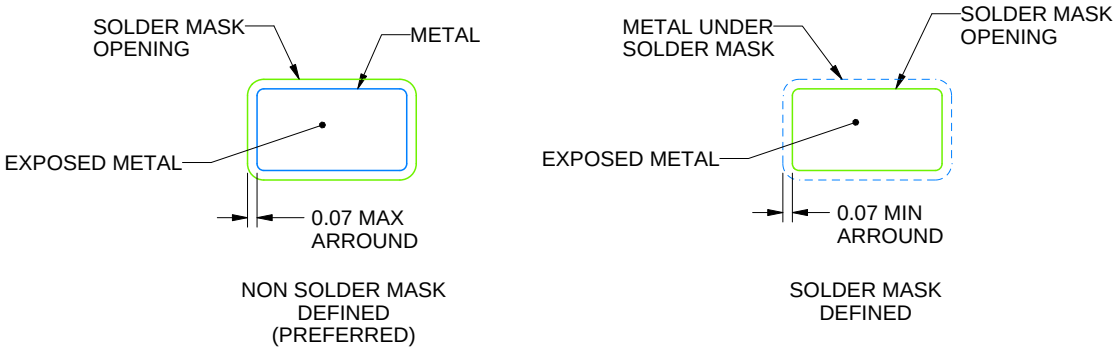

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

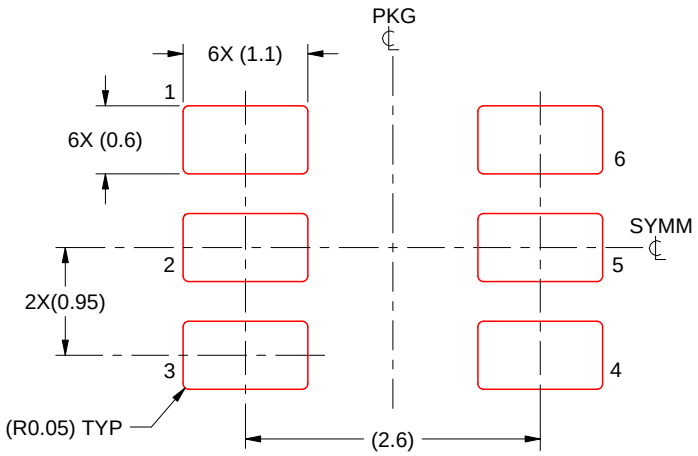



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

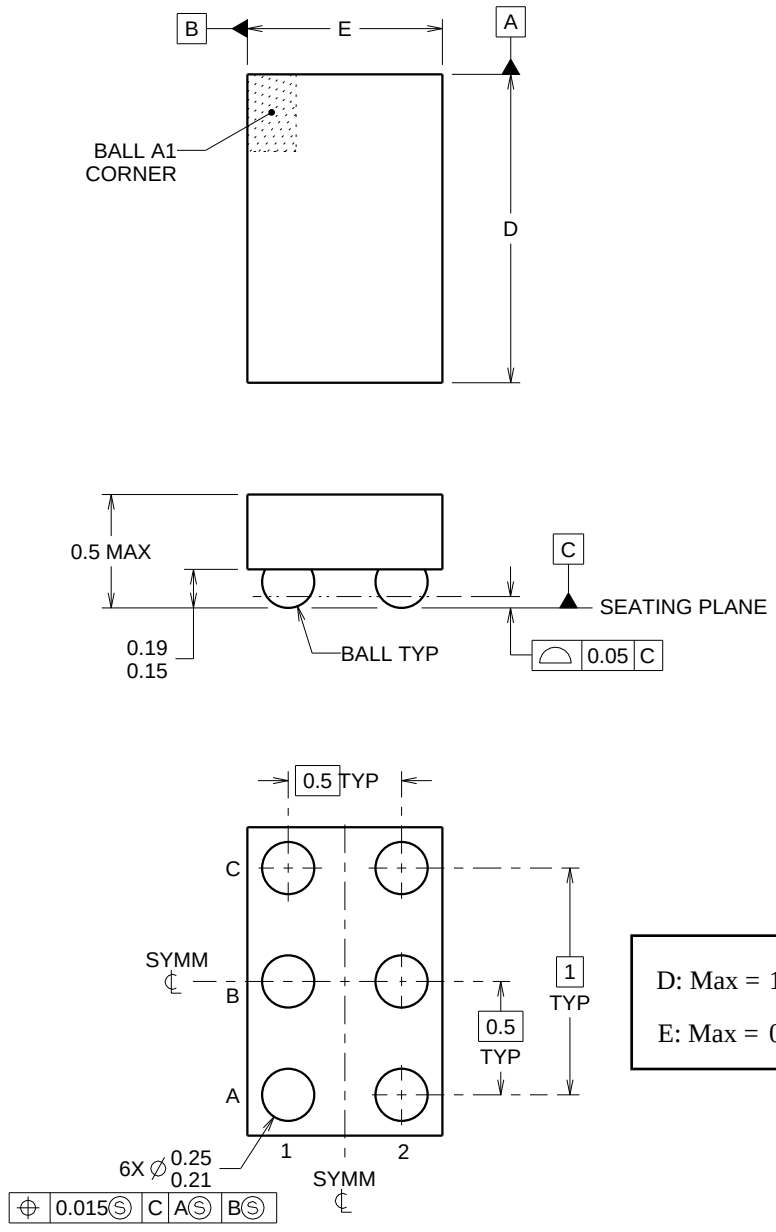
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YZP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 1.418 mm, Min =1.358 mm

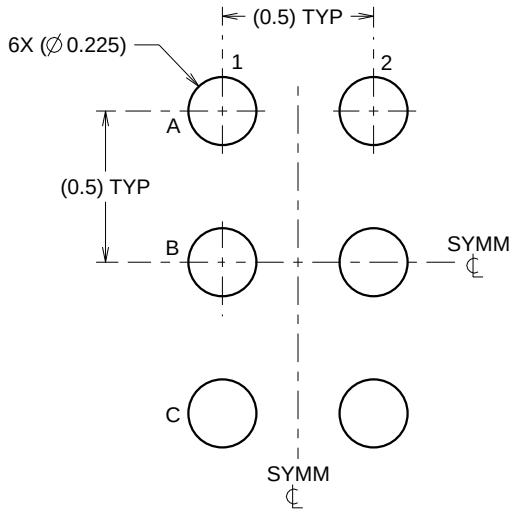
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

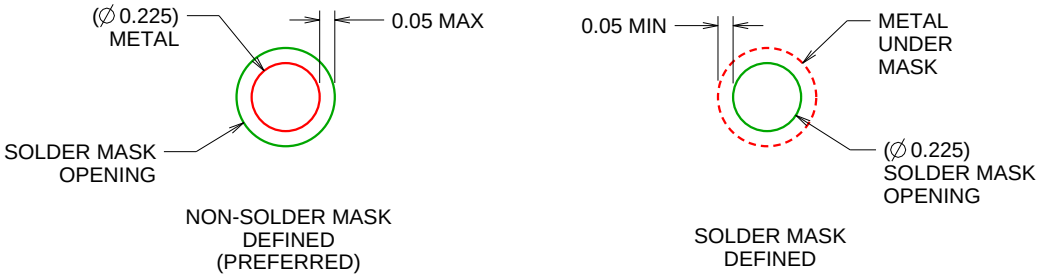
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:40X




SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

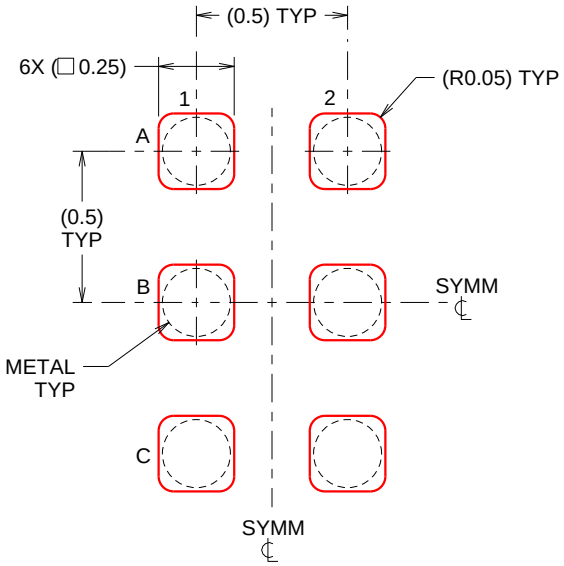
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

# EXAMPLE STENCIL DESIGN

## YZP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

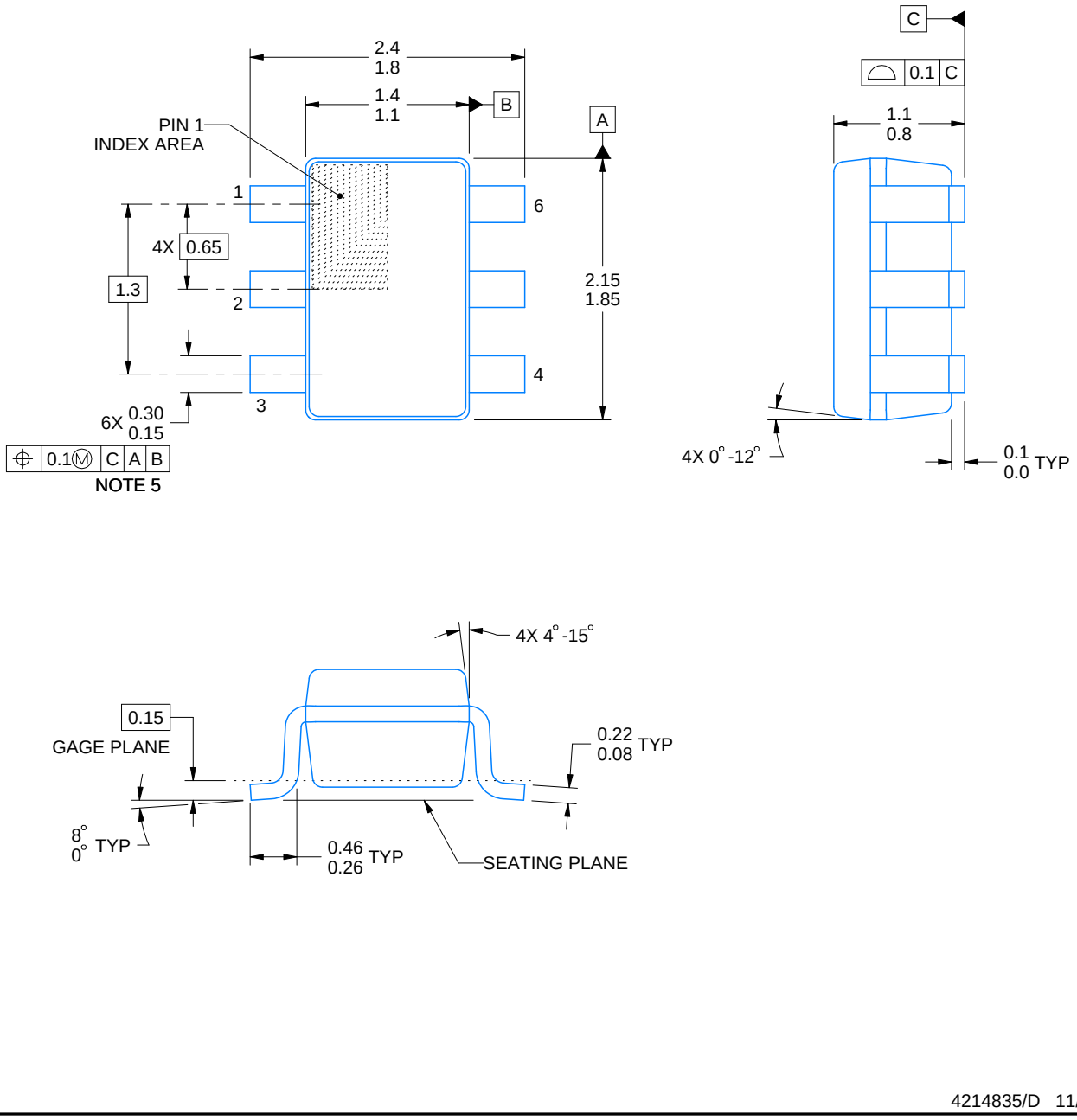
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0006A

## SOT - 1.1 max height

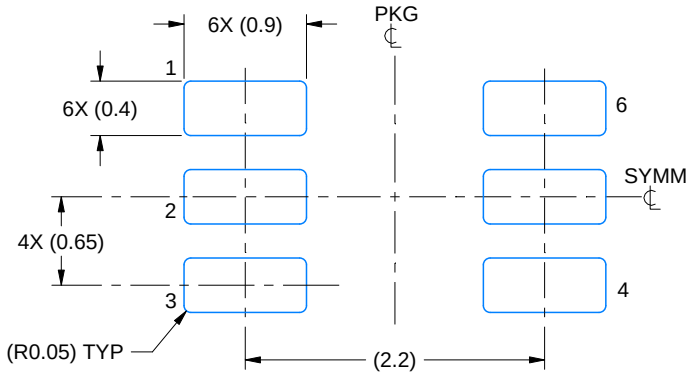
SMALL OUTLINE TRANSISTOR



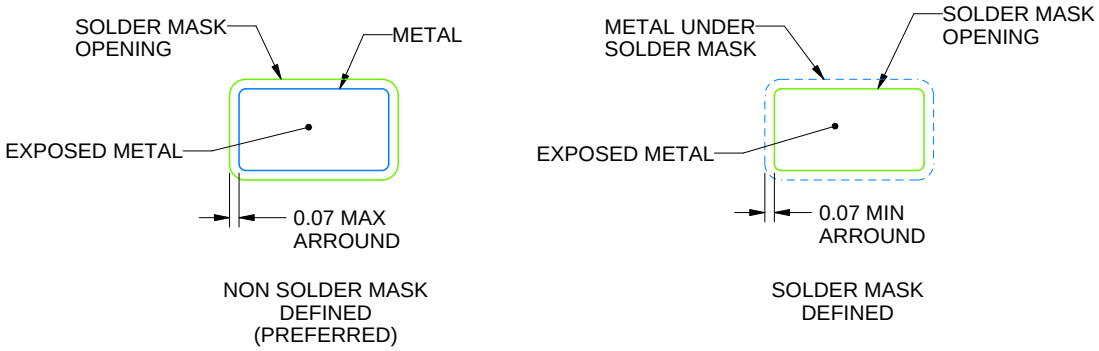

4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

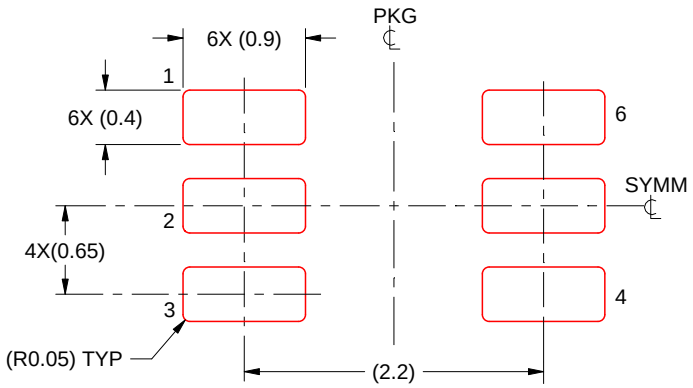



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

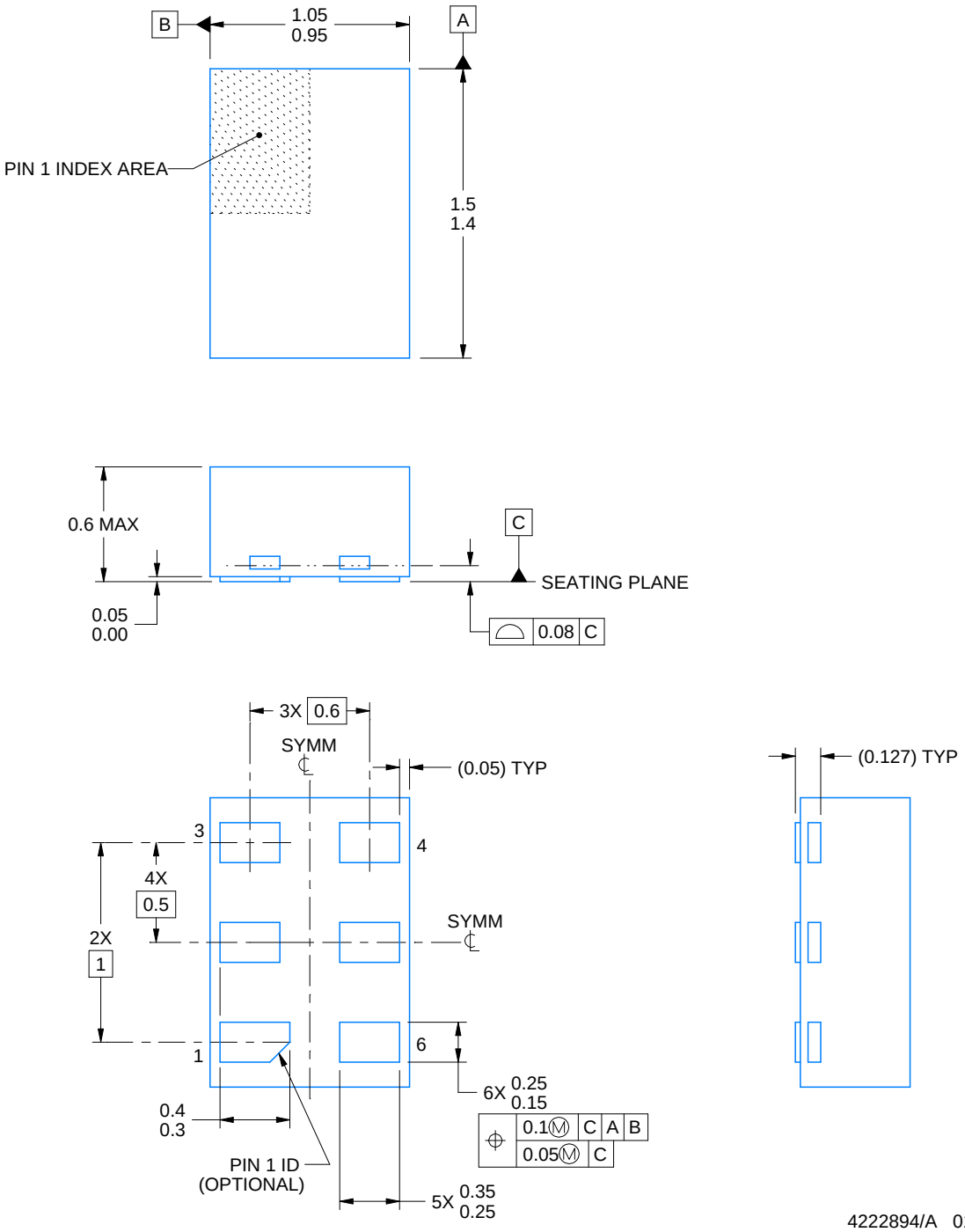
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DRY0006A

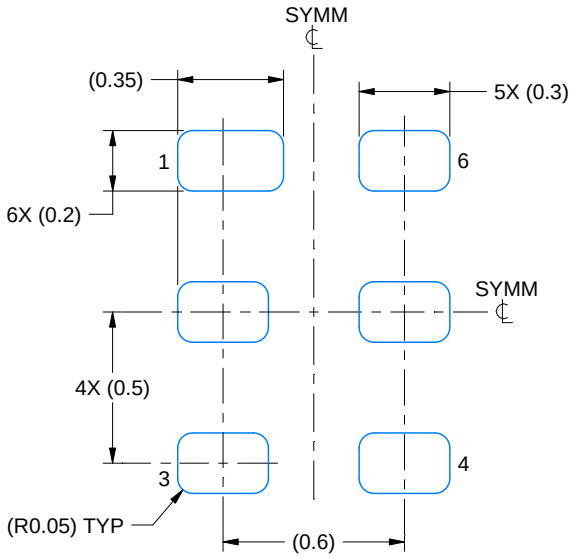
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

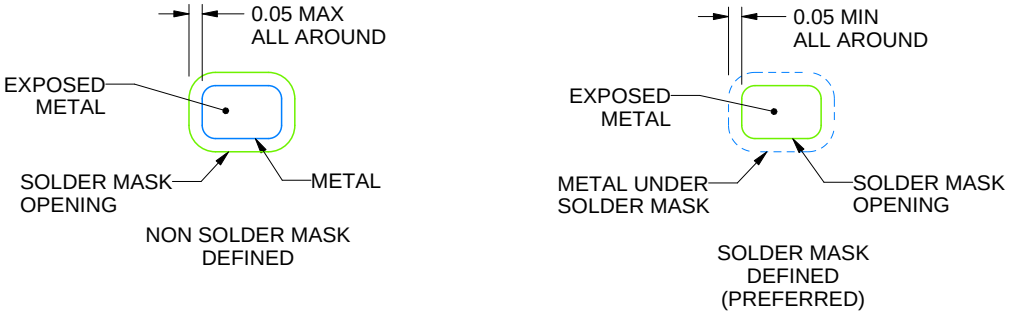



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

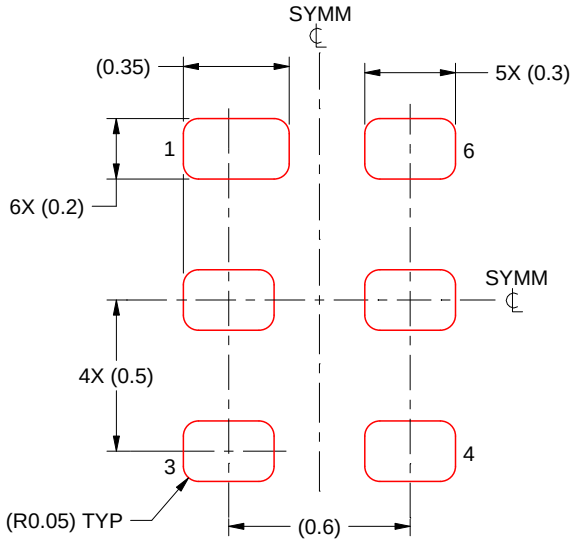
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

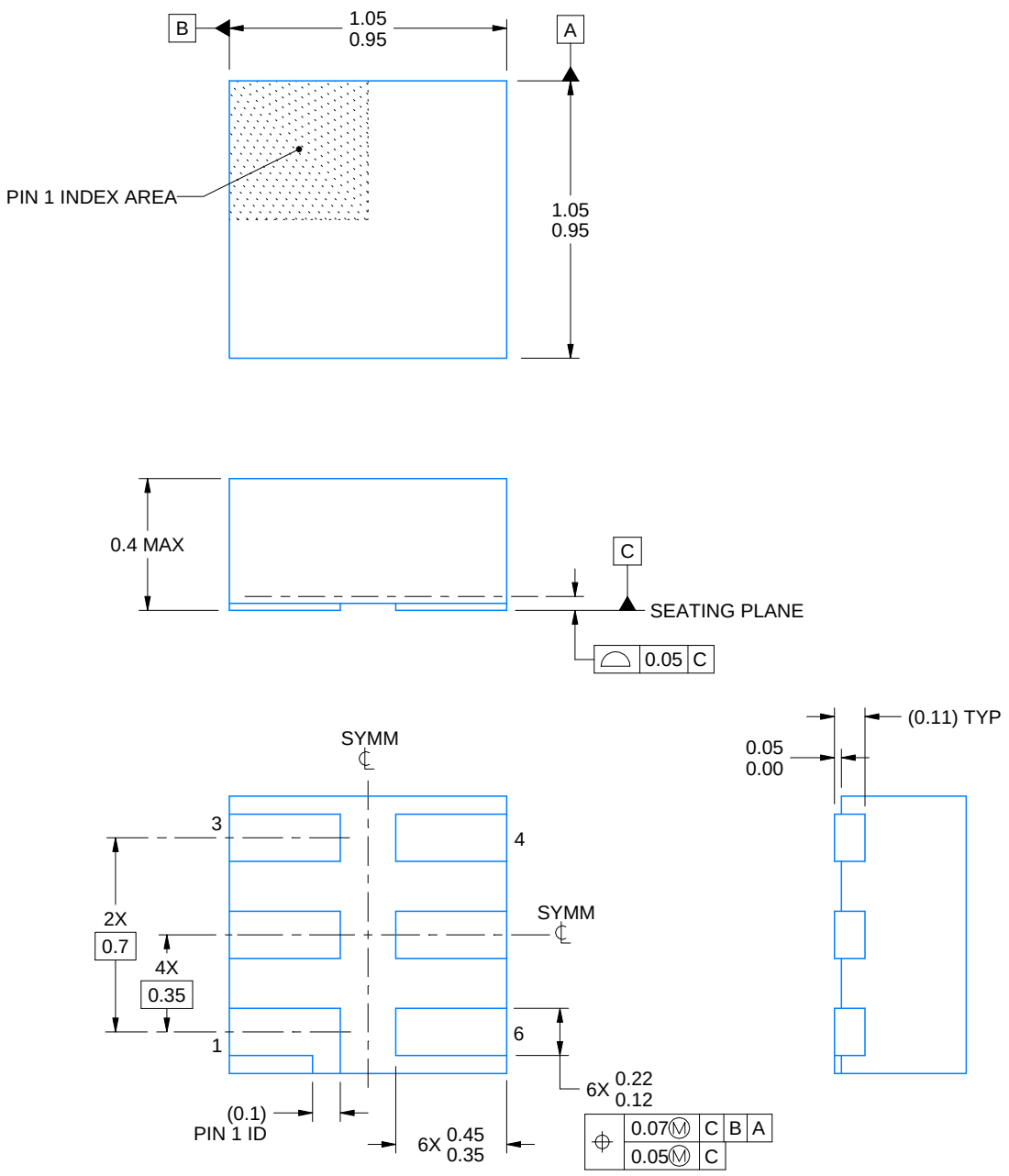
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

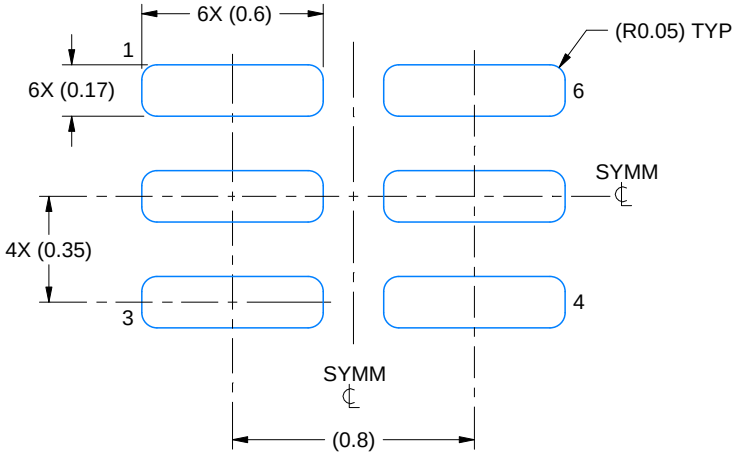
PLASTIC SMALL OUTLINE - NO LEAD



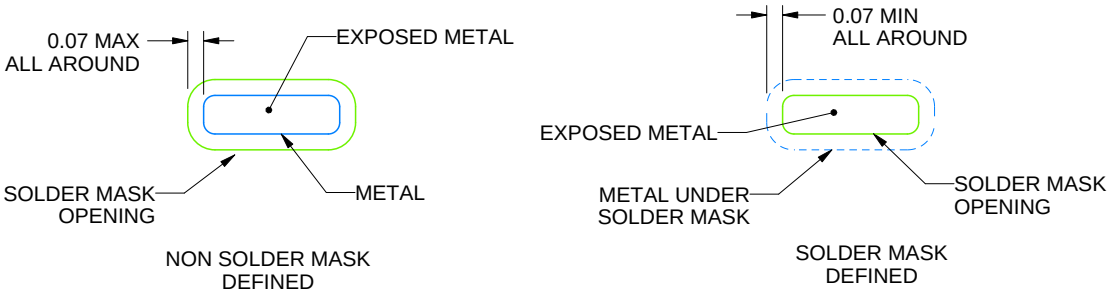

4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

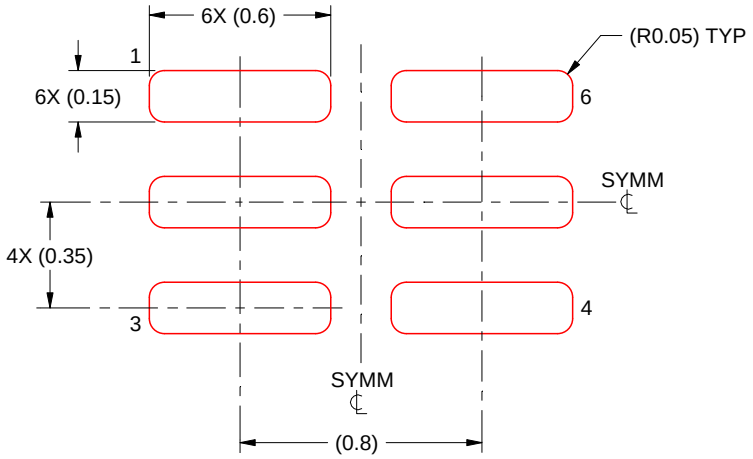
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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