

SN74AUP1T34-Q1 1 位单向电压电平转换器

1 特性

- 适用于汽车电子 应用
 - 符合 AEC-Q100 标准
 - 器件温度等级 1: -40°C 至 125°C 的环境运行温度范围
 - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 3A
 - 带电器件模型 (CDM) ESD 分类等级 C5
- 0.9V 至 3.6V 的宽运行 VCC 范围
- 均衡的传播延迟: $t_{PLH} = t_{PHL}$ (1.8V 至 3.3V 转换时的典型值)
- 低静态功耗: ICC 最高为 5μA
- ±6mA 输出驱动 (电压为 3V 时)
- I_{off} 支持部分掉电模式运行
- VCC 隔离特性 – 如果 VCCA 输入接地, 则 B 端口处于高阻态
- 输入滞后可实现输入转换和输入上更好的开关噪声抗扰度
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
- 5000V 人体模型 (AEC-Q100-002-E)
- 锁存性能满足 100mA, 符合 Q100-004-D 规范

2 应用范围

- 汽车
- 企业
- 工业
- 个人电子产品
- 电信

3 说明

SN74AUP1T34-Q1 器件是一款 1 位非反向转换器, 使用两条独立的可配置电源轨。该单向转换器在 A 和 B 两端口间转换。A 端口设计用于跟踪 VCCA。VCCA 可接受从 0.9V 到 3.6V 范围内的电源电压。B 端口设计用于跟踪 VCCB。VCCB 可接受从 0.9V 至 3.6V 间的电源电压值。这可实现 1V, 1.2V, 1.5V, 1.8V, 2.5V 和 3.3V 电压节点间的低压转换。此外, SN74AUP1T34-Q1 完全适用于使用 I_{off} 的局部掉电应用。 I_{off} 电路会禁用输出, 从而在器件掉电时防止电流回流损坏器件。

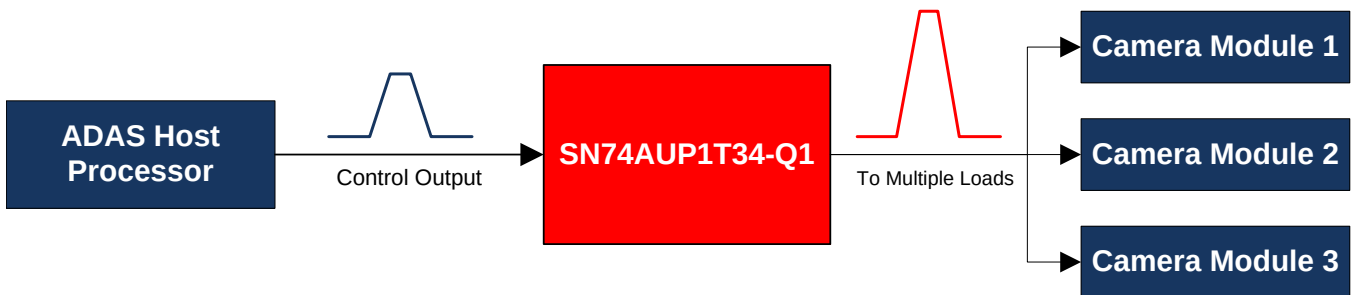
VCC 隔离特性确保了在 VCCA 输入在 GND 上时, B 端口处于高阻抗状态。如果 VCCB 输入在 GND 上, 到 A 侧的任一输入都不会导致泄漏电流, 即使在悬空状态时也是如此。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74AUP1T34-Q1	SC70 (5)	2.00mm × 1.25mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

示例应用图



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目录

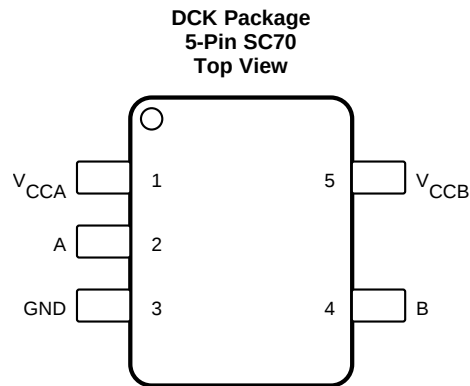
1	特性	1	8.3	Feature Description	7
2	应用范围	1	8.4	Device Functional Modes	7
3	说明	1	9	Application and Implementation	8
4	修订历史记录	2	9.1	Application Information	8
5	Pin Configuration and Functions	3	9.2	Typical Application	8
6	Specifications	3	10	Power Supply Recommendations	9
6.1	Absolute Maximum Ratings	3	11	Layout	10
6.2	ESD Ratings	3	11.1	Layout Guidelines	10
6.3	Recommended Operating Conditions	4	11.2	Layout Example	10
6.4	Thermal Information	4	12	器件和文档支持	11
6.5	AC Electrical Characteristics	5	12.1	社区资源	11
6.6	Typical Characteristics	6	12.2	商标	11
7	Parameter Measurement Information	6	12.3	静电放电警告	11
8	Detailed Description	7	12.4	Glossary	11
8.1	Overview	7	13	机械、封装和可订购信息	11
8.2	Functional Block Diagram	7			

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2013) to Revision A	Page
• 已添加 ESD 额定值表，特性 描述部分，器件功能模式，应用和 实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。	1
• 已删除 订购信息表	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	2	I	Input Port. Referenced to V_{CCA} .
B	4	O	Output Port. Referenced to V_{CCB} .
GND	3	—	Ground.
V_{CCA}	1	—	Input Port DC Power Supply.
V_{CCB}	5	—	Output Port DC Power Supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} , V_{CCB}	Supply voltage		−0.3	4	V
V_I	Input voltage		−0.5	4.6	V
V_O	Voltage applied to any output in the high-impedance or power-off state		−0.5	4.6	V
	Voltage applied to any output in the high or low state		−0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature		−65	150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ , Classification 3A	5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ , Classification C5	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

SN74AUP1T34-Q1

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCCA	VCCB	MIN	MAX	UNIT
V_{CCA}, V_{CCB} Supply voltage				0.9	3.6	V
V_{IH} High-level input voltage		0.9 V to 1.95 V	0.9 V to 1.95 V	$0.65 \times V_{CCA}$		V
		2.3 V to 2.7 V	0.9 V to 3.6 V	1.6		
		3 V to 3.6 V	0.9 V to 3.6 V	2		
V_{IL} Low-level input voltage		0.9 V	0.9 V to 1.95 V	$0.3 \times V_{CCA}$		V
		1 V to 1.95 V	0.9 V to 1.95 V	$0.35 \times V_{CCA}$		
		2.3 V to 2.7 V	0.9 V to 3.6 V	0.7		
		3 V to 3.6 V	0.9 V to 3.6 V	0.9		
$\Delta t/\Delta v$ Input transition rise or fall rate		3 V to 3.6 V	0.9 V to 3.6 V		200	ns/V
T_A Operating free-air temperature				–40	125	°C
V_{OH}	$I_{OH} = -100 \mu A$	$V_I = V_{IH}$	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCB} - 0.2$	V
	$I_{OH} = -0.25 \text{ mA}$		0.9 V to 1 V	0.9 V to 1 V	$0.75 \times V_{CCB}$	
	$I_{OH} = -1.5 \text{ mA}$		1.2 V	1.2 V	1	
	$I_{OH} = -2 \text{ mA}$		1.65 V	1.65 V	1.32	
	$I_{OH} = -3 \text{ mA}$		2.3 V	2.3 V	1.9	
	$I_{OH} = -6 \text{ mA}$		3 V	3 V	2.72	
V_{OL}	$I_{OL} = 100 \mu A$	$V_I = V_{IL}$	0.9 V to 3.6 V	0.9 V to 3.6 V	0.1	V
	$I_{OL} = 0.25 \text{ mA}$		0.9 V to 1 V	0.9 V to 1 V	0.1	
	$I_{OL} = 1.5 \text{ mA}$		1.2 V	1.2 V	$0.3 \times V_{CCB}$	
	$I_{OL} = 2 \text{ mA}$		1.65 V	1.65 V	0.31	
	$I_{OL} = 3 \text{ mA}$		2.3 V	2.3 V	0.31	
	$I_{OL} = 6 \text{ mA}$		3 V	3 V	0.31	
I_i Control inputs	$V_i = V_{CCA}$ or GND	0.9 V to 3.6 V	0.9 V to 3.6 V		± 1	μA
I_{off} A or B port	V_I or $V_O = 0$ to 3.6 V	0 V	0 V to 3.6 V		± 5	μA
		0 V to 3.6 V	0 V		± 5	
I_{CCA}	$V_I = V_{CCI}$ or GND, $I_O = 0 \text{ mA}$	0.9 V to 3.6 V	0.9 V to 3.6 V		2.7	μA
		0.9 V to 3.6 V	V_{CCA}		2	
		0 V	0 V to 3.6 V		1	
		0 V to 3.6 V	0 V		1	
I_{CCB}	$V_I = V_{CCI}$ or GND, $I_O = 0 \text{ mA}$	0.9 V to 3.6 V	0.9 V to 3.6 V		2.7	μA
		0.9 V to 3.6 V	V_{CCA}		2	
		0 V	0 V to 3.6 V		1	
		0 V to 3.6 V	0 V		1	
$I_{CCA} + I_{CCB}$	$V_I = V_{CCI}$ or GND, $I_O = 0 \text{ mA}$	0.9 V to 3.6 V	0.9 V to 3.6 V		5.4	μA
C_{io} A or B port		3.3 V	3.3 V		4	pF

6.4 Thermal Information

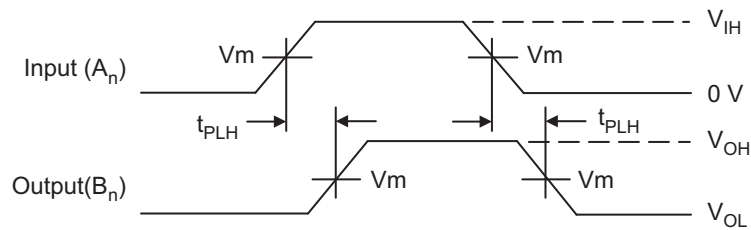
THERMAL METRIC ⁽¹⁾		SN74AUP1T34-Q1	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	301.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	C _L	VCCA	VCCB = 0.9 V		VCCB = 1.2 V		VCCB = 1.65 V		VCCB = 2.3 V		VCCB = 3 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t _{PLH} /t _{PHL}	5 pF	0.9 V	25		18		16.2		16.3		16.8		ns
	5 pF	1.2 V		42.5		24.9		23.2		22.6		22.5	
	5 pF	1.65 V		40		10.7		8.84		8.08		7.88	
	5 pF	2.3 V		41.3		8.02		5.73		4.92		4.2	
	5 pF	3 V		42.5		7.61		4.5		3.65		3.39	
t _{PLH} /t _{PHL}	10 pF	0.9 V	28.9		19.8		17.9		18		18.5		ns
	10 pF	1.2 V		43.22		12.33		9.57		8.81		8.61	
	10 pF	1.65 V		40.44		9.21		6.57		5.6		4.73	
	10 pF	2.3 V		41.56		8.3		5.54		4.42		4.07	
	10 pF	3 V		42.81		7.87		4.8		3.8		3.36	
t _{PLH} /t _{PHL}	15 pF	0.9 V	30.6		21.6		19.6		19.7		20.3		ns
	15 pF	1.2 V		43.87		16.2		11.8		11		11	
	15 pF	1.65 V		40.78		14.7		8.8		7.1		6.4	
	15 pF	2.3 V		41.79		14.9		7.6		5.88		5.27	
	15 pF	3 V		43.09		16.2		6.98		5.4		4.7	
t _{PLH} /t _{PHL}	30 pF	0.9 V	32.1		21.3		18.7		18		18.3		ns
	30 pF	1.2 V		45.65		15.1		12.37		11.61		11.41	
	30 pF	1.65 V		41.72		12.18		8.15		6.94		6.1	
	30 pF	2.3 V		42.44		12.35		7.25		5.55		4.97	
	30 pF	3 V		43.69		11.6		6.92		4.95		4.35	



$$V_{MI} = V_{IH}/2; V_{MO} = V_{CCB}/2$$

$$t_R = t_F = 2.0 \text{ ns, 10% to 90%}; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$$

Figure 1. Waveform 1 - Propagation Delays

6.6 Typical Characteristics

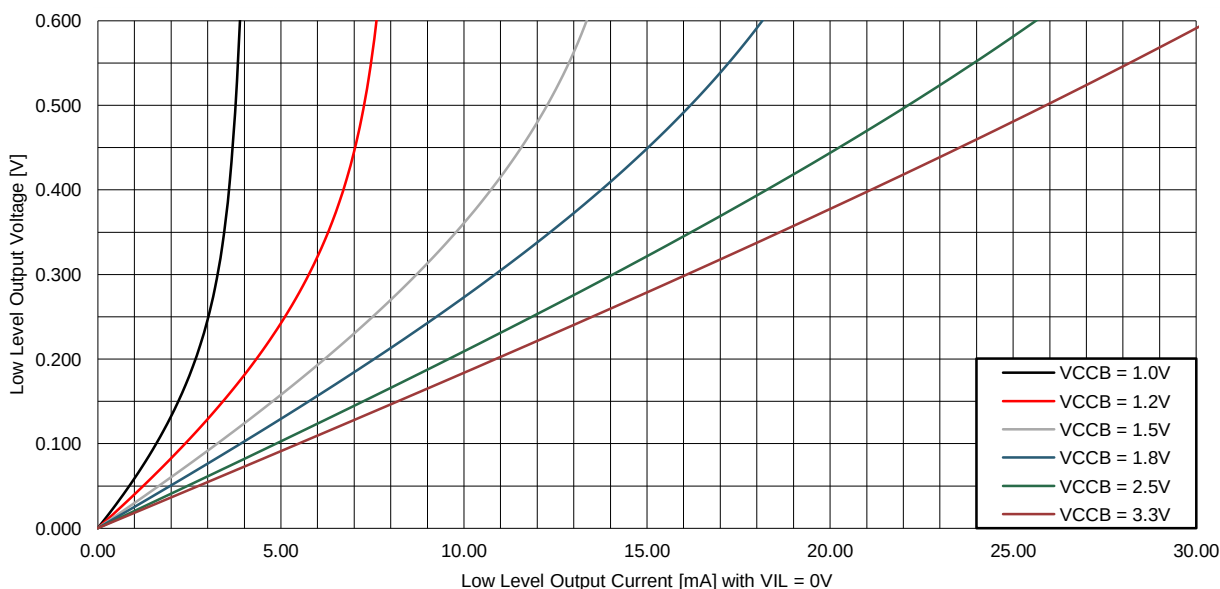
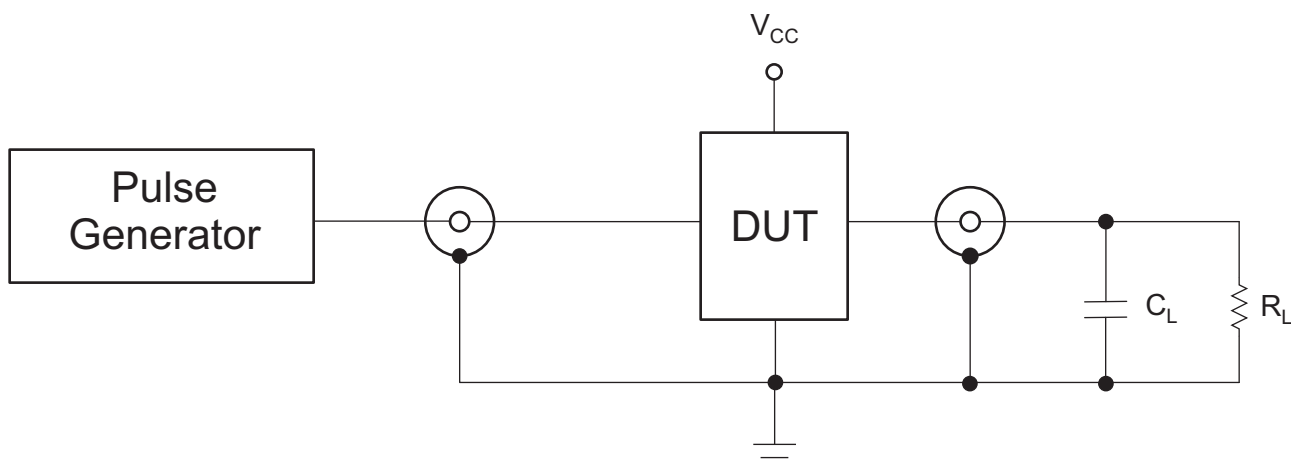


Figure 2. Low Level Output Voltage vs Low Level Output Current

7 Parameter Measurement Information



TEST

t_{PLH} , t_{PHL}

C_L = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

R_L = 1 M Ω or equivalent

Z_{OUT} of pulse generator = 50 Ω

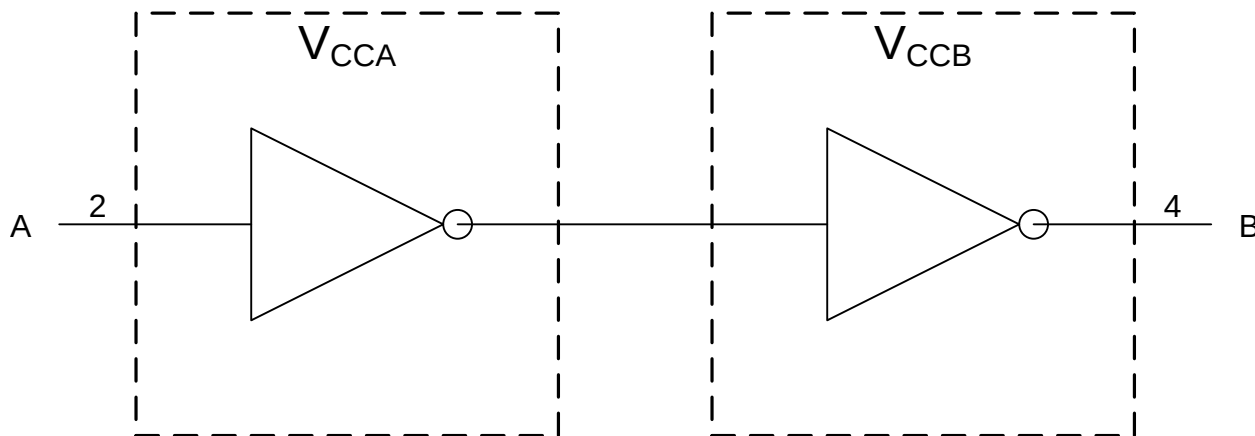
Figure 3. AC (Propagation Delay) Test Circuit

8 Detailed Description

8.1 Overview

The SN74AUP1T34-Q1 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to V_{CCA} , receives the signal that is to be level translated. Pin B, which is referenced to V_{CCB} , transmits the level translated signal. Both supply pins V_{CCA} and V_{CCB} support a voltage range from 0.9 V to 3.6 V.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34-Q1 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

8.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1T34-Q1.

Table 1. Function Table

INPUT	OUTPUT
A PORT	B PORT
L	L
H	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1T34-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

9.2 Typical Application

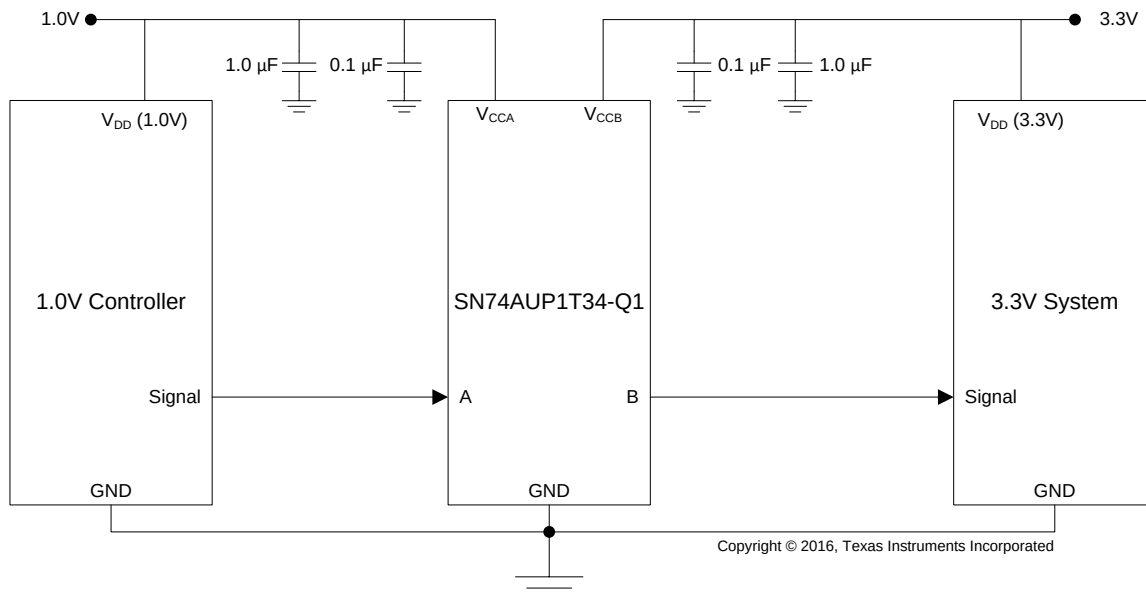


Figure 4. Typical Application Example

9.2.1 Design Requirements

Table 2 lists the design requirements of the SN74AUP1T34-Q1.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0.9 V to 3.6 V
Output Voltage Range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74AUP1T34-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74AUP1T34-Q1 device is driving to determine the output voltage range.

9.2.3 Application Curve

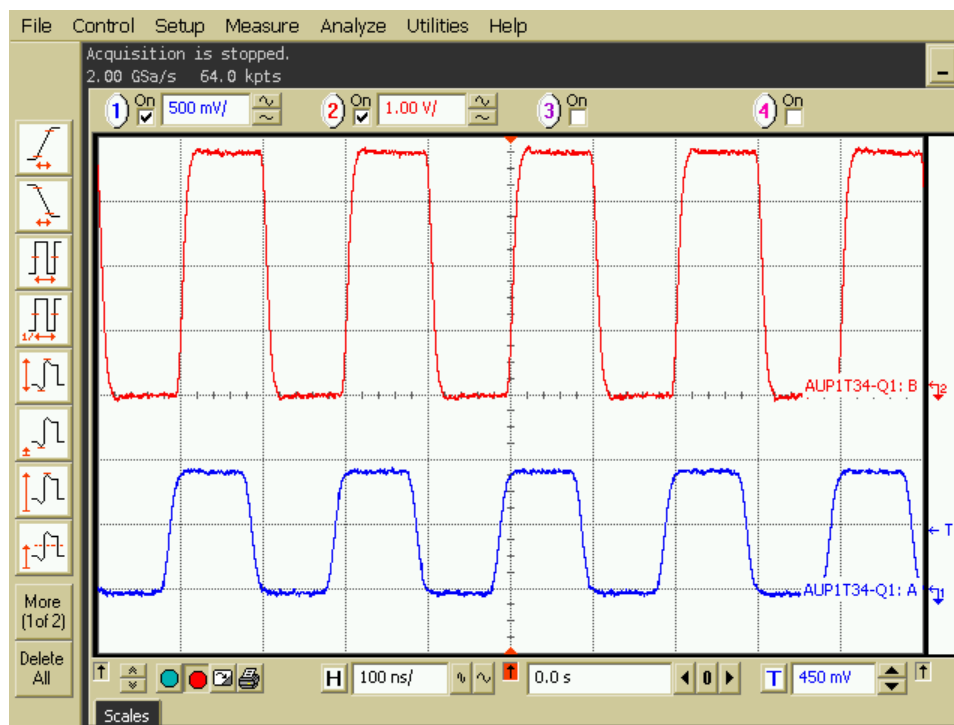


Figure 5. 10 MHz Up Translation (0.9 V to 3.6 V)

10 Power Supply Recommendations

Connect ground before applying either V_{CCA} or V_{CCB} . There is no specific power sequence requirement for the SN74AUP1T34. V_{CCA} or V_{CCB} may be powered up first, and V_{CCA} or V_{CCB} may be powered down first.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

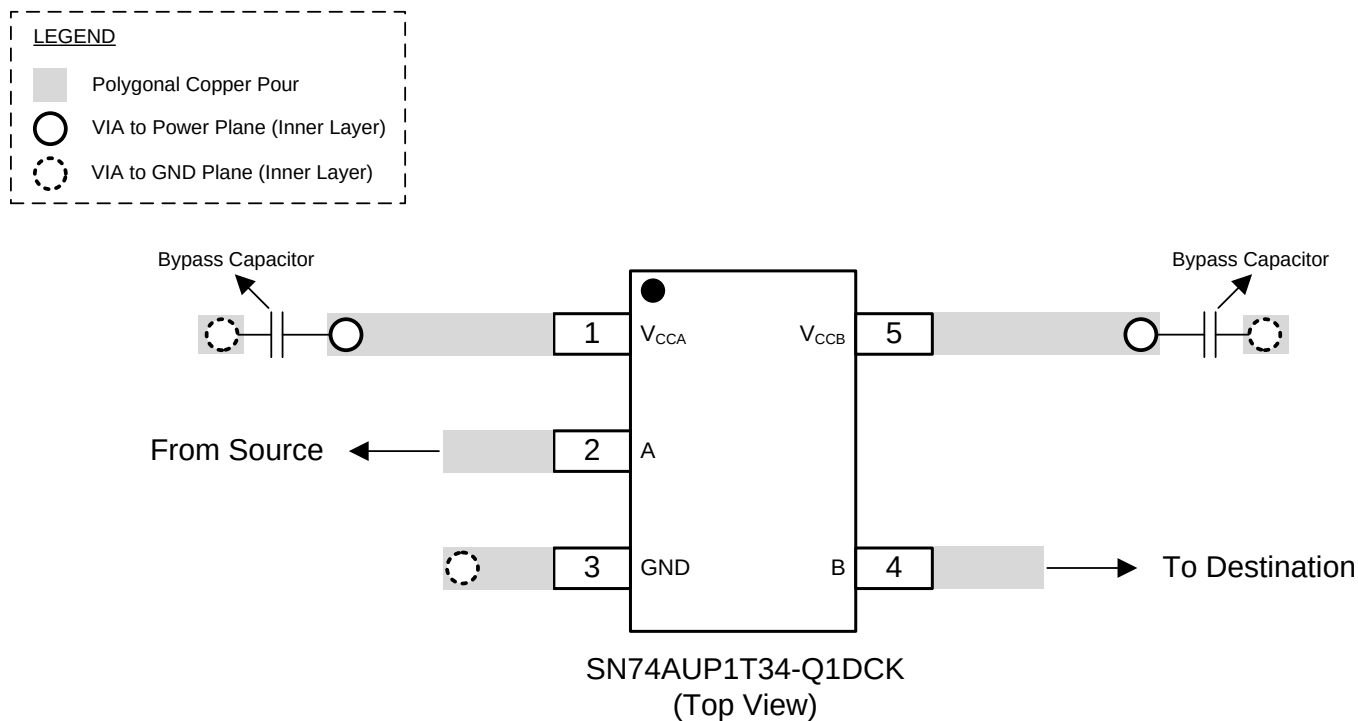


Figure 6. Example Layout

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

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12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1T34QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(U4E, U4J)
SN74AUP1T34QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(U4E, U4J)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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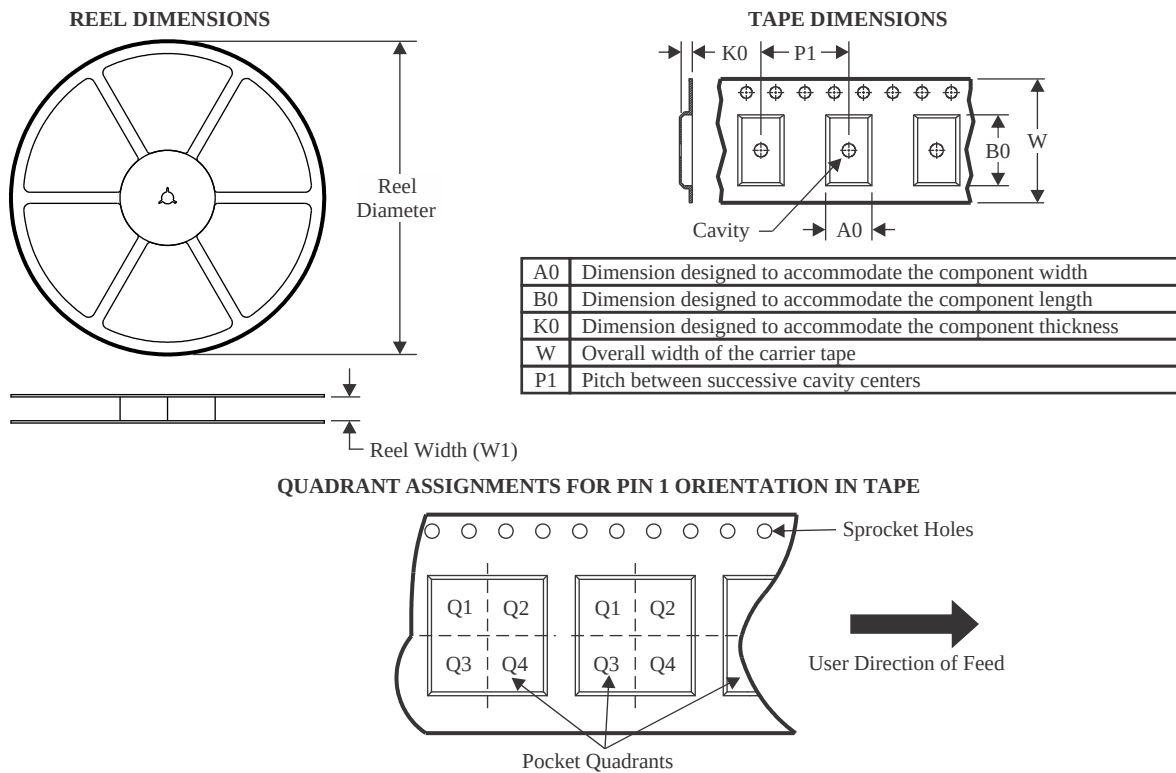
OTHER QUALIFIED VERSIONS OF SN74AUP1T34-Q1 :

- Catalog : [SN74AUP1T34](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

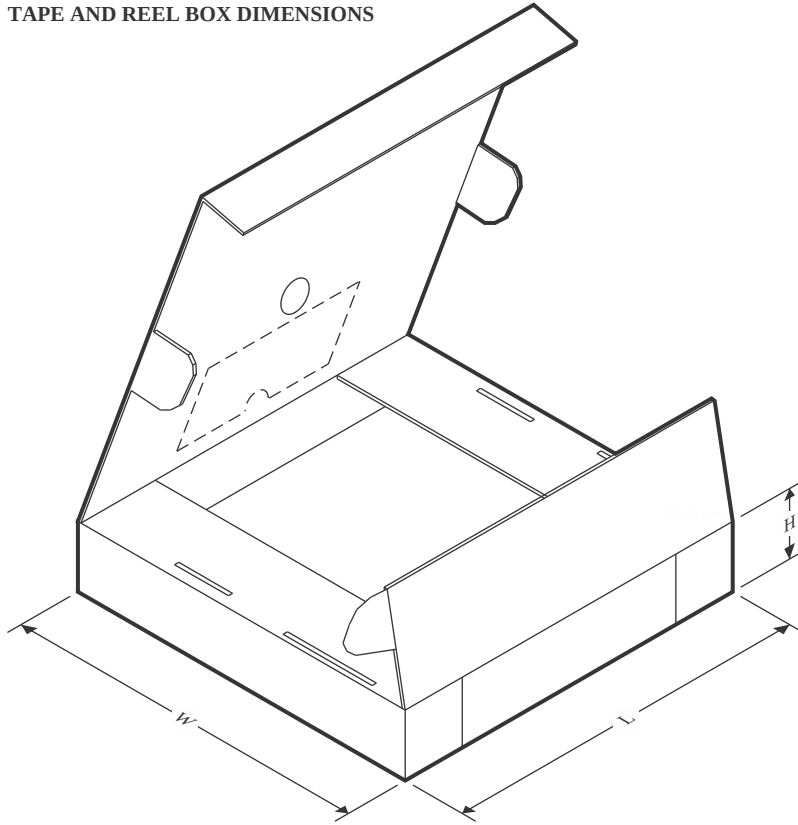
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T34QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T34QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0



SOT - 1.1 max height

Technical drawing of a mechanical part showing three views: front, side, and top.

Front View Dimensions:

- Overall width: 2.4 (1.8)
- Overall height: 2.15 (1.85)
- Horizontal hole locations: 1.4 (1.1)
- Vertical hole locations: 1.3 (1.3)
- Hole sizes: 0.15 (0.1)
- Feature: NOTE 4
- Pin 1 Index Area (hatched)

Side View Dimensions:

- Width: 1.1 MAX
- Thickness: 0.1 C

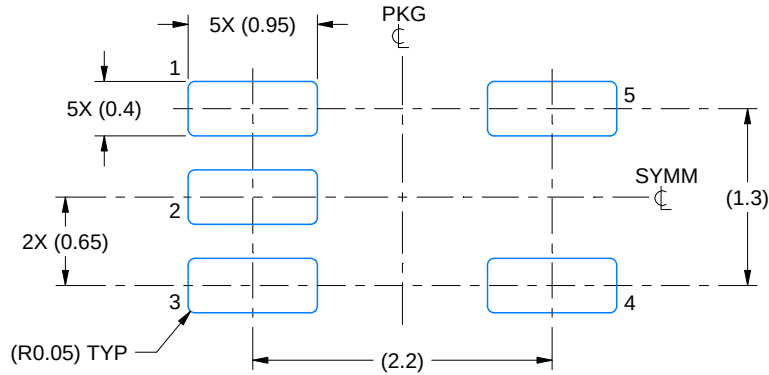
Top View Dimensions:

- Width: 0.46 TYP (0.26 TYP)
- Height: 0.22 TYP (0.08 TYP)
- Gage Plane
- Seating Plane
- Surface texture: 4X 4° -15°

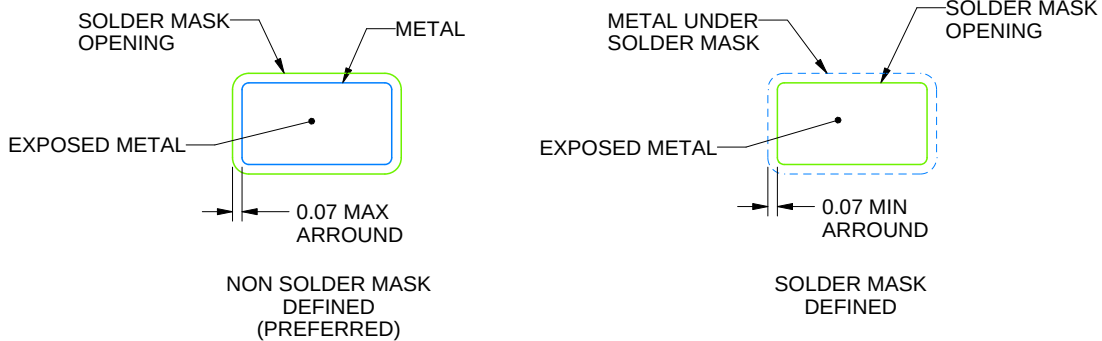
Surface Texture Symbols:

- Front View: 0.1 (0.05) C A B
- Top View: 0.1 (0.05) C A B

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

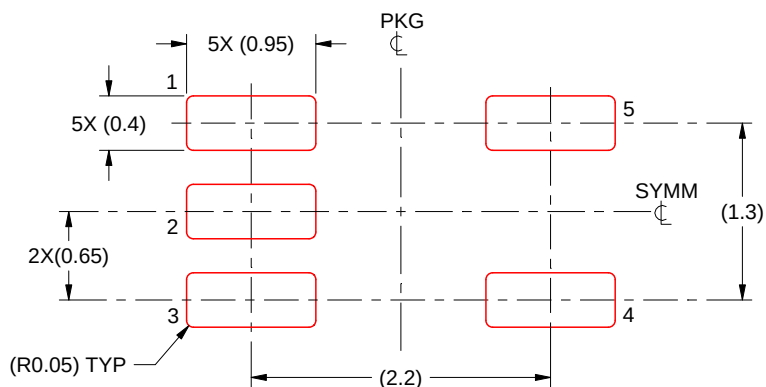


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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