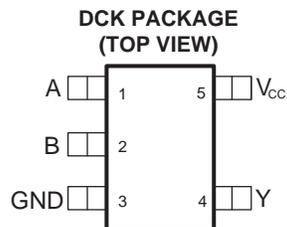


低功耗单路 2 输入正与门

查询样品: [SN74AUP1G08-Q1](#)

特性

- 具有符合 **AEC-Q100** 的下列结果:
 - 器件温度 1 级: **-40°C 至 125°C** 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
 - 器件充电器件模型 (CDM) ESD 分类等级 **C3B**
- 采用德州仪器的 **NanoStar™** 封装
- 低静态功耗:
 - I_{CC}=0.9μA** (最大值)
- 低动态功耗: **3.3V** 时的典型值,
 - C_{pd}=4.3pF**
- 低输入电容: **C_i=1.5pF** (典型值)
- 低噪声: 过冲和下冲
小于 **V_{CC}** 的 **10%**
- **I_{关闭}** 支持部分断电模式运行
- 施密特触发器的运行可实现低输入转换以及输入上更好的开关噪声抗扰度 (**V_{hys}=250mV**, 这是 **3.3V** 时的典型值)
- **0.8V 至 3.6V** 的宽运行 **V_{CC}** 范围
- 针对 **3.3V** 运行进行了优化
- 可耐受 **3.6V** 输入/输出 (I/O) 以支持混合模式信号运行
- **3.3V** 时, **t_{pd}=4.3ns** (最大值)
- 适合于点到点应用
- 锁存性能超过 **100mA** (符合 **JESD-78, II** 类规范的要求)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

说明

AUP 系列产品是 TI 针对业界对于电池供电便携式应用的低功耗需求的主要解决方案。此系列可确保在整个 0.8V 至 3.6V 的 V_{CC} 范围内实现超低静态和动态功耗，从而延长电池的使用寿命（请见图 1）。这个产品还保持了出色的信号完整性（请见图 2 中显示的极低下冲和上冲特性）。

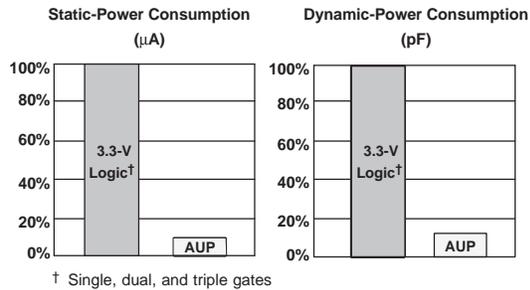


图 1. AUP - 最低功耗系列

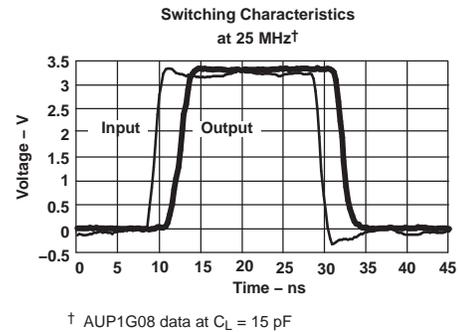


图 2. 出色的信号完整性

这个单路 2 输入正与门执行布尔函数：正逻辑中的 $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ 。

NanoStar 封装技术是集成电路 (IC) 封装理念的重要突破，这是因为此技术使用芯片作为封装。

该器件完全符合使用 $I_{\text{关闭}}$ 的部分断电应用的规范要求。 $I_{\text{关闭}}$ 电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T_A	ORDERABLE PART NUMBER ⁽²⁾	TOP-SIDE MARKING
-40°C to 125°C	SN74AUP1G08QDCKRQ1	SIT

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	L
H	L	L
H	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	4.6	V	
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V	
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V	
V _O	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature range	-65	150	°C	
ESD ratings	Human body model (HBM) AEC-Q100 classification level H2			2	kV
	Charged device model (CDM) AEC-Q100 classification level C3B			750	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN74AUP1G08-Q1	UNIT
		DCK (5 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance	304.7	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	115.3	
θ _{JB}	Junction-to-board thermal resistance	80.3	
ψ _{JT}	Junction-to-top characterization parameter	3.5	
ψ _{JB}	Junction-to-board characterization parameter	79.4	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

- (1) 有关传统和新的热 度量的更多信息，请参阅 *IC 封装热度量应用报告*，SPRA953。

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.9	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	-20	μA
		V _{CC} = 1.1 V	-1.1	
		V _{CC} = 1.4 V	-1.7	
		V _{CC} = 1.65 V	-1.9	
		V _{CC} = 2.3 V	-3.1	
		V _{CC} = 3 V	-4	
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20	μA
		V _{CC} = 1.1 V	1.1	
		V _{CC} = 1.4 V	1.7	
		V _{CC} = 1.65 V	1.9	
		V _{CC} = 2.3 V	3.1	
		V _{CC} = 3 V	4	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V	200	ns/V
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		T _A = 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} - 0.1			V _{CC} - 0.1		V _{CC} - 0.1		V
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		0.7 × V _{CC}		
	I _{OH} = -1.7 mA	1.4 V	1.11			1.03		1.03		
	I _{OH} = -1.9 mA	1.65 V	1.32			1.3		1.3		
	I _{OH} = -2.3 mA	2.3 V	2.05			1.97		1.97		
	I _{OH} = -3.1 mA		1.9			1.85		1.85		
	I _{OH} = -2.7 mA	3 V	2.72			2.67		2.67		
	I _{OH} = -4 mA		2.6			2.55		2.55		

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		T _A = 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1		0.1	V
	I _{OL} = 1.1 mA	1.1 V			0.3 × V _{CC}		0.3 × V _{CC}		0.3 × V _{CC}	
	I _{OL} = 1.7 mA	1.4 V			0.31		0.37		0.37	
	I _{OL} = 1.9 mA	1.65 V			0.31		0.35		0.35	
	I _{OL} = 2.3 mA	2.3 V			0.31		0.33		0.33	
	I _{OL} = 3.1 mA				0.44		0.45		0.45	
	I _{OL} = 2.7 mA	3 V			0.31		0.33		0.33	
	I _{OL} = 4 mA				0.44		0.45		0.45	
I _I	A or B input	V _I = GND to 3.6 V			0.1		0.5		0.5	μA
I _{off}		V _I or V _O = 0 V to 3.6 V			0.2		0.6		0.8	μA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V			0.2		0.6		0.8	μA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0			0.5		0.9		1.2	μA
ΔI _{CC}		V _I = V _{CC} - 0.6 V ⁽¹⁾ , I _O = 0			40		50		23	μA
C _i	V _I = V _{CC} or GND	0 V			1.5					pF
		3.6 V			1.5					
C _o	V _O = GND	0 V			3					pF

(1) One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V		21				ns
			1.2 V ± 0.1 V	1.5	8.5	14.7	1	17.2	
			1.5 V ± 0.1 V	1	6.2	10	0.5	11.3	
			1.8 V ± 0.15 V	1	5	7.7	0.5	9	
			2.5 V ± 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V ± 0.3 V	1	2.9	4.2	0.5	4.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V	24					ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.6	9.9	16.3	3.1	19.9	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.3	7.2	11.1	1.8	13.2	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	1.6	5.8	8.7	1.1	10.6	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1	4.3	5.9	0.5	7.3	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	3.4	4.8	0.5	5.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

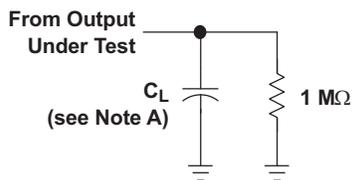
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V	32.8							ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.9	13.1	20.9	4.4	25.5	4.4	27.8	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3.4	9.5	14.2	2.9	16.9	2.9	18	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.5	7.7	11	2	13.5	2	19.7	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.8	5.7	7.6	1.3	9.4	1.3	11	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	4.7	6.2	1	7.5	1	8.7	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	4	pF
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	4	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	4	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	4.1	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	4.3	

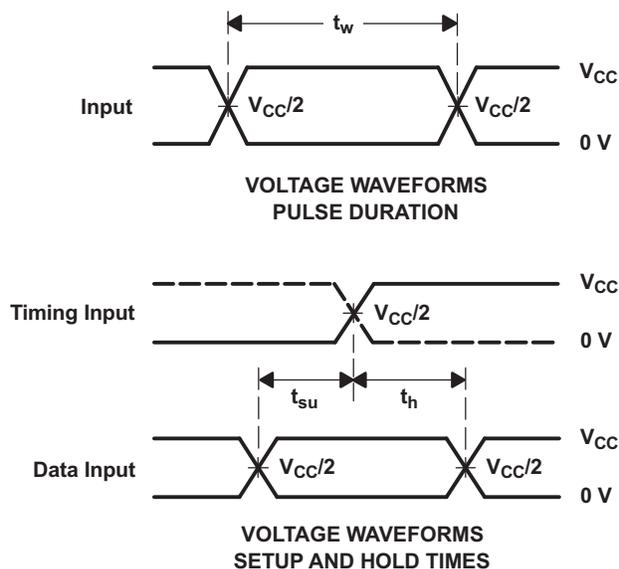
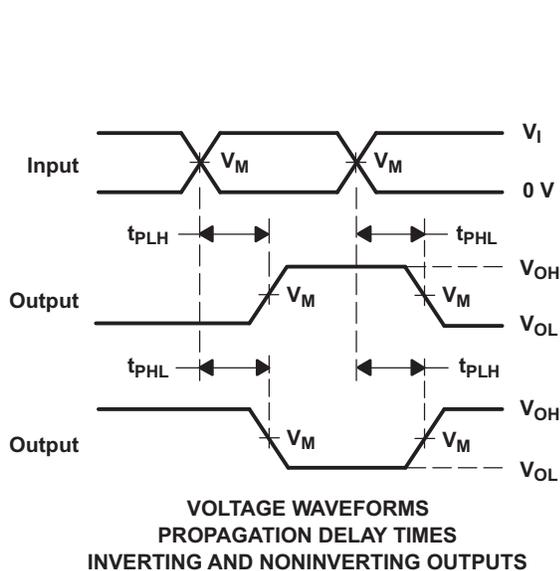
PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

$T_A = -25^\circ\text{C to } 85^\circ\text{C}$

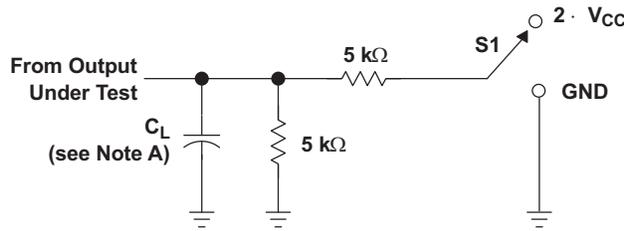
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)**

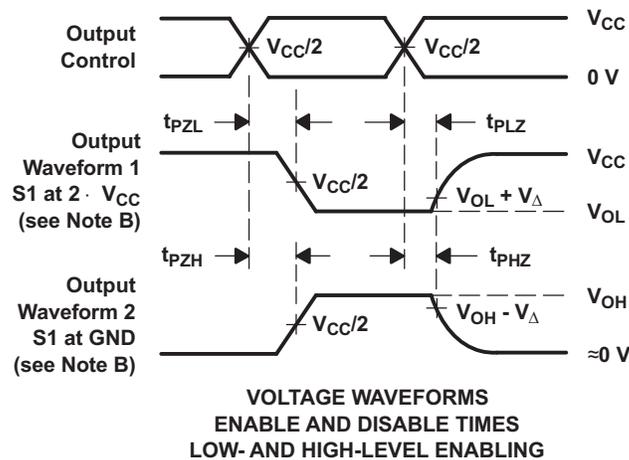


TEST	S1
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PHL}	GND

LOAD CIRCUIT

$T_A = -25^\circ\text{C}$ to 85°C

	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, slew rate $\geq 1\text{ V/ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G08QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(SIJ, SIT)
SN74AUP1G08QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(SIJ, SIT)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AUP1G08-Q1 :

- Catalog : [SN74AUP1G08](#)

NOTE: Qualified Version Definitions:

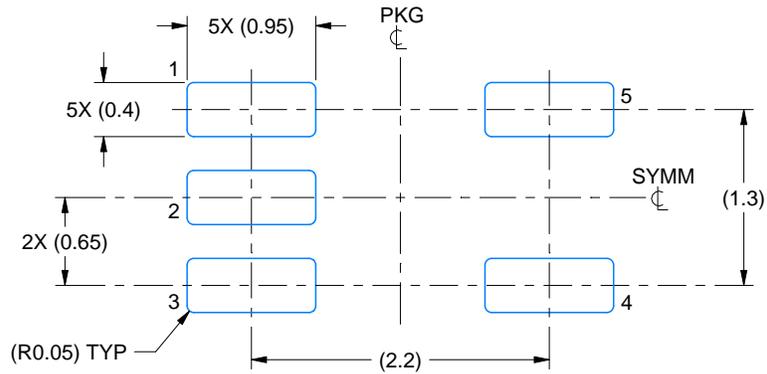
- Catalog - TI's standard catalog product

EXAMPLE BOARD LAYOUT

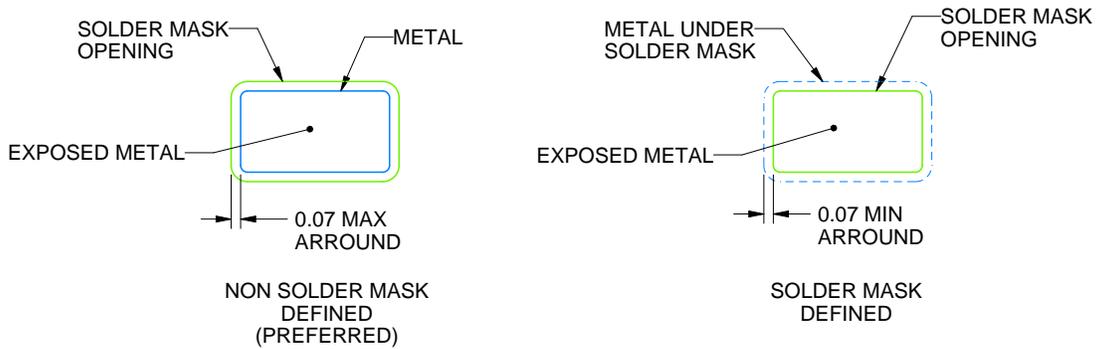
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

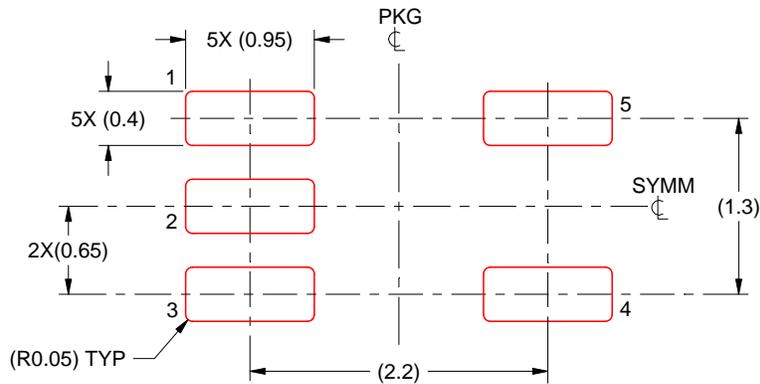
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司