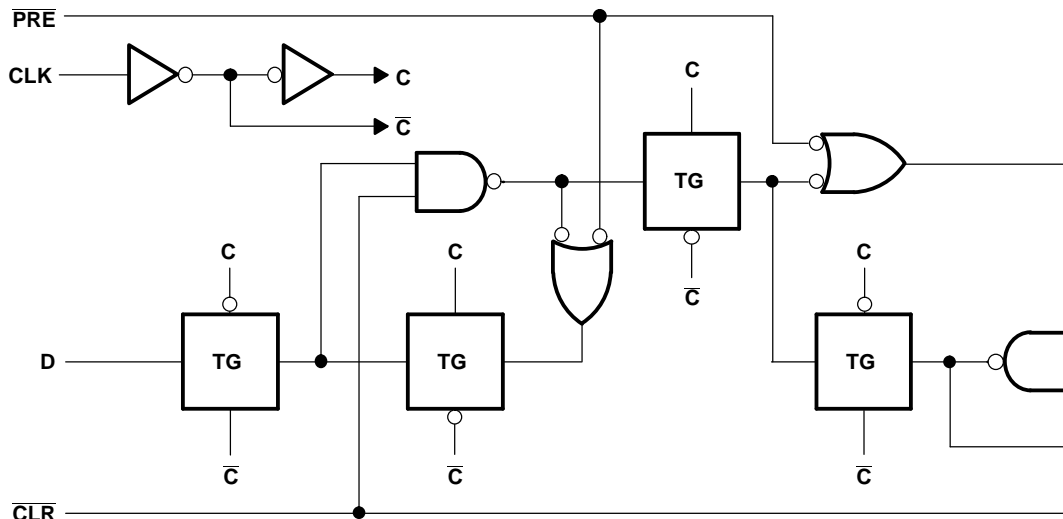


SN74AUC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES483A–AUGUST 2003–REVISED MARCH 2005

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	3.6	V
V_I	Input voltage range ⁽²⁾		-0.5	3.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	3.6	V
V_O	Output voltage range ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾			47	°C/W
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V		0	V
		V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V		0.7	
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V		−0.7	mA
		V _{CC} = 1.1 V		−3	
		V _{CC} = 1.4 V		−5	
		V _{CC} = 1.65 V		−8	
		V _{CC} = 2.3 V		−9	
I _{OL}	Low-level output current	V _{CC} = 0.8 V		0.7	mA
		V _{CC} = 1.1 V		3	
		V _{CC} = 1.4 V		5	
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
Δt/Δv	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = −100 μA	0.8 V to 2.7 V	V _{CC} − 0.1			V
	I _{OH} = −0.7 mA	0.8 V		0.55		
	I _{OH} = −3 mA	1.1 V		0.8		
	I _{OH} = −5 mA	1.4 V		1		
	I _{OH} = −8 mA	1.65 V		1.2		
	I _{OH} = −9 mA	2.3 V		1.8		
V _{OL}	I _{OL} = 100 μA	0.8 V to 2.7 V			0.2	V
	I _{OL} = 0.7 mA	0.8 V		0.25		
	I _{OL} = 3 mA	1.1 V			0.3	
	I _{OL} = 5 mA	1.4 V			0.4	
	I _{OL} = 8 mA	1.65 V			0.45	
	I _{OL} = 9 mA	2.3 V			0.6	
I _I	V _I = V _{CC} or GND	0 to 2.7 V			±5	μA
I _{off}	V _I or V _O = 2.7 V	0			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V			10	μA
C _i	D inputs	V _I = V _{CC} or GND	2.5 V		2	pF
	Control inputs	V _I = V _{CC} or GND	2.5 V		2.5	

(1) All typical values are at T_A = 25°C.

SN74AUC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES483A–AUGUST 2003–REVISED MARCH 2005

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	UNIT	
		TYP	MIN MAX	MIN MAX	MIN MAX	MIN MAX		
f _{clock}	Clock frequency	100	225	250	300	350	MHz	
t _w	Pulse duration	CLK high or low	4.6	1.3	0.6	0.5	0.5	ns
		CL $\overline{\text{R}}$ low	6.6	2	1.5	1.5	1.5	
		PRE low	4.8	1.8	1.5	1.5	1.5	
t _{su}	Setup time before CLK↑	Data	2.3	1	0.6	0.6	0.7	ns
		CL $\overline{\text{R}}$ inactive	0	0	0	0	0.3	
		PRE inactive	0	0	0	0.2	0.3	
t _h	Hold time, data after CLK↑	2.1	0.3	0.3	0.3	0.3	ns	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	UNIT
			TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
f_{max}			100	225	250	300	350	MHz
t_{pd}	CLK	Q or \overline{Q}	9.5	1.3 4	0.7 2.5	0.5 1.2 2.1	0.5 1.4	ns
	$\overline{\text{CLR}}$		10.5	1.5 4.1	1.1 2.9	0.9 1.4 2.4	0.7 1.6	
	$\overline{\text{PRE}}$		12	1.6 4.7	1.1 2.8	0.9 1.4 2.4	0.7 1.6	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30\text{ pF}$ (unless otherwise noted) (see Figure 1)

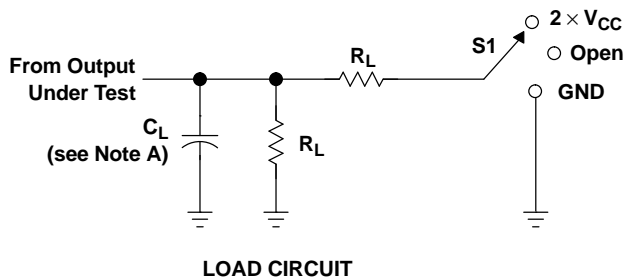
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			300			350		MHz
t_{pd}	CLK	Q or \overline{Q}	1.2	1.9	2.8	1	2.2	ns
	$\overline{\text{CLR}}$		1.3	2.1	3	1.1	2.4	
	$\overline{\text{PRE}}$		1.3	2.1	3.1	1.1	2.5	

Operating Characteristics

$T_A = 25^\circ\text{C}$

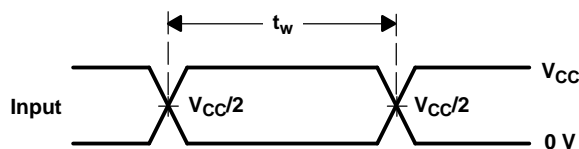
PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance $f = 10\text{ MHz}$	36	36	36	37	41	pF

PARAMETER MEASUREMENT INFORMATION

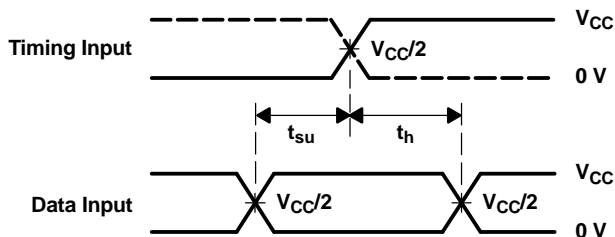


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

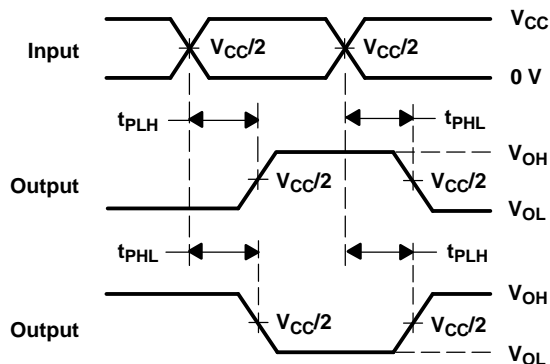
V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



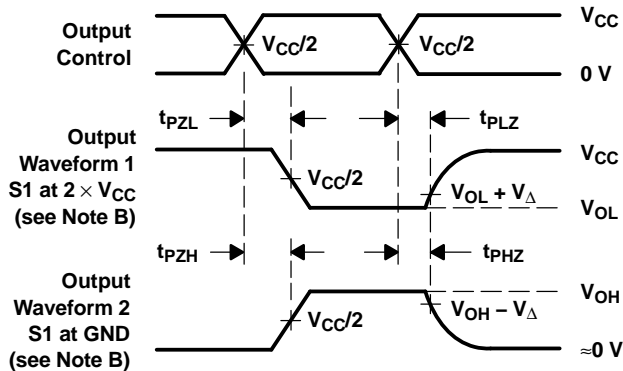
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate \geq 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUC74RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS74
SN74AUC74RGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS74

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC74RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC74RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

RGY 14

VQFN - 1 mm max height

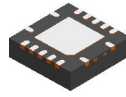
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



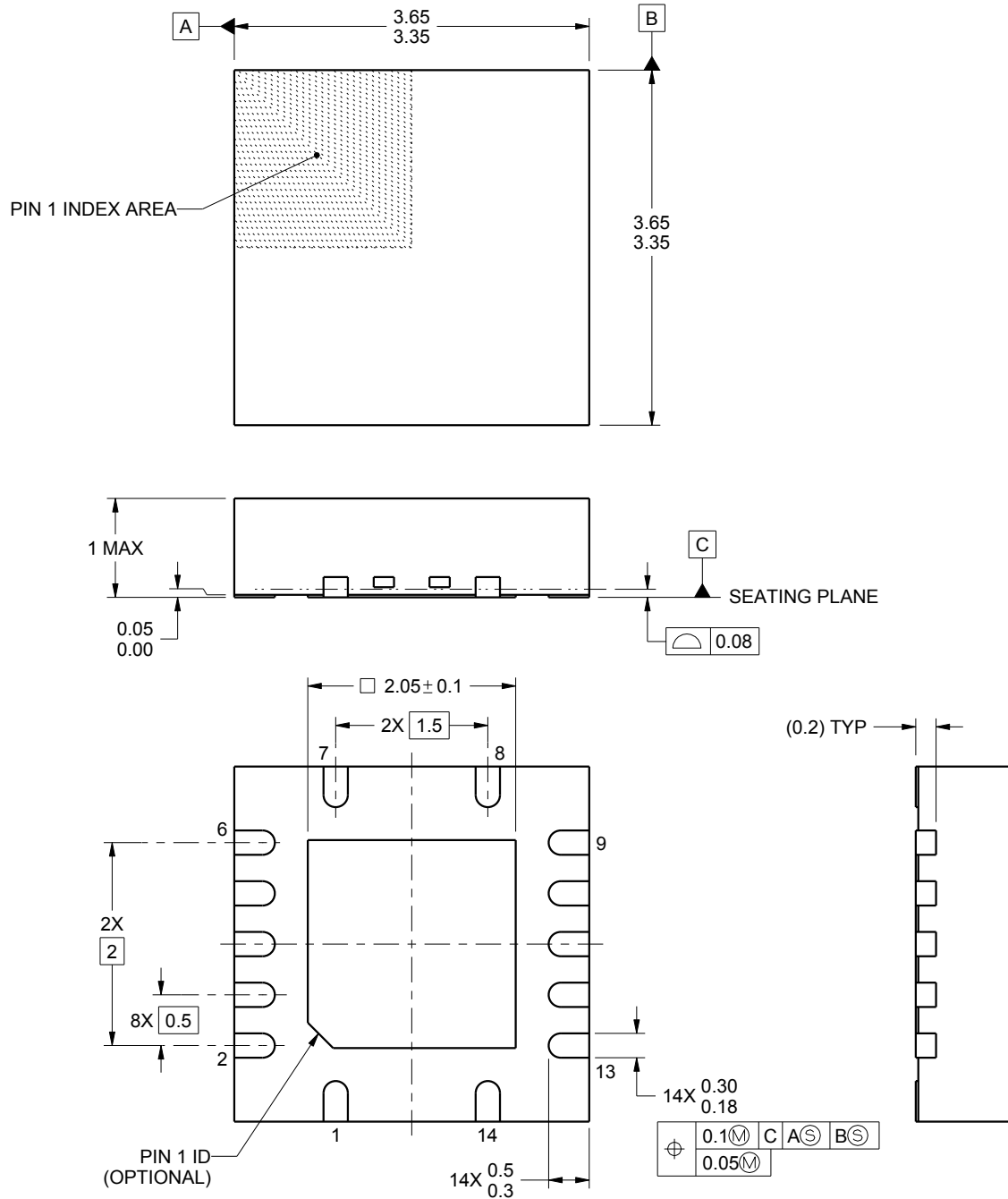
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

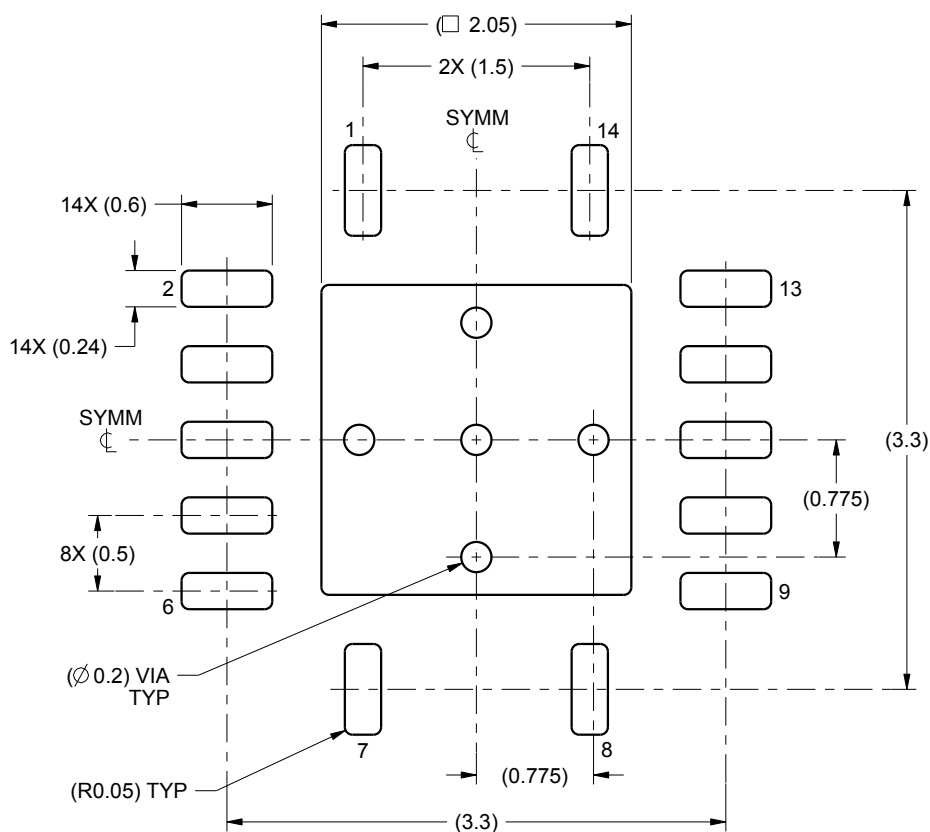
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

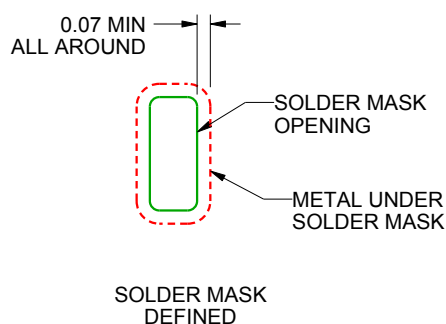
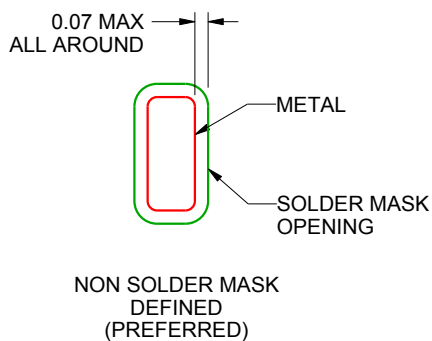
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

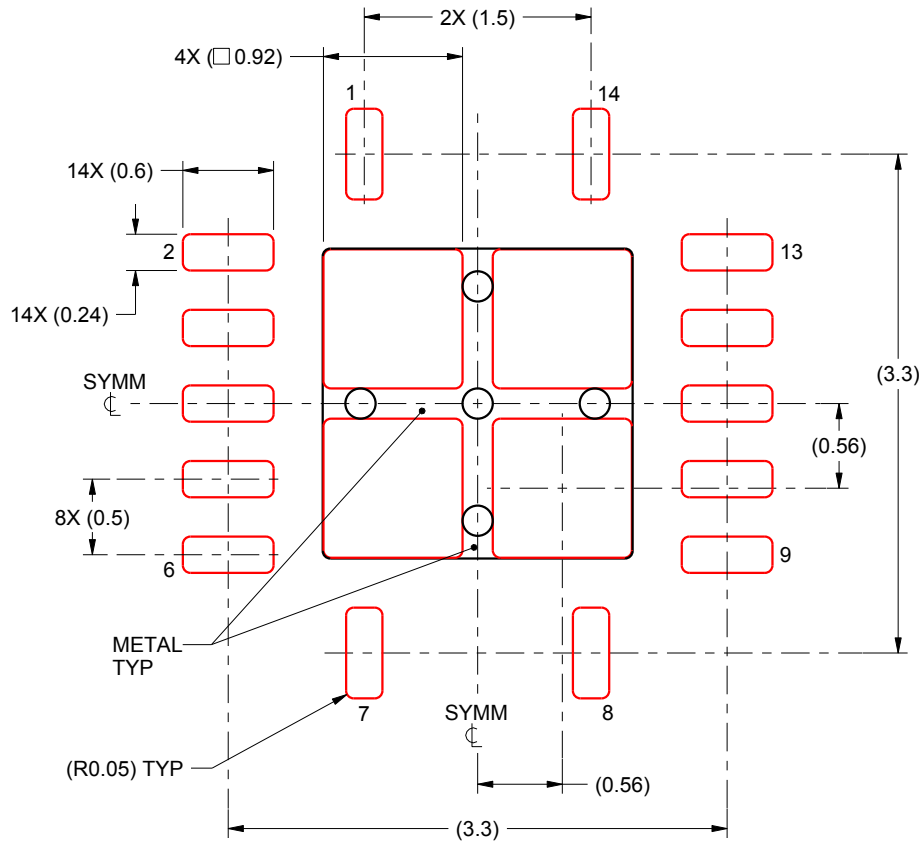
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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